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Modelling of symmetric switched capacitor multilevel inverter for high power appliances

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ABSTRACT

While designing the inverter, the total harmonic distortion (THD) in the output is a major concern to decide its performance. In order to calculate the total harmonic distortion (THD) of a symmetric modular multilevel inverter (MMI) with switched capacitors, a Harris hawk optimization (HHO) was used in this study. Utilizing symmetric and identical DC sources, the suggested modular multilevel inverter is designed. The suggested topology may be expanded up to many levels and utilizes fewer switches to provide 9 levels of output than conventi1al cascaded H-bridge multilevel inverters. Using a low-frequency switching control approach known as selective harmonic elimination pulse width modulation, the switches are less stressed and the inverter output's THD profile is improved. Additionally, the switching angles of the MMI have been optimized by solving the non-linear equations of the SHEPWM using the Harris Hawk Optimizer. Ant colony optimization (ACO) and particle swarm optimization (PSO), two alternative optimizers, were compared in terms of the THD of the output. This comparison shows that the HHO delivers a lower THD than other optimization techniques approximately near to 5%, as per the IEEE-519 standard, and is thus more highly advised. Finally, a hardware configuration for the suggested inverter is implemented to confirm the simulation findings.

KEYWORDS: THD, SHEPWM, PSO, ACO, HHO, Nine-Level Inverter
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1. INTRODUCTION

Inverters have several issues, including reduced efficiency, a high dv/dt ratio, increased power losses, and a high total harmonic distortion [1]. A multilevel inverter is designed to overcome these issues. The cascaded multilevel inverter is now widely used [2]. The multilevel inverter's output contains fewer harmonics than the binary inverter's output, signifying it is a more efficient converter. Multilevel inverters are also known as NPC, FC, and cascaded MLI [3-4]. Cascaded MLI control is simpler than other MLI control methods since it does not need clamping diodes or flying capacitors [5]. Multilevel inverters have been studied and developed for over three decades and have various industrial applications [6-7]. It should be highlighted that this is still a growing technology with some recent breakthroughs [8-10]. Multilevel inverters are becoming increasingly common. It is feasible to maintain several dc phases synthesizing the waveform output voltage while boosting power levels, and harmonic efficiency, and minimizing EMI emissions [11-13]. The applications include industrial variable frequency drives, electric cars, and grid-connected solar systems. Continuing research is developing efficient multilevel circuit configurations for high-power appliances. Modern multilevel inverters have fewer components and smaller carrier signals than older models. There are various levels and polarity-generating components [14-15] in this study. High-frequency switches create positive rates initially, and then low-frequency switches to reverse the voltage component. THD measures the inverter's performance [16]. Consequently, the complexity of higher-level control circuits is decreased by a large factor. This study built and tested a single-phase 9-level switched capacitor inverter employing SHEPWM and Harris Hawk Optimization. According to simulation results, the suggested inverter's harmonic distortion falls by nearly 5%, and the same was validated using a hardware model.

2. SUGGESTED SYMMETRIC INVERTER TOPOLOGY

The suggested inverter's schematic design is shown in Figure 1, together with the primary circuit for level generation and the secondary circuit for voltage reversal/polarity generation. An H-bridge inverts the output polarity every half cycle. A main circuit simultaneously creates up to 'n' levels of levels from dc sources. Direct current sources must be symmetrical for the inverter's input. Each direct current source is split into two equal halves so that fewer sources can produce the same output level. To prevent short-circuiting, the circuit makes use of a MOSFET and diodes [17]. See table.1 to compare the switching devices

and components of the proposed m-level inverter with the current standard design topologies. Figure 2 depicts the comparison between the number of switches (MOSFETs) needed for the proposed inverter and traditional inverters.

The following shows the relationship between the components utilized in the circuit design.

Number of capacitors (Nc) = 2 Nv,

Where Nv = Number of voltage sources

Number of Switches (Ns) = Nc + 4

Number of diodes (Nd) = Nc

Number of levels (Nstep) = 2Nc + 1

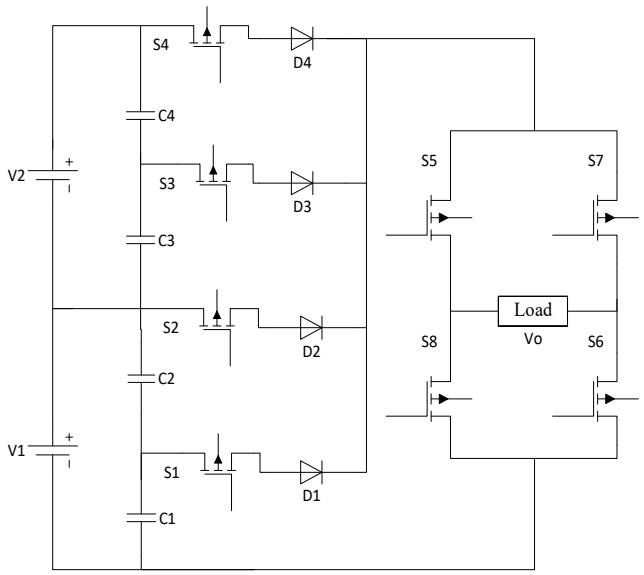


Figure 1. A 9-level Symmetric Switched Capacitor modular multilevel inverter

Table 1. Comparison of devices & components with proposed topology

Inverter	NPC MLI	FC MLI	CHB MLI	Proposed MMI
No of Switches	2 (k–1)	2(k–1)	2(k–1)	((k-1)/2) +4
No of Diodes	2 (k–1)	2(k–1)	2(k–1)	0
No of Clamping diodes	(k–1)* (k–2)	0	0	0
No of Capacitors	(k – 1)	(k – 1)	(k –1)/2	(k-1)/2
No of Balancing Capacitors	0	(k–1)* (k–2)/2	0	0

Where k represents the number of voltage levels.

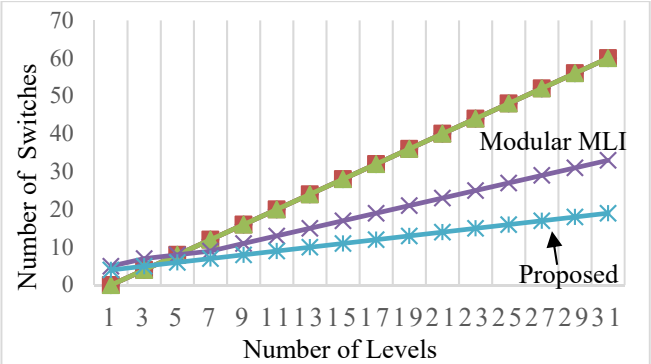


Figure 2. Number of switches Vs Number of levels

For the 9-level output V_o, this inverter has nine modes of operation: the first four modes produce positive voltage levels (V/2, V, 3V/2, 2V), and the following four produce negative voltage levels (-V/2, -V, -3V/2, -2V), and the ninth mode (0V) is achieved by switching the sequence shown in table 2.

Table 2. Switching modes for 9-level operation

Mode	S1	S2	S3	S4	S5	S6	S7	S8	O/P Voltage
I	1	0	0	0	1	1	0	0	**V/2**
II	0	1	0	0	1	1	0	0	**V**
III	0	0	1	0	1	1	0	0	**(3/2)V**
IV	0	0	0	1	1	1	0	0	**2V**
V	1	0	0	0	0	0	1	1	**-V/2**
VI	0	1	0	0	0	0	1	1	**-V**
VII	0	0	1	0	0	0	1	1	**-(3/2)V**
VIII	0	0	0	1	0	0	1	1	**-2V**
IX	0	0	0	0	0	0	0	0	**0**

3. PWM CONTROL AND SWITCHING OPTIMIZATION

A variety of modulation methods, such as high-frequency or low-frequency modulation, may be used to achieve a harmonic reduction in multilevel inverters. It is possible to effectively eliminate higher-order harmonics from an inverter's output using methods of high switching frequency modulation such as sine pulse modulation, stair-cased modulation, digital pulse width modulation, phase-shifted modulation, etc. In contrast, lower-order harmonics such as the 3rd and 5th harmonics, which are found in abundance in nature, will not be eliminated by high-frequency modulation methods [18-19]. Low-frequency topologies such as SVPWM and SHEPWM were introduced [20] to the system to address this problem. An approach for lowering the dominating harmonics of lower order as well as the switching losses of the hybrid multilevel inverter that has been proposed [21-22] was developed in this study, which used SHEPWM to accomplish this. The 9-level output is designed to produce a wave that is roughly sinusoidal in nature, as seen in the simulation in Figure 3.

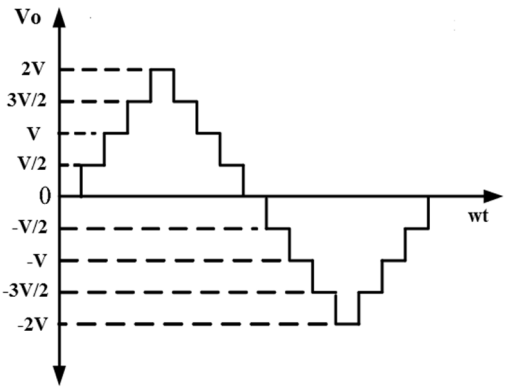


Figure 3. The approximated 9-level inverter output

3.1 Implementation of Fundamental Switching Frequency Control (SHEPWM)

Fundamental switching frequency control is one of the best PWM control methods for multilevel converters [23]. FSFC control can be achieved based on SHEPWM. Generally, the waveform of multilevel inverter output is expressed using Fourier series expansion. The generalized expression for Fourier series expansion is given in equation (1).

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \tag{1}$$

Here, V_n= nth harmonic voltage magnitude. Due to the odd symmetry of the quarter-wave, the even-order harmonics become zero. Therefore the expression for V_n becomes,

$$V_n = \begin{cases} \frac{4V_{dc}}{n\pi} \sum_{i=1}^{k} \cos(n\alpha_i); \text{for odd values of 'n'} \\ 0; \text{for even values of 'n'} \end{cases} \tag{2}$$

Where α_i is the switching angles of ith harmonic and is between 0°-90° (i.e. 0<$\alpha_i < \frac{\pi}{2}$).

SHEPWM aims to suppress lower-order harmonics, whereas harmonic filters remove the remaining harmonics. This research developed a 15-level asymmetric inverter with a fundamental switching frequency control scheme to conceal the 5th, 7th, and 11th harmonic voltages. The application of 15-level output will reduce the size of the harmonic filters as the prominent harmonics from the 5th to 11th harmonics are controlled. By expanding equation (2) for odd values of 'n', equation (3) can be obtained as;

$$\left.\begin{aligned} \tfrac{4V_{dc}}{\pi}[\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4] &= V_1 \\ \tfrac{4V_{dc}}{5\pi}[\cos5\alpha_1 + \cos5\alpha_2 + \cos5\alpha_3 + \cos5\alpha_4] &= V_5 \\ \tfrac{4V_{dc}}{7\pi}[\cos7\alpha_1 + \cos7\alpha_2 + \cos7\alpha_3 + \cos7\alpha_4] &= V_7 \\ \tfrac{4V_{dc}}{11\pi}[\cos11\alpha_1 + \cos11\alpha_2 + \cos11\alpha_3 + \cos11\alpha_4] &= V_{11} \end{aligned}\right\} \tag{3}$$

Where, V_5, V_7, V_{11} are the harmonic voltages of the 5th, 7th & 11th harmonics, respectively, which are required to suppress to reduce the THD of output voltage. Therefore, these are equated to zero, and the resulting equation can be represented in equation (5). The fundamental voltage component in equation (3) is equated to the modulation index corresponding PWM scheme, which can be written as:

$$M = \frac{V_1}{V_{1\max}} \tag{4}$$

Where,

V_{1max} = Peak fundamental voltage.

$$V_{1\max} = \frac{4kV_{dc}}{\pi}$$

V_1 = Fundamental component of voltage

k = Degree of freedom = $(N-1)/2$

N = No of levels

By combining (3) and (4) the above conditions can be written as follows.

$$\left.\begin{aligned} \tfrac{4V_{dc}}{\pi}[\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4] &= M \\ \tfrac{4V_{dc}}{5\pi}[\cos5\alpha_1 + \cos5\alpha_2 + \cos5\alpha_3 + \cos5\alpha_4] &= 0 \\ \tfrac{4V_{dc}}{7\pi}[\cos7\alpha_1 + \cos7\alpha_2 + \cos7\alpha_3 + \cos7\alpha_4] &= 0 \\ \tfrac{4V_{dc}}{11\pi}[\cos11\alpha_1 + \cos11\alpha_2 + \cos11\alpha_3 + \cos11\alpha_4] &= 0 \end{aligned}\right\} \tag{5}$$

The switching angles must not violate the constraints,

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \frac{\pi}{2} \tag{6}$$

The set of non-linear equations in (5) can be solved using constraint (6) to obtain the switching angles required for the fifteen-level inverter. These equations can be solved using a fundamental switching frequency control method and optimization methods to optimize the inverter's switching angles. Any optimization approach includes defining an objective function associated with the parameters to be assessed. The primary objectives are [24],

a. To obtain the value of the base voltage equivalent to any preset or expected value.
b. To suppress or reduce a few harmonics of lower order.

The inverter's switching angles influence the output harmonic voltages. The generalized harmonic voltage objective function (OF) consists of the following form to achieve the above objectives [25]:

$$OF = \min_{\alpha_k}\left\{\left(100\times\left(\frac{V_1^* - V_1}{V_1^*}\right)^4\right) + \sum_{k=2}^{N}\frac{1}{h_k}\left(50\times\frac{V_{h_k}}{V_1}\right)^2\right\} \tag{7}$$

To reduce the 5th, 7th, and 11th harmonics, the above objective function can be taken as:

$$FF = 100 * \frac{(V_{1d} - V_1)^4}{V_{1d}^4} + \left(\frac{50}{V_1}\right)^2 * \left(\frac{V_5^2}{5} + \frac{V_7^2}{7} + \frac{V_{11}^2}{11}\right) \tag{8}$$

Where, V_{1d} = Desired fundamental voltage, V_1 = Actual fundamental voltage, V_5 = Harmonic voltage of 5th Harmonic, V_7 = Harmonic voltage of 7th harmonic, and V_{11} = Harmonic voltage of 11th harmonic.

The aim of this research is to minimize the above objective function to reduce THD. The transcendental equations (5), satisfying the constraint function (6) with objective function (8), can be solved by using Harris hawk optimization for minimum THD and optimal switching angles. The comparison between different switching control methods with the proposed SHEPWM control.

3.2 Harris Hawk Optimization

An optimization model influenced by nature is the Harris Hawk Optimizer. The wild Harris' hawks' coordinated conduct and pursuit manner inspired HHO to call a surprise pounce. Several hawks cooperate together to swoop on prey from various angles. Harris hawks' chasing patterns vary based on the environment and the prey's escape strategies. For optimum MLI switching angles using SHEPWM, Harris hawk's knowledge

while hunting prey is mathematically formulated.

The Harris hawk has a distinctive community that aims to track, encircle, smoot, and capture the likely prey within a group. This species is among the most knowledgeable and distinguished birds of predatory nature. In the first population, seven killing tactics or surprise pounces are assumed to be a group of hawks who wish to achieve the aim (optimization problem solution). Suppose the animal does not catch because of the complication of appearance and the escaping actions of the prey. In that case, swaps are pursued to reach the other hawks in the group after capturing the escaping prey. The most significant advantage is that the birds follow their goal by puzzling and completing their escape. HHO gives Harris Hawks the solution, and the targeted pray is the best solution.

Step 1 - Exploration Phase: Harris hawks stick up arbitrarily, sit in certain areas, and follow and track the prey. The leader hawks are focused on the location of the communities and their prey. This is defined as a mathematical equation for the distance (q) switch between hawks and prey, as follows:

$$X(t+1)=\begin{cases} X_{rand}(t)-r_1X_{rand}(t)-2r_2X(t), & q\geq 0.5 \\ X_r(t)-X_m(t)-r_3(L_B+r_4(U_B-L_B)), & q<0.5 \end{cases} \quad (9)$$

Where, r_1, r_2, r_3, r_4 *and* q are the random values between 0 and 1. $X(t+1)$ is the position update vector of the Hawk for the $(i+1)^{th}$ iteration, $X_r(t)$ is the position of the prey and $X(t)$ is the position vector of the Hawk at the i^{th} iteration. U_B & L_B are the Upper & Lower bounds, respectively and $X_{rand}(t)$, and $X_m(t)$ are the random populations.
Each Hawk has an average position as:

$$X_{i+1}(t)=\frac{1}{N}\sum_{i=1}^{N}X_i(t) \quad (10)$$

Where, $X_i(t)$ = Hawks current position, $X_{i+1}(t)$ = Updating position vector, N = Number of Hawks.

Step 2 - The hawks are attempting to identify and reach the prey during the exploration phase. As a result, the energy (E) of the prey is significantly modified and provided by Escaping Energy, $E=2E_0\left(1-\frac{t}{T}\right)$ (11)

Where T is the maximum iteration number, t is the current iteration, and the initial energy (E_0) varies at random from (-1 to 1) during each iteration. $E\geq 1$ Indicates that the prey is tired and that hawks are looking for prey in a new location. $E<1$. Also indicates that the prey is tired and that its attack is intensified by fast striking.

Step 3 - Exploitation phase: The switching tactics will begin to focus on the prey at this stage. The prey still tends to escape from the hawks, and it is seen that the potential to escape the prey is 'r'. If r<0.5 the prey can escape safely; if r≥0.5 it would be unable to escape. Even so, the hawks target the prey and win or lose in a soft or hard siege. The hard siege takes place as the prey escapes if (r≥0.5) and $|E|<0.5$. If (r≥0.5) and $|E|\geq 0.5$ then there will be a soft siege. 'r' is a chance for the prey to escape here. It can be modeled in the following mathematical form in steps 4 to 7.

Step 4 - Soft siege: The prey here (switching angle for proposed problem) has potential and is trying to escape by sprouting and is smoothly modeled around the hawks.

$$X(t+1)=\Delta X(t)-E|JX_\alpha(t)-X(t)| \quad (12)$$

$$\Delta X(t)=X_\alpha(t)-X(t) \quad (13)$$

$J=2(1-r_5)$ is the prey jumps at random, $\Delta X(t)$ is the difference in the position of the vector in successive iterations to r_5, which is a random number inside the (0,1) range.

Step 5 - Hard siege: The prey in this situation is completely tired and barely surrounded by the hawks and surprise. The locations will be updated by (13),

$$X(t+1)=X_\alpha(t)-E|\Delta X(t)| \quad (14)$$

Step 6 - Soft siege with continued rapid dives: The prey still has the energy and is attempting to get away from it, which can be summarized as total and r<0.5, with a soft siege needed to begin until the hawks begin to pounce. This move is more intelligent than in the past. The Levy flight (LF) concept has been applied to progressive rapid dives of hawks for the soft siege, and the next move is calculated by the hawks using the following equation:

$$Y=X_\alpha(t)-E|JX_\alpha(t)-X(t)| \quad (15)$$

Although they have attempted several times, the Hawks compare each movement with the previous dive to determine whether it was successful. If diving is unsuccessful, the animal is treated irregularly, briefly, and rapidly. We presume that the Hawks dive into the following rules based on LF patterns:

$$Z=Y+S\times LF(D) \quad (16)$$

Where D is the dimension of the problem, S is the random vector 1 to D, and LF is the levy flight function to follow:

$$LF(x)=0.01\times\frac{\mu\times\sigma}{|v|^{1/\beta}} \quad (17)$$

$$\sigma=\left(\frac{\tau(1+\beta)\times\sin\left(\frac{\pi\beta}{2}\right)}{\tau\left(\frac{1+\beta}{2}\right)\times\beta\times 2^{\left(\frac{\beta-1}{2}\right)}}\right)^{\frac{1}{\beta}} \quad (18)$$

Where u and v are unintended values (0, 1) and β are expected to be 1.5. Therefore, in the soft siege phase, the last upgrade rule of the hawk position is:

$$X(t+1)=\begin{cases} Y, F(Y)<F(X(t)) \\ Z, F(Z)<F(X(t)) \end{cases} \quad (19)$$

Where Y and Z are calculated using (15) and (16).

Step 7 - In this case, a hard siege of relentless quick dives: and r<0.5 are lost and exhausted. The hawks then use a hard siege, in which they keep their distance from the prey to kill it. The updating rule in this case is:

$$Y=X_\alpha(t)-E|JX_\alpha(t)-X(t)| \quad (20)$$

$$Z=Y+S\times LF(D) \quad (21)$$

For the latest iteration, Y and Z at (20) and (21) are the next positions before the prey is killed, i.e. the optimal solution is achieved. The SHEPWM transcendental equations are solved using the Harris hawk optimization method to get the switching angles of the proposed 9-level inverter. The switching angles for various modulation indexes are computed and stored in

lookup tables, satisfying all load conditions. For a given modulation index or varying load conditions, these angles are retrieved from memory in real-time. The switching angles for the modulation index from 0.5 to 1 were determined using the Harris hawk algorithm.

4. RESULTS AND DISCUSSIONS

4.1 Simulation Results

In this study, the optimization problem given by equation (7) is evaluated using PSO, ACO, and HHO as a function of the modulation index, and the convergence characteristics are shown in figures 4, 5, and 6 for the 9-level operation of the inverter using two identical dc sources. Figure 7 depicts the variation of the modulation index with the switching angles of the proposed topology.

According to the convergence characteristics shown in Figures 4, 5, and 6, the best value of fitness in this study is in the vicinity of the modulation index of 0.85 or below. The switching angles determined for a modulation index of 0.85 using HHO are illustrated in Figure 7 and are listed in Table 3 as a consequence of the optimization algorithms PSO and ACO.

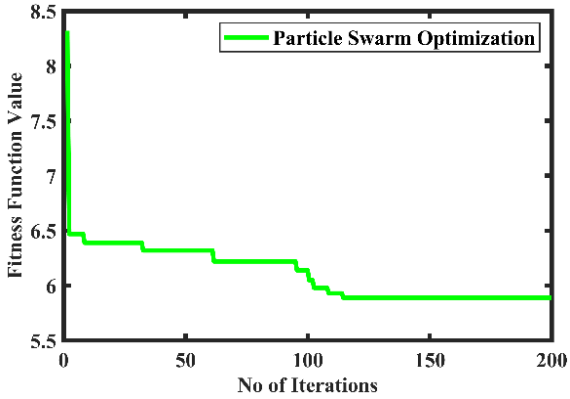


Figure 4. Convergence Characteristics using PSO

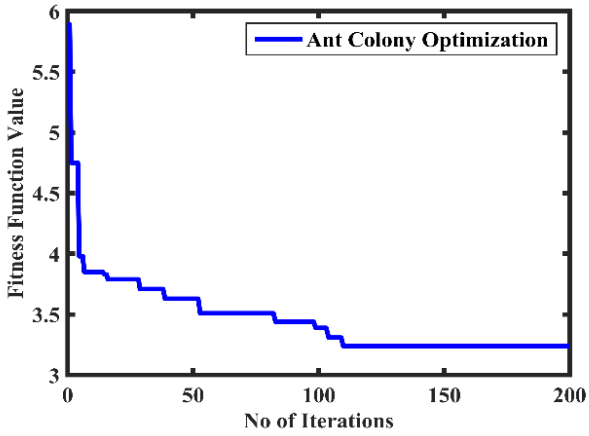


Figure 5. Convergence Characteristics using ACO

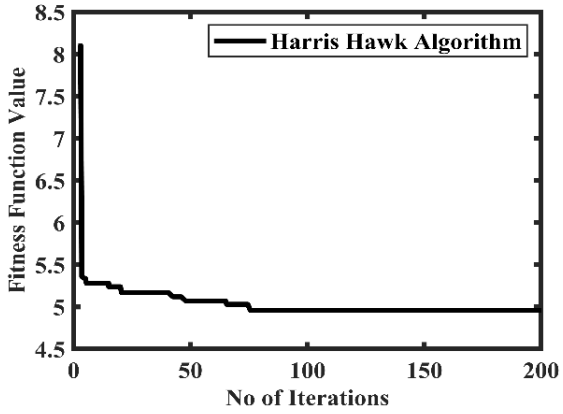


Figure 6. Convergence Characteristics using HHO

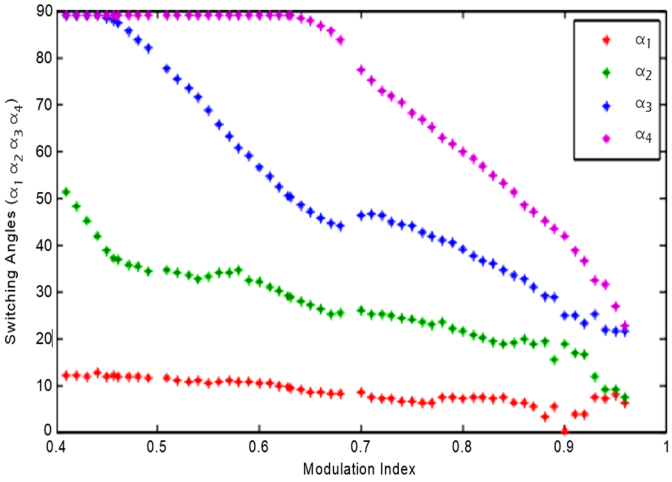


Figure 7. Switching angles Vs modulation index using HHO

Table 3. Optimal switching angles and corresponding THD

Algorithm	Modulation Index (MI)	Optimized Switching Angles (degrees)				THD %
		α_1	α_2	α_3	α_4	
PSO	0.85	9.83	20.32	38.32	60.21	9.49
ACO		9.46	19.65	36.92	59.45	6.25
HHO		8.94	18.69	35.69	56.45	5.73

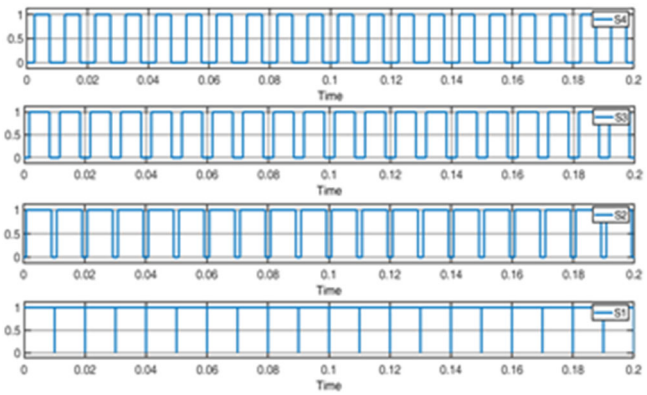


Figure 8. Switching pulses of level generation part

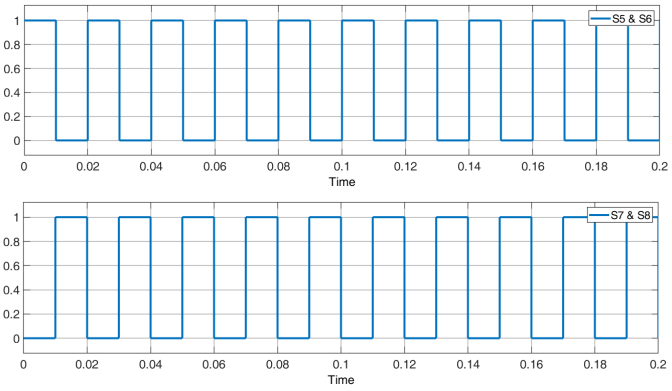


Figure 9. Switching pulses of polarity generation part

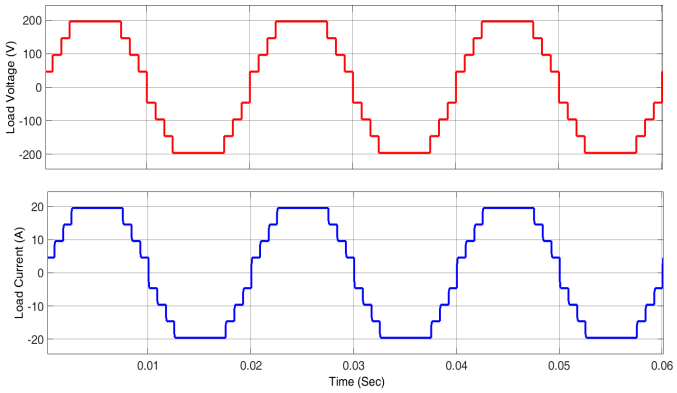
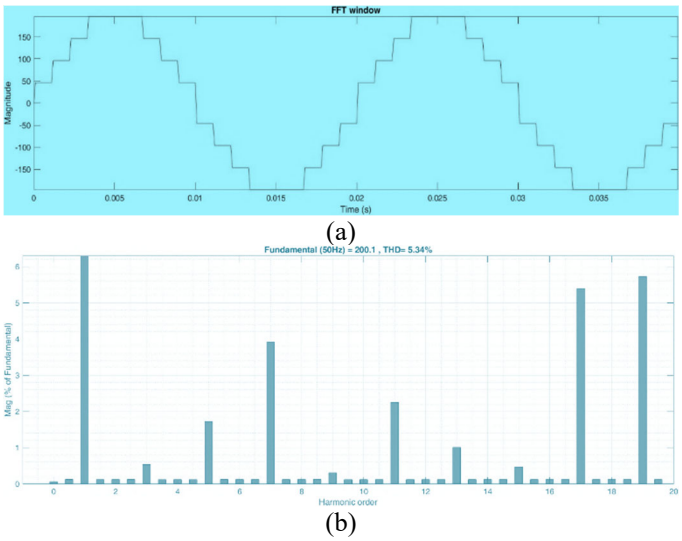


Figure 10. Load voltage and load current waveforms of 9-level output

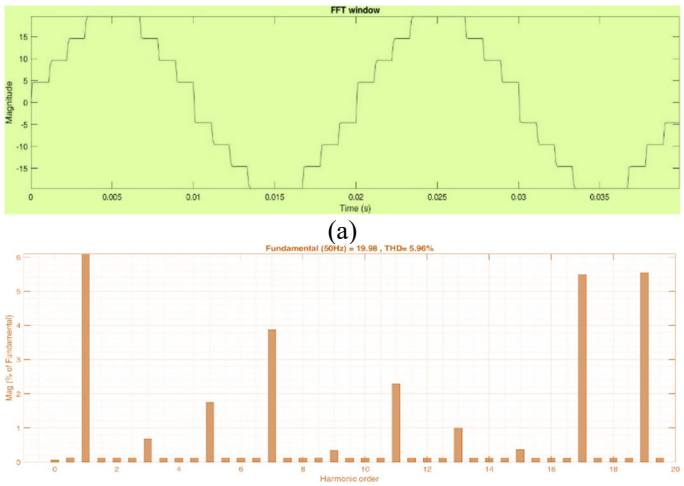
The HHO Algorithm takes 70 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in Figure 6. The switching pulses of the primary circuit are illustrated in Figure 8. Also, Figure 9 presents the triggering pulses of the polarity generation part. The output voltage and current waveforms of nine-level inverters are presented in Figure 10. The THD of output voltage and output current of the 9-level inverter is measured with switching angles computed by the HHO algorithm at 0.85 modulation index. The THD of o/p voltage is 5.34% at 200.1V, shown in Figure 11 and the THD of output current is 5.96% at 19.98A, as shown in Figure 12.



(a)

(b)

Figure 11. Voltage harmonic distortion using HHO
(a) FFT Window (b) THD of output voltage



(a)

(b)

Figure 12. Current harmonic distortion using HHO
(a) FFT Window (b) THD of output current

4.2. Experimental Framework

The suggested nine-level MLI framework is constructed. Figure 13 depicts the laboratory equipment arrangement. The MLI's H-bridge and level developer are comprised of eight switches (IRF840N MOSFET). The switching pulses to the MOSFETs in the proposed 9-level inverter are generated by an IC AT89C51 microcontroller. The output voltage waveform for R-L Load (R=10 & L=0.5mH) is shown in Figure 14. The Harris hawk optimization approach is used to determine the ideal switching angles necessary to remove harmonics of the fifth and seventh orders. The THD in the framework's output voltage is 5.97%, which is almost equivalent to the 5.34% achieved from the Simulink for the HHO control method. The modeling and experimental results illustrate the suggested 9-level inverter's validity and practicality. It is determined from this study that the HHO would result in a lower THD for the proposed inverter with selective harmonic removal. The THD analysis of the hardware framework is presented in Figure 15 using a power quality analyzer.

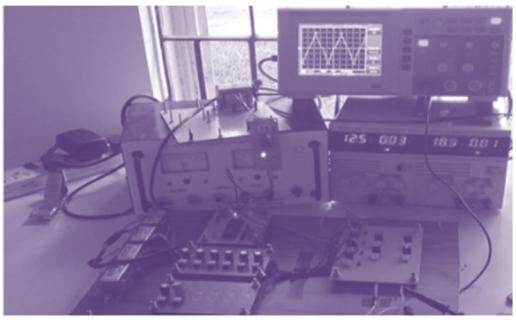


Figure 13. The hardware setup of 9-level MLI

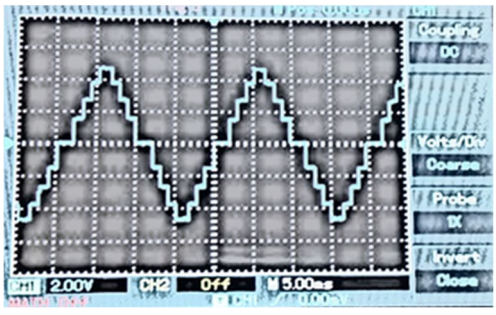


Figure 14. The output voltage of nine-level MLI

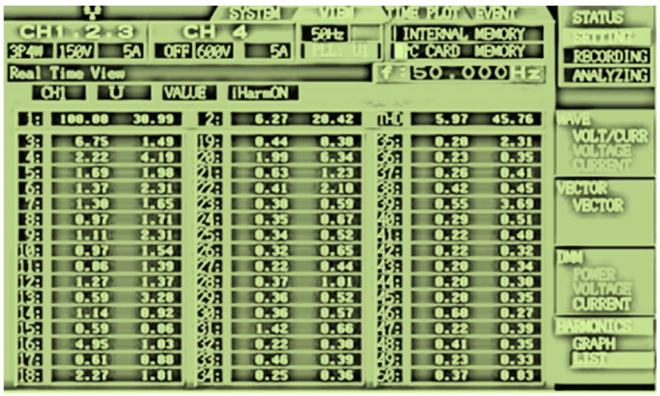


Figure 15. THD analysis of 9-level MLI using Power Quality Analyzer

5. CONCLUSIONS

A nine-level symmetrical inverter with fewer switches was proposed in this research. Selective harmonic elimination pulse width modulation is utilized to reduce THD in the multilevel inverter. Optimizing methods such as PSO, ACO, and HHO were used to find optimal switch angles for the proposed 9-leve MMI. This study concludes that the Harris hawk optimization approach reduces THD in comparison to other optimizers. The inverter's output voltage gives 5.34% THD. As a result, the proposed inverter works with a variety of single-phase loads. There is 5.34% THD from the Simulink model, whereas the framework model has 5.97% THD. Thus, the results obtained from the simulation are validated with experimental results using the HHO algorithm.

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NOMENCLATURE

THD	Total Harmonic Distortion
MMI	Modular Multilevel Inverter
PSO	Particle swarm optimization
ACO	Ant Colony Optimization
HHO	Harris Hawk Optimization
PWM	Pulse Width Modulation
SHEPWM	Selective Harmonic Elimination PWM
SVPWM	Space Vector Pulse Width Modulation
MLI	Multilevel Inverter
NPC	Neutral Point Clamping
FC	Flying Capacitor
CHB	Cascaded H-Bridge
N_{Switch}	Number of Switches
N_{Gate}	Number of Gate Drivers
N_{Source}	Number of DC Sources
N_{Diode}	Number of Switched Diodes
N_{DClink}	Number of DC link Capacitors
T_{Block}	Total Blocking Voltage