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Implementation of an asymmetric multilevel inverter for solar photovoltaic applications using N-R approach

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ABSTRACT

Two-level inverters are the most basic kind of multi-level inverter (MLIs). Total harmonic distortion diminishes as the number of output levels is increased. In classic MLI topologies, more electronic components are utilized to get higher-level outputs, which raises the cost, complexity, and volume of typical MLI installations. By reducing the use of power components, overall costs can be reduced. Further, the two and three-level inverters produce constant dv/dt output, which increases the stress on the power switches. This research proposed an asymmetric MLI topology that is suitable for PV applications and utilizes a minimum number of components. A selective harmonic elimination-based pulse width modulation (SHEPWM) is implemented for the proposed inverter to eliminate the lower-order dominant harmonics. The non-linear transcendental equations produced by the SHEPWM are solved for the switching angles of the proposed inverter using the Newton-Raphson approach. The performance of the inverter is analyzed based on the THD of output for different operating levels of the inverter. In this research, the NR method yielded a THD of 7.3% at a 0.9 modulation index. Also, the proposed inverter is applied to grid-connected solar PV systems for the analysis of THD.T The THD of the grid voltage is measured as 0.06% and the THD of the grid current is 4.8% with the proposed inverter which is acceptable as per the IEEE519 standards.

KEYWORDS: THD, Optimized inverter, N-R method, Asymmetric Inverter, SHEPWM

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1. INTRODUCTION

Designing medium-voltage converters for multiple applications such as motor drives, solid-state transformers, and solar photovoltaic presents some common problems such as difficulties with large-scale photovoltaic systems, which complicate the converter and control circuit. Multilevel inverter theory was first introduced in 1971 as a substitute for medium-power applications for a series of connected power electronic switching devices [1]. During the 1971-1981 era, the MLIs such as neutral point clamped (NPC), a flying capacitor (FC), and cascaded H-bridge (CHB), were suggested [2]. Because of its basic circuit design, the idea of a three-level NPC converter has become more popular and is still commercially available. However, the rise in levels of neutral point clamped topology considerably increases the number of clamping diodes [3]. The inverse retrieval times of the clamping diode render this topology feasible to develop an inverter with more levels for medium power applications [4]. Hence, the neutral point clamped topology and the flying capacitor topologies are too inadequate for MV and HV applications because they use many condensers requiring prior charging and balancing of the capacitors [5-6]. Furthermore, a large dc-link capacitor needed for single-cell topology limits its application to medium and high voltages, particularly solar PV applications, where different PV panels are connected in series [7]. This vast number of series-connected PV panels will decrease the overall system efficiency due to common MPPT and series resistance [8-9]. Modular structures have been developed by cascading the full-bridge inverters, named multi-cell multilevel CHB converter topology, which provides MPPT operation at the module level and is scalable to various voltage levels. Also, clamping diodes and capacitors are not used by CHB topologies [10].

The CHB is getting rid of the more series PV modules; however, continuous module parameters and partial shading will cause mismatch problems [11]. These mismatch problems create imbalance and result in low quality of power to the grid [12]. While using CHB converters for PV applications, this module mismatch is another challenge compared to converters in solid-state transformers and solid-state motor drives. In new industrial and academic research paradigms, multilevel inverters have evolved dramatically because of their ability to produce high-quality output at reduced costs. Philosophers have worked on lowering inverter costs by utilizing fewer components. The main aim of a multilevel topology of the inverter is to incorporate the harmonic profile into the IEEE-519 standard, which eliminates the need for heavy filters [13]. Multiple targets such as minimum THD, low dv/dt stress, and lower common-mode voltages are available to guarantee the use of electric motors. Electromagnetic interference (EMI) problems are less frequent on multilevel inverters than on conventional 2-level and 3-level inverters [14]. In general,

researchers aimed at increasing the basic units in series or cascading the basic unit to get more output voltage levels to improve the inverter's efficiency at lower THD [15]. The inverter perceives its usefulness in PV-fed UPS, propulsion systems, integration of green energy sources, aero planes, battery-powered vehicles, etc. A simple control strategy is necessary to reduce the complexity of multilevel inverters. Therefore, the investigators focused on efficient topology architecture and modulation [16-17].

This paper presented an asymmetric MLI structure with a minimum switch count by avoiding the use of bidirectional switches, clamping diodes, and capacitors in its design. In addition, the proposed converter does not affect diode reverse recovery times, and capacitor voltage balancing and uses a simple gate control circuit due to the absence of bidirectional switches [18-20]. A low switching frequency control method is used for the proposed inverter to eliminate the lower-order harmonics [21-22]. A numerical technique, known as the Newton-Raphson method, is used to find a viable solution to the transcendental equations for determining the inverter's optimal switching angles. The proposed inverter is operated for different possible levels (seven-level, eleven-level, fifteen-level), and the corresponding THDs are analyzed.

2. IMPLEMENTATION OF ASYMMETRIC INVERTER

This research presented a simple design topology of an asymmetric inverter suitable to variable dc sources such as SPV systems [23]. The basic cell configuration of the suggested model is given in Figure 1(a). It has a single voltage source in series with a power switch connected across the bypass diode. During the switch 'S' is turned ON, the source voltage 'V' appears at the load, then $V_{dc\text{-}out}$ becomes source voltage 'V', and while the switch 'S' is turned OFF, then the source voltage is isolated from the load; hence $V_{dc\text{-}out}$ is '0'.

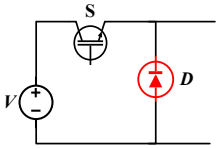


Figure 1 (a). The basic cell configuration

Basic cell structures are cascaded, as shown in Figure 1(b) for 'n' cell structure of the suggested configuration of the inverter, known as the primary circuit.

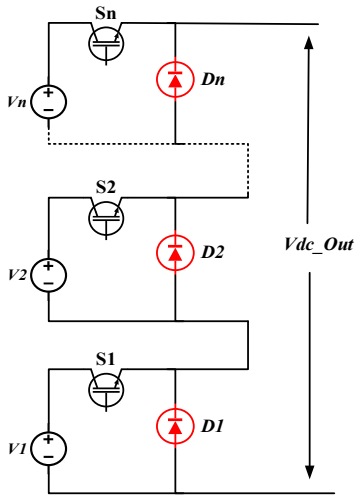


Figure 1 (b). 'n' cell cascaded primary circuit

However, this 'n' cell configuration can generate a multilevel output only with a positive polarity. The bidirectional output of the inverter can be obtained with polarity reversal by connecting an H-bridge auxiliary circuit at the output of the primary circuit, as shown in Figure 1(c).

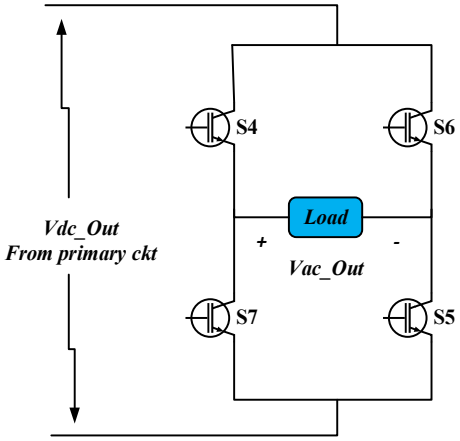


Figure 1 (c). Auxiliary Circuit

Therefore, the full cycle of the output's +ve and -ve polarity is achieved by combining the primary and auxiliary circuits. This structure synthesizes 15-output voltage levels with 7-positive, 7-negative, and a zero level using a polarity generator (auxiliary circuit) like the H-bridge module.

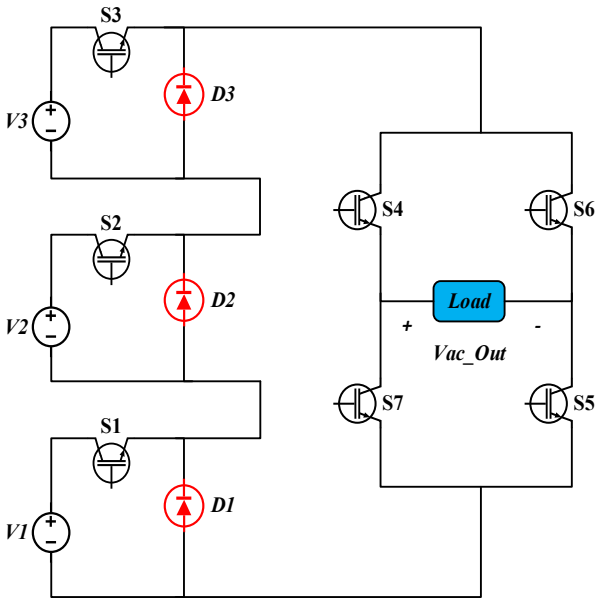


Figure 2. Proposed asymmetric inverter topology

The topology of the proposed multilevel inverter for 15-level output is shown in Figure 2. In its design, the primary circuit is cascaded with three basic cell structures and interconnected across the auxiliary circuit, which uses three dc sources, seven controlled switches (IGBTs), and 3-diodes. The proposed topology and switching path choices are appropriately configured so that IGBTs or diodes can never dead short-circuit with the dc sources. The rating of numerous dc sources depends on the magnitude of output levels. The dc source reduced voltage rating specifies V_{dc} step voltage at the output. Different potential dc voltage source combinations are presented in Table 1.

Table 1. Choice of dc sources for suggested topology

Method of Selection	Choice of DC Sources	No of Steps	No of Levels	Max. O/p Voltage
Equal Magnitude	$V_1=V_2=V_3=V_{dc}$	4	7	$3V_{dc}$
Unequal Magnitude	$V_1= V_{dc}$, $V_2=V_3=2V_{dc}$	6	11	$5V_{dc}$
Binary Approach	$V_1= V_{dc}$, $V_2= 2V_{dc}$, $V_3= 4V_{dc}$	8	15	$7V_{dc}$

The binary approach is considered for this study among the above three choices of dc source selection. Since multilevel inverters work with high efficiency at low switching and conduction losses, output voltage levels significantly increase with the minimum number of sources and switching devices. Therefore, the choice of voltages for 15-level output is as follows,

$$V_1= V_{dc}, \quad V_2= 2V_{dc}, \quad V_3= 4V_{dc}$$

This approach also offers asymmetrical operation to multilevel inverter ideal for variable PV voltages due to variable solar irradiance. The switching sequence for different output step voltages varies from +7 V_{dc} to -7 V_{dc}, including the '0' voltage level.

The switches S_4 and S_5 in the auxiliary circuit continuously conduct 7 levels of +ve half cycle of output voltage and switches S_6 & S_7 conduct for 7 levels of a -ve half cycle of output. The '0' output level is obtained by either a short circuit of load with switches S_4 & S_6 ON, or S_5 & S_7 ON. Thus, the fifteen-level output voltage is obtained from the proposed converter by operating the primary and axillary circuits according to the switching conditions described in Table 2.

Table 2. Asymmetric switching sequences and output voltage levels of the proposed 15-level inverter

ON Switches	Power flow path	Output voltage level
S_1, S_2, S_3, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+7V_{dc}$
S_2, S_3, S_4 & S_5	$V_2^+ \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow V_2^-$	$+6V_{dc}$
S_1, S_3, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+5V_{dc}$
S_3, S_4 & S_5	$V_3^+ \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3^-$	$+4V_{dc}$
S_1, S_2, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$Load $\rightarrow S_5 \rightarrow V_1^-$	$+3V_{dc}$
S_2, S_4 & S_5	$V_2^+ \rightarrow S_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow V_2^-$	$+2V_{dc}$
S_1, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+V_{dc}$
S_4 & $S_{6\,(or)}$ S_5 & S_7	$S_4 \rightarrow$ Load $\rightarrow S_6 \rightarrow S_4$ (or) $S_5 \rightarrow$ Load $\rightarrow S_7 \rightarrow S_5$	0
S_1, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-V_{dc}$
S_2, S_6 & S_7	$V_2^+ \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow V_2^-$	$-2V_{dc}$
S_1, S_2, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$Load $\rightarrow S_7 \rightarrow V_1^-$	$-3V_{dc}$
S_3, S_6 & S_7	$V_3^+ \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3^-$	$-4V_{dc}$
S_1, S_3, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-5V_{dc}$
S_2, S_3, S_6 & S_7	$V_2^+ \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow V_2^-$	$-6V_{dc}$
S_1, S_2, S_3, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-7V_{dc}$

3. COMPARISON WITH SIMILAR TOPOLOGIES

A reduced switch multilevel inverter's main goal is to add levels while using fewer electrical components. Therefore, a number of comparisons between the recommended topology and other cascaded inverters of the same sort were made, including switch count, number of diodes, and dc sources.

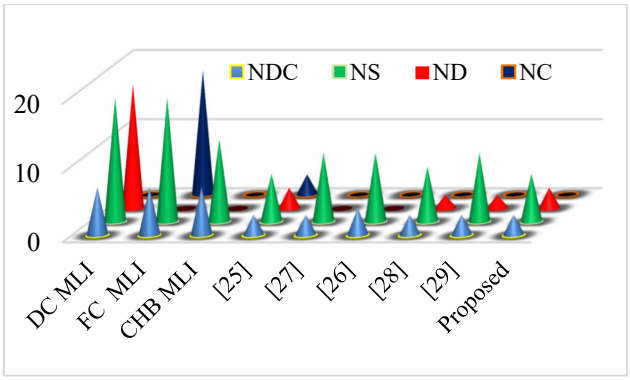


Figure 3. Comparison between the existing 15-level asymmetric topologies and the proposed 15-level inverter

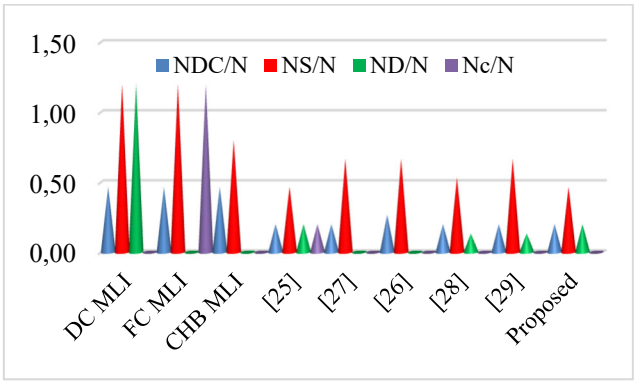
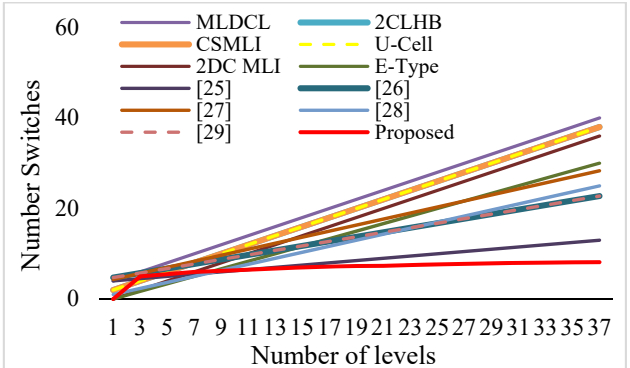
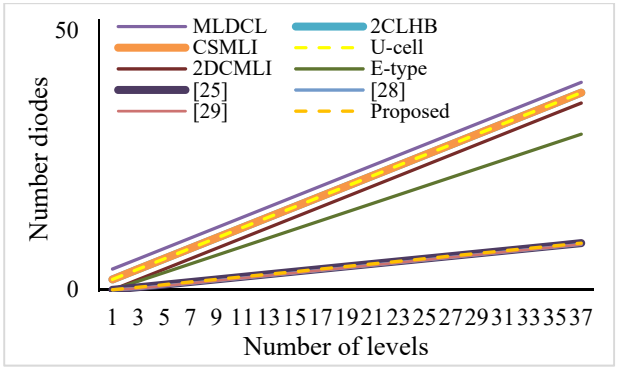


Figure 4. DC sources, switches, diodes & capacitor ratio comparison for other 15-level inverters with proposed 15-level inverter

The comparison between the number of dc sources, switches, diodes, and capacitors required for various topologies cited in this thesis with the proposed topology is shown in figure 3. This distinction demonstrates that the suggested topology uses fewer devices in its design. Different components required are presented in Figure 4. Here the N_{dc}/N and N_s/N are very smaller compared to the other topologies given in the literature. Figure 5 shows the comparison between the number of switches, diodes, and dc sources necessary for the proposed inverter with other topologies.



(a)



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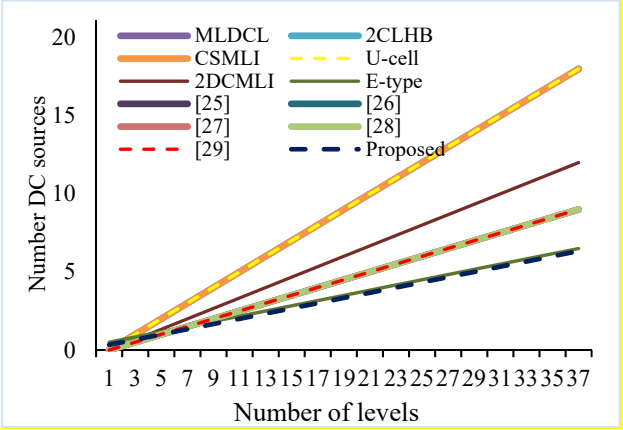


(c)

Figure 5. Comparison between the design components of various MLIs

4. SELECTIVE HARMONIC ELIMINATION PWM

Selective Harmonic Elimination PWM (SHEPWM) control is one of the best PWM control methods for multilevel converters. Generally, the waveform of multilevel inverter output is expressed using Fourier series expansion. The generalized expression for Fourier series expansion is given in equation (1).

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \tag{1}$$

Here, V_n= n^{th} harmonic voltage magnitude. Due to the odd symmetry of the quarter-wave, the even-order harmonics become zero. Therefore the expression for V_n becomes,

$$V_n = \begin{cases} \frac{4V_{dc}}{n\pi}\sum_{i=1}^{k}\cos(n\alpha_i); \textit{for odd values of 'n'} \\ 0; \textit{for even values of 'n'} \end{cases} \tag{2}$$

Where α_i is the switching angles of i^{th} harmonic and is between 0°-90° (i.e. $0 < \alpha_i < \frac{\pi}{2}$).

SHEPWM aims to suppress lower-order harmonics, whereas harmonic filters remove the remaining harmonics. This research developed a 15-level asymmetric inverter with a fundamental switching frequency control scheme to conceal the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonic voltages. The application of 15-level output will reduce the size of the harmonic filters as the prominent harmonics from the 5^{th} to 19^{th} harmonics are controlled. By expanding equation (2) for odd values of 'n', equation (3) can be obtained.

$$\left.\begin{aligned} \frac{4V_{dc}}{\pi}[\cos\alpha_1 + \cos\alpha_2 + \cdots \ldots + \cos\alpha_7] &= V_1 \\ \frac{4V_{dc}}{5\pi}[\cos5\alpha_1 + \cos5\alpha_2 + \cdots \ldots + \cos5\alpha_7] &= V_5 \\ \frac{4V_{dc}}{7\pi}[\cos7\alpha_1 + \cos7\alpha_2 + \cdots \ldots + \cos7\alpha_7] &= V_7 \\ \frac{4V_{dc}}{11\pi}[\cos11\alpha_1 + \cos11\alpha_2 + \cdots \ldots + \cos11\alpha_7] &= V_{11} \\ \frac{4V_{dc}}{13\pi}[\cos13\alpha_1 + \cos13\alpha_2 + \cdots \ldots + \cos13\alpha_7] &= V_{13} \\ \frac{4V_{dc}}{17\pi}[\cos17\alpha_1 + \cos17\alpha_2 + \cdots \ldots + \cos17\alpha_7] &= V_{17} \\ \frac{4V_{dc}}{19\pi}[\cos19\alpha_1 + \cos19\alpha_2 + \cdots \ldots + \cos19\alpha_7] &= V_{19} \end{aligned}\right\} \tag{3}$$

Where, V_5, V_7, V_{11}, V_{13}, V_{17}, V_{19} are the harmonic voltages of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th} harmonics, respectively, which are required to suppress to reduce the THD of output voltage. Therefore, these are equated to zero, and the resulting equation can be represented in equation (5). The fundamental voltage component in equation (3) is equated to the modulation index corresponding PWM scheme, which can be written as:

$$M = \frac{V_1}{V_{1\max}} \tag{4}$$

Where, V_{1max} = Peak fundamental voltage, $V_{1\max} = \frac{4kV_{dc}}{\pi}$,

V_1 = Actual fundamental voltage, k = Degree of freedom = $(N-1)/2$, N = No of output voltage levels

By combining (3) and (4) the above conditions can be written as follows.

$$\left.\begin{aligned} \frac{4V_{dc}}{\pi}(\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4 + \cos\alpha_5 + \cos\alpha_6 + \cos\alpha_7) &= M \\ \frac{4V_{dc}}{5\pi}(\cos5\alpha_1 + \cos5\alpha_2 + \cos5\alpha_3 + \cos5\alpha_4 + \cos5\alpha_5 + \cos5\alpha_6 + \cos5\alpha_7) &= 0 \\ \frac{4V_{dc}}{7\pi}(\cos7\alpha_1 + \cos7\alpha_2 + \cos7\alpha_3 + \cos7\alpha_4 + \cos7\alpha_5 + \cos7\alpha_6 + \cos7\alpha_7) &= 0 \\ \frac{4V_{dc}}{11\pi}(\cos11\alpha_1 + \cos11\alpha_2 + \cos11\alpha_3 + \cos11\alpha_4 + \cos11\alpha_5 + \cos11\alpha_6 + \cos11\alpha_7) &= 0 \\ \frac{4V_{dc}}{13\pi}(\cos13\alpha_1 + \cos13\alpha_2 + \cos13\alpha_3 + \cos13\alpha_4 + \cos13\alpha_5 + \cos13\alpha_6 + \cos13\alpha_7) &= 0 \\ \frac{4V_{dc}}{17\pi}(\cos17\alpha_1 + \cos17\alpha_2 + \cos17\alpha_3 + \cos17\alpha_4 + \cos17\alpha_5 + \cos17\alpha_6 + \cos17\alpha_7) &= 0 \\ \frac{4V_{dc}}{19\pi}(\cos19\alpha_1 + \cos19\alpha_2 + \cos19\alpha_3 + \cos19\alpha_4 + \cos19\alpha_5 + \cos19\alpha_6 + \cos19\alpha_7) &= 0 \end{aligned}\right\} \tag{5}$$

The switching angles must not violate the constraints,

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \qquad (6)$$

The set of non-linear equations in (5) can be solved using constraint (6) to obtain the switching angles required for the fifteen-level inverter. These equations can be solved using a fundamental switching frequency control method and optimization methods to optimize the inverter's switching angles. Any optimization strategy requires developing an objective function related to the variables to be evaluated. The primary objectives are,

a. To obtain the value of the base voltage equivalent to any preset or expected value.
b. To suppress or reduce a few harmonics of lower order.

The inverter's switching angles influence the output harmonic voltages. The generalized harmonic voltage objective function (OF) consists of the following form to achieve the above objectives:

$$OF = \min_{\alpha_k}\left\{\left(100\times\left(\frac{V_1^* - V_1}{V_1^*}\right)^4\right) + \sum_{k=2}^{N}\frac{1}{h_k}\left(50\times\frac{V_{h_k}}{V_1}\right)^2\right\} \qquad (7)$$

To minimize the 5th, 7th, 11th, 13th, 17th, and 19th harmonics, the above objective function can be taken as:

$$OF = 100\times\left(\frac{V_1^* - V_1}{V_1^*}\right)^4 + \left(\frac{50}{V_1}\right)^2\times\left(\frac{V_5^2}{5}+\frac{V_7^2}{7}+\frac{V_{11}^2}{11}+\frac{V_{13}^2}{13}+\frac{V_{17}^2}{17}+\frac{V_{19}^2}{19}\right) \qquad (8)$$

Where,

V_{1d} = Desired fundamental voltage, V_1 = Actual fundamental voltage, V_5 = Harmonic voltage of 5th Harmonic, V_7 = Harmonic voltage of 7th harmonic, V_{11} = Harmonic voltage of 11th harmonic, V_{13} = Harmonic voltage of 13th harmonic, V_{17} = Harmonic voltage of 17th harmonic, V_{19} = Harmonic voltage of 19th harmonic.

The objective of this research is to minimize the above objective function to reduce THD. The transcendental equations (5), satisfying the constraint function (6) with objective function (8), can be solved by using the N-R method for minimum THD and optimal switching angles of the proposed multilevel inverter. The comparison between different switching control methods with the proposed SHEPWM control is given in table.3.

Table 3. Comparison between switching control methods with SHEPWM

Method of switching	SVPM	SVPWM	SHEPWM
Utilization of dc sources	0~0.866	0~1	0~1.12
Frequency of switching	Medium	High	Low
Complexity	Low	High	High
Implementation	Online	Online	Offline

5. IMPLEMENTATION OF NEWTON RAPHSON (N-R) METHOD

The seven switching angles for seven switches in the inverter are first computed by the numerical successive approximation technique known as Newton Raphson (N-R) approach. The computation of switching angles involves equations (5) with equation (6). The step-by-step procedure followed in the N-R method for the solution of non-linear equations is described below.

Step 1: For the calculation of switching angles, a matrix is formulated with seven (1-7) switching angles in equation (9)

$$\alpha^i = [\alpha^1, \alpha^2, \alpha^3, \alpha^4, \alpha^5, \alpha^6, \alpha^7]^T \qquad (9)$$

Step 2: The non-linear system matrix is formulated in equation (10), and the transpose matrix of its partial derivation concerning switching angles is given in equation (11)

$$F^i = \begin{bmatrix} \cos(\alpha_1^i)+\cos(\alpha_2^i)+\cos(\alpha_3^i)+\cos(\alpha_4^i)+\cos(\alpha_5^i)+\cos(\alpha_6^i)+\cos(\alpha_7^i) \\ \cos(5\alpha_1^i)+\cos(5\alpha_2^i)+\cos(5\alpha_3^i)+\cos(5\alpha_4^i)+\cos(5\alpha_5^i)+\cos(5\alpha_6^i)+\cos(5\alpha_7^i) \\ \cos(7\alpha_1^i)+\cos(7\alpha_2^i)+\cos(7\alpha_3^i)+\cos(7\alpha_4^i)+\cos(7\alpha_5^i)+\cos(7\alpha_6^i)+\cos(7\alpha_7^i) \\ \cos(11\alpha_1^i)+\cos(11\alpha_2^i)+\cos(11\alpha_3^i)+\cos(11\alpha_4^i)+\cos(11\alpha_5^i)+\cos(11\alpha_6^i)+\cos(11\alpha_7^i) \\ \cos(13\alpha_1^i)+\cos(13\alpha_2^i)+\cos(13\alpha_3^i)+\cos(13\alpha_4^i)+\cos(13\alpha_5^i)+\cos(13\alpha_6^i)+\cos(13\alpha_7^i) \\ \cos(17\alpha_1^i)+\cos(17\alpha_2^i)+\cos(17\alpha_3^i)+\cos(17\alpha_4^i)+\cos(17\alpha_5^i)+\cos(17\alpha_6^i)+\cos(17\alpha_7^i) \\ \cos(19\alpha_1^i)+\cos(19\alpha_2^i)+\cos(19\alpha_3^i)+\cos(19\alpha_4^i)+\cos(19\alpha_5^i)+\cos(19\alpha_6^i)+\cos(19\alpha_7^i) \end{bmatrix} \qquad (10)$$

$$\left[\frac{\partial F^i}{\partial \alpha}\right]^T = \begin{bmatrix} -sin(\alpha_1^i)-sin(5\alpha_1^i)-sin(7\alpha_1^i)-sin(11\alpha_1^i)-sin(13\alpha_1^i)-sin(17\alpha_1^i)-sin(19\alpha_1^i) \\ -sin(\alpha_2^i)-sin(5\alpha_2^i)-sin(7\alpha_2^i)-sin(11\alpha_2^i)-sin(13\alpha_2^i)-sin(17\alpha_2^i)-sin(19\alpha_2^i) \\ -sin(\alpha_3^i)-sin(5\alpha_3^i)-sin(7\alpha_3^i)-sin(11\alpha_3^i)-sin(13\alpha_3^i)-sin(17\alpha_3^i)-sin(19\alpha_3^i) \\ -sin(\alpha_4^i)-sin(5\alpha_4^i)-sin(7\alpha_4^i)-sin(11\alpha_4^i)-sin(13\alpha_4^i)-sin(17\alpha_4^i)-sin(19\alpha_4^i) \\ -sin(\alpha_5^i)-sin(5\alpha_5^i)-sin(7\alpha_5^i)-sin(11\alpha_5^i)-sin(13\alpha_5^i)-sin(17\alpha_5^i)-sin(19\alpha_5^i) \\ -sin(\alpha_6^i)-sin(5\alpha_6^i)-sin(7\alpha_6^i)-sin(11\alpha_6^i)-sin(13\alpha_6^i)-sin(17\alpha_6^i)-sin(19\alpha_6^i) \\ -sin(\alpha_7^i)-sin(5\alpha_7^i)-sin(7\alpha_7^i)-sin(11\alpha_7^i)-sin(13\alpha_7^i)-sin(17\alpha_7^i)-sin(19\alpha_7^i) \end{bmatrix} \qquad (11)$$

Step 3: Formulation of harmonic magnitude matrix and represented in equation (12)

$$T = \left[\frac{\pi M_i}{4}, 0, 0, 0, 0, 0, 0\right]^T \qquad (12)$$

Equations (5) and (12) are modified and rewritten as equation (13)

$$F(\alpha) = T \qquad (13)$$

The matrices (9) to (13) are simulated in MATLAB software for the programmed N-R method, which is implemented

described in the following steps.

Step 1: Predict the initial switching angles using the equal area criterion with the equation (14)

$$\alpha^0 = [\alpha_1^0, \alpha_2^0, \alpha_3^0, \alpha_4^0, \alpha_5^0, \alpha_6^0, \alpha_7^0] \quad (14)$$

Step 2: This step involves the design equations of the N-R approach from equations (15) to (18)

$$F(\alpha^0) = F^0 \quad (15)$$

The equation (13) is linearized to get the α^0

$$F^0 + \left[\frac{\partial F}{\partial \alpha}\right]^0 d\alpha^0 = T \quad (16)$$

And,

$$d\alpha^0 = [d\alpha_1^0, d\alpha_2^0, d\alpha_3^0, d\alpha_4^0, d\alpha_5^0, d\alpha_6^0, d\alpha_7^0] \quad (17)$$

Equation (17) can be solved using the inverse of the equation represented in equation (18).

$$d\alpha^0 = INV\left[\frac{\partial F}{\partial \alpha}\right]^0 (T - F^0) \quad (18)$$

Step 3: Update the initial values using the equation (19)

$$\alpha^{i+1} = \alpha^i + d\alpha^i \quad (19)$$

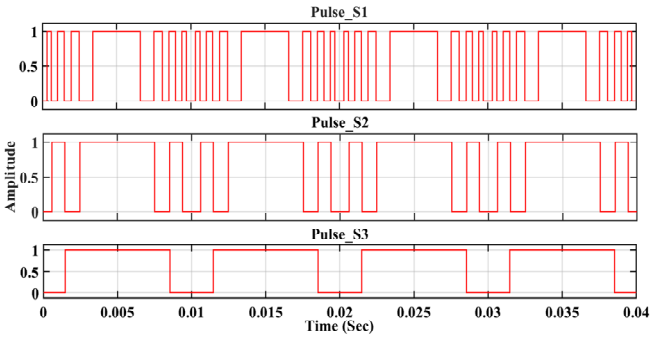
Step 2 & 3 are repeated till the $d\alpha^i$ is satisfied for the degree of accuracy and to satisfy the constraint, $\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}$. Thus the switching angles α_1 to α_7 be evaluated using the Newton Raphson approach, and the same is stored in the look-up tables for different modulation indexes. These switching angles are retrieved from the memory of look-up tables during the real-time operation of the inverter for the required modulation index.

6. RESULTS & DISCUSSIONS

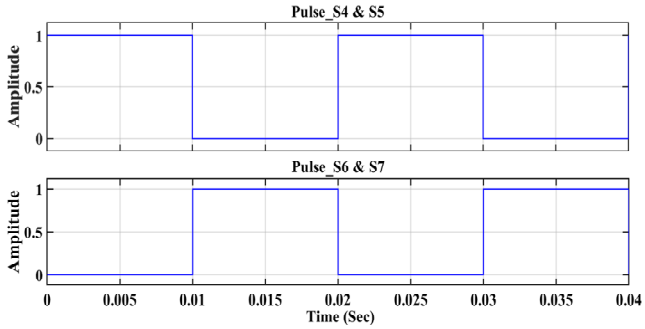
The proposed asymmetric inverter is implemented on MATLAB Simulink using seven IGBT switches, three switched diodes, and three dc sources. To generate the switching pulses, a selective harmonic elimination pulse width modulation has been used. The switching frequency is 50Hz, the maximum harmonic frequency is 1 kHz, and the Nyquist frequency for THD is 5 kHz. The inverter's load is modeled as a non-resistive load with R = 26.83 Ω and L = 9.9 mH. The switching angles are evaluated using SHEPWM at 0.9 modulation index. The proposed inverter can operate at different levels with the choice of dc sources as described below.

6.1 Equal magnitude of dc sources

Considering the input dc sources of the proposed inverter shown in Figure 2 as the ratio of 1:1:1, i.e. all the dc sources with equal magnitude, a seven-level output voltage is produced at the inverter output. Here the magnitude of dc sources is taken as V_1 = 37V, V_2 = 37V, and V_3 = 37V to get a peak voltage of 111V. The switching pulses of the seven-level operation of the proposed inverter are shown in Figure 6. Figure 7 shows the 7-level output voltage waveform of the proposed inverter with an equal magnitude of dc sources, and Figure 8 shows the corresponding THD of the 7-level output of the proposed inverter, which is 15.36%.



(a)



(b)

Figure 6. Switching pulses of proposed inverter for seven-level operation. (a) Primary circuit (b) Auxiliary circuit

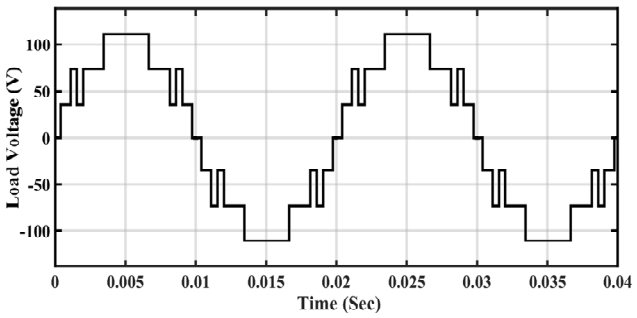


Figure 7. The 7-Level output voltage of the asymmetric inverter

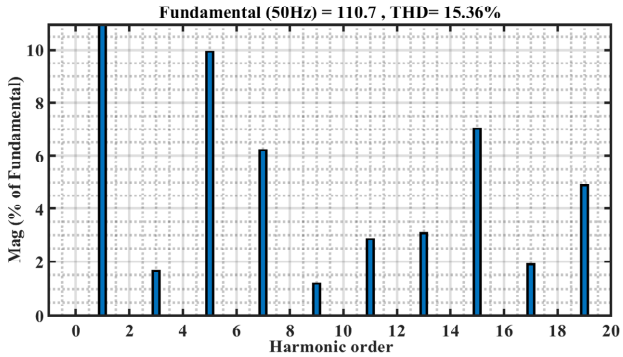
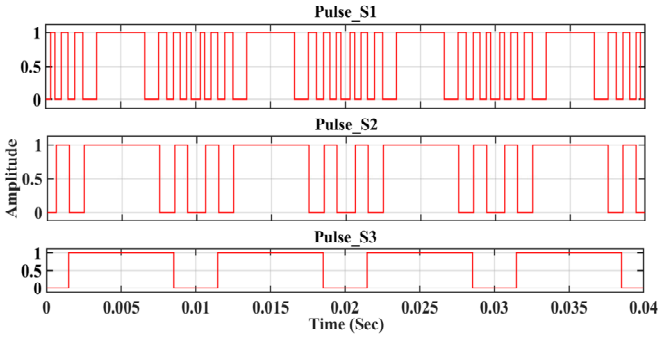


Figure 8. THD of output voltage for 7-level operation

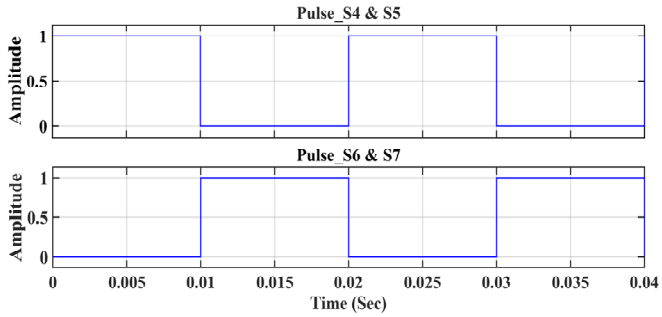
6.2 Unequal magnitude of dc sources

Considering the input dc sources of the proposed inverter shown in Figure 2 as the ratio of 1:2:2, i.e. the dc sources with unequal magnitude, an eleven-level output voltage is produced at the inverter output. Here the magnitude of dc sources is taken as V_1 = 37V, V_2 = 74V, and V_3 = 74V to get a peak voltage of 185V. The switching pulses of eleven level operation of the proposed inverter are shown in Figure 9. Figure 10 shows the

11-level output voltage waveform of the proposed inverter with an unequal magnitude of dc sources. Figure 11 shows the corresponding THD of the 11-level output of the proposed inverter, which is 11.17%.



(a)



(b)

Figure 9. Switching pulses of proposed inverter for eleven level operation. (a) Primary circuits (b) Auxiliary circuit

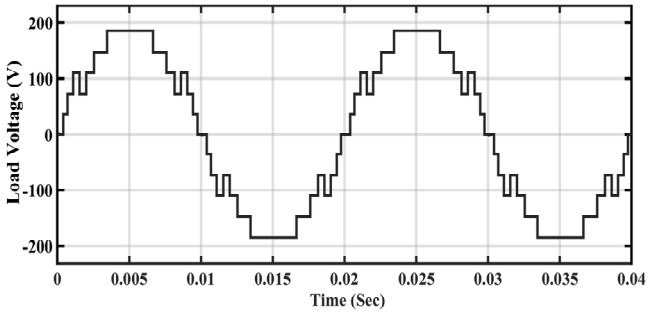


Figure 10. The 11-level output voltage of the asymmetric inverter

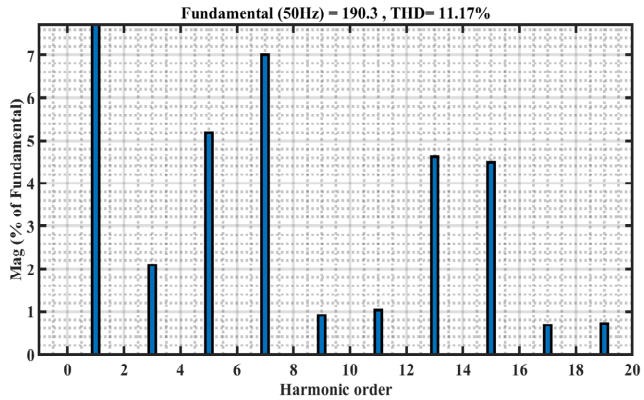
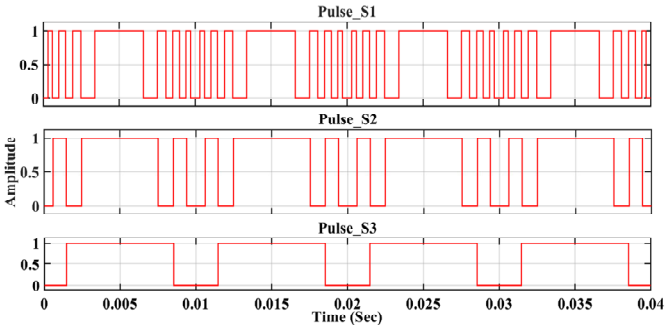


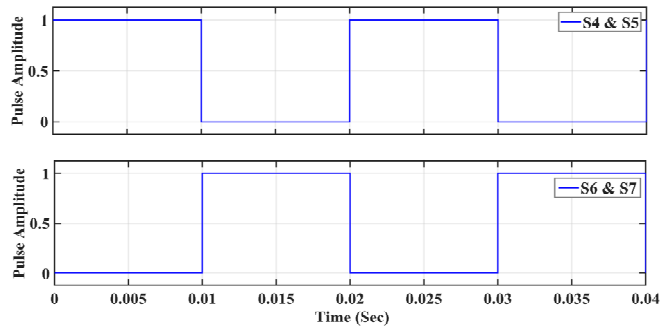
Figure 11. THD of output voltage for 11-level operation

6.3 Binary approach of DC sources

Considering the input dc sources of the proposed inverter shown in Figure 2 as the ratio of 1:2:4, i.e. the dc source magnitudes are different from one to another, a fifteen-level output voltage is produced at the inverter output. Here the magnitude of dc sources is taken as V_1 = 37V, V_2 = 74V, and V_3 = 148V to get a peak voltage of 259V. The switching pulses corresponding to the generated switching angles are shown in Figure 12(a) for the primary circuit and Figure 12(b) for an auxiliary circuit. Figure 13 shows the 15-level output voltage waveform of the proposed inverter with the binary approach of dc sources (1:2:4 ratio) Figure 14 shows the load current waveform for 15-level operation, and Figure 15 shows the corresponding THD of the 15-level output of the proposed inverter, which is 7.3%. Figure 14 confirms that the output current waveform approximately resembles the sinusoidal waveform without using any filter at the output of the inverter. Also, it is in phase with the load voltage so that the power factor is maintained approximately unity.



(a)



(b)

Figure 12. Switching pulses of proposed inverter for 15-level operation. (a) Primary circuits (b) Auxiliary circuit

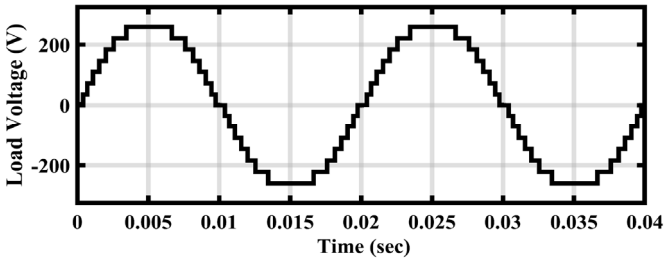


Figure 13. The 15-level output voltage of the asymmetric inverter

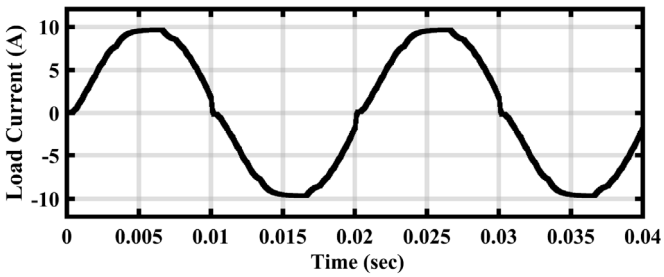


Figure 14. The 15-level output current of asymmetric inverter

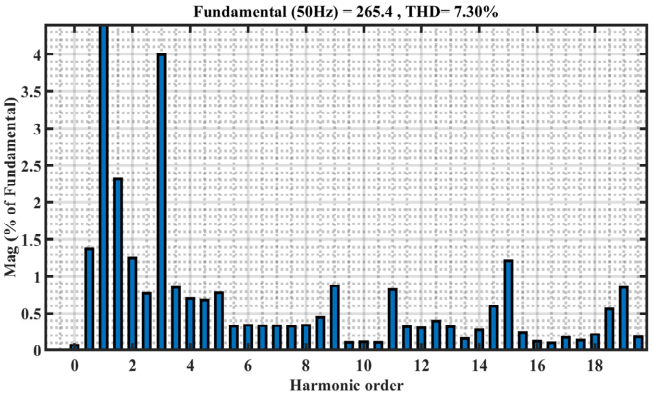


Figure 15. THD of the output voltage of the proposed inverter for 15-level operation

The detailed comparison of the results of the proposed inverter was compared with the work presented in the literature. Table.4 reveals that the proposed asymmetric inverter utilizes less number of switches compared to the other topologies and also produces less % THD without employing any filter at the output.

The peak value of output voltage is 259V, and the peak value of current is 9.65A for the figures shown in 13 and 14 respectively. To get the RMS values of output voltage and current, the peak values are divided by $\sqrt{2}$. Thus, the RMS value of the output voltage is 183.16 V, and the RMS value of the output current is 6.83A.

Therefore the output power of the 15-level inverter is determined by taking the product of RMS values of output voltage and current.

$$P_0 = V_{RMS} * I_{RMS}$$
$$= 183.16 * 6.83$$
$$= 1250 \text{ W}$$

Thus the output of the proposed 15-level inverter is computed as 1250W.

Table 4. THD comparisons of the proposed inverter with literature work

Author	Type of Inverter	No of Sources	No of Switches	No of Levels	Max. O/p Voltage	%THD
Jagdish Kumar (2008)	Symmetric CHB	5	20	11	$5V_{dc}$	7.9%
Aman Parkash (2014)	Symmetric H-Bridge	3	12	7	$3V_{dc}$	11.68%
	Symmetric CHB inverter	4	16	9	$4V_{dc}$	19.3%
Faouzi ARMI (2016)	Symmetric CHB inverter	3	12	7	$3V_{dc}$	25.91%
	Asymmetric CHB inverter	3	12	9	$4V_{dc}$	10.2%
Wahidah Abd Halim (2017)	Symmetric CHB inverter	3	12	7	$3V_{dc}$	11.9%
	Asymmetric CHB inverter	4	16	9	$4V_{dc}$	8.4%
Proposed	Asymmetric modular Multilevel inverter	3	7	7	$3V_{dc}$	15.36%
		3	7	11	$5V_{dc}$	11.17%
		3	7	15	$7V_{dc}$	7.30%

6.4 Application of Proposed Inverter on Grid-connected PV System

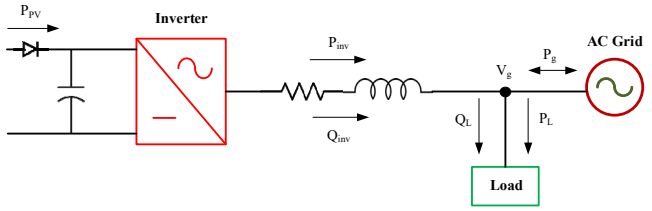


Figure 16. Power flow diagram for single-phase grid-connected SPV system

Single-phase SPV systems are generally implemented for low-power applications of the range of a few kilowatts with maximum power point tracking at unity power factor [27]. The SPV system pumps the power into the grid when the output power exceeds the load demand. The active power flow in the grid-connected SPV system depends on the power generated by the SPV system or the power demand of the grid. Figure 16 shows the power flow diagram between the SPV system and grid when the unity power factor is required at the grid side for low and medium power applications.

Asymmetric PV sources feed the input dc supply of the proposed inverter. The current into the grid is injected by using an adaptive PI controller. The nature of the current injected to be sinusoidal and in phase with the grid voltage to maintain the

unity power factor. To produce a sinusoidal grid current, the dc voltages provided by the PV array must be kept constant at all times.

There are two different control strategies used for voltage control for injecting the current into the grid. One can control the total dc voltage of the proposed inverter, while the other control the dc voltage of specific dc sources supplied by the PV array. Because asymmetrical PV inputs are connected to the inverter through dc links, individual dc-dc boost converters with MPPT controllers are constructed for each PV source in the proposed configuration. Under various operating situations, these independent MPPT controllers keep the dc-link voltages in the 1: 2: 4 ratio. To produce the reference PV voltages such as V_{dc1}, V_{dc2}, and V_{dc3} a P&O-based MPPT algorithm is used. The Simulation model diagram is given in Figure 17 for the grid-connected PV-based proposed inverter.

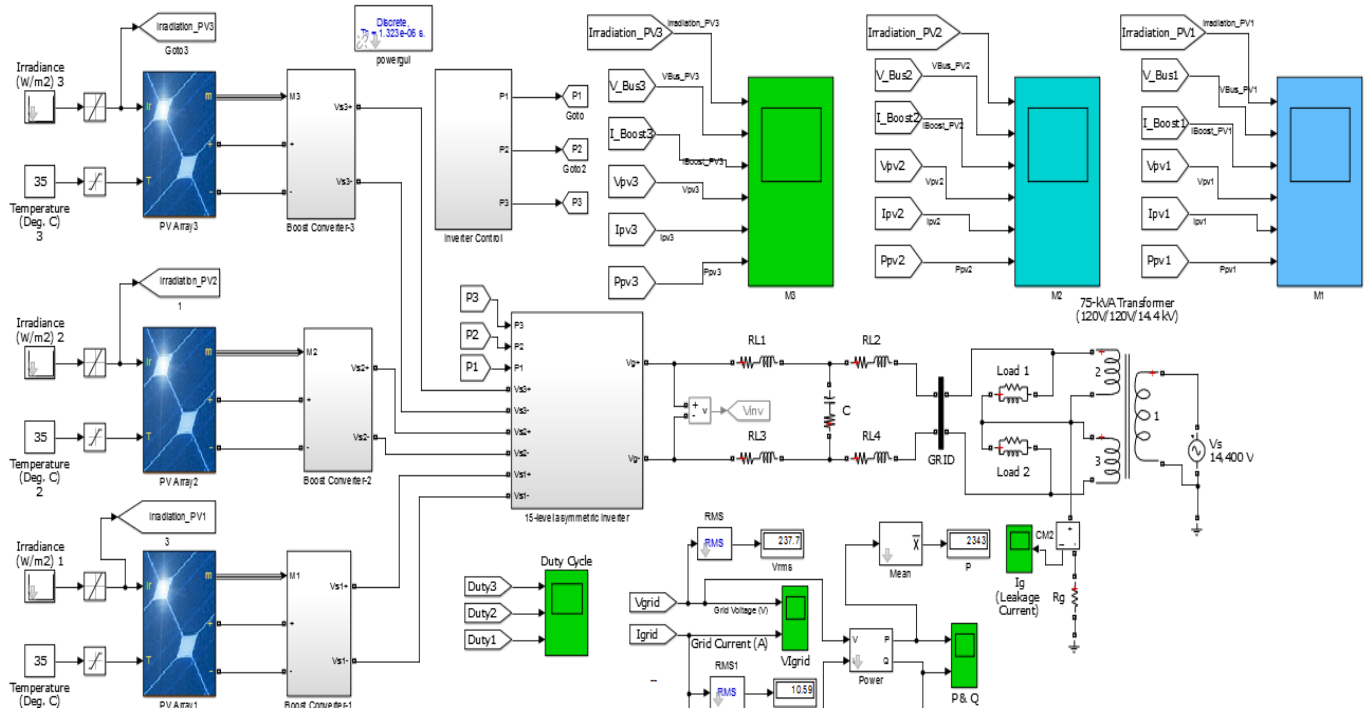


Figure 17. Single-phase grid-connected SPV system with the Proposed Asymmetric Inverter

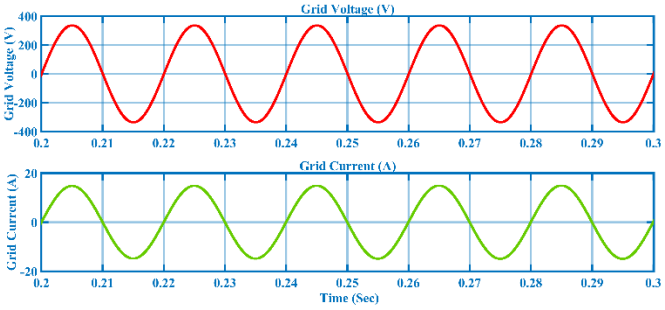


Figure 18. Grid Voltage and Grid current waveforms

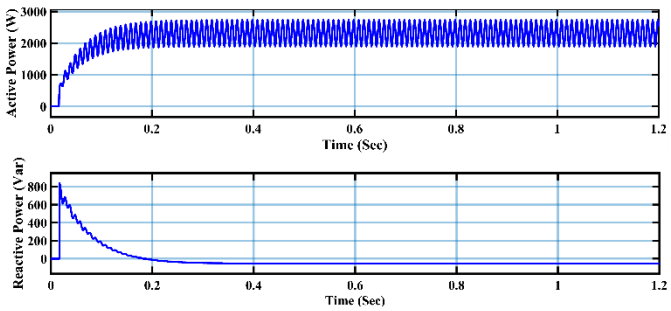


Figure 19. Active & Reactive power delivered by the inverter to the grid

While connecting the proposed asymmetric inverter to the single-phase grid-connected PV system, three different PV sources were considered as shown in Figure 17. The grid voltage and grid current waveforms for the same are given in Figure 18. Also, Figure 19 presents the Active and Reactive power output of the grid-connected PV system with the proposed inverter. Further, the THDs of grid voltage and currents were measured and is given in Figure 20 and Figure 21 respectively.

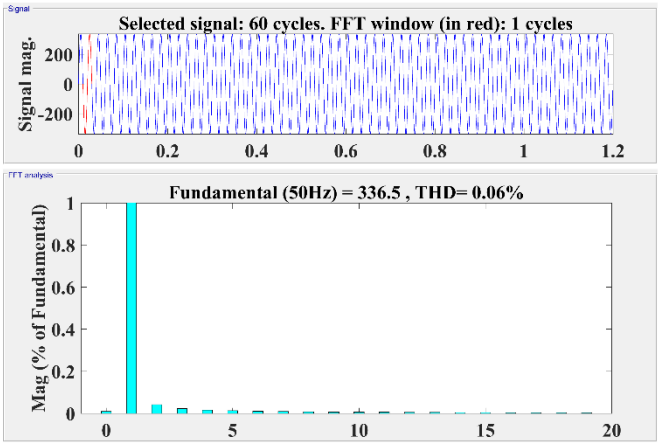


Figure 20. THD of the Grid voltage waveform

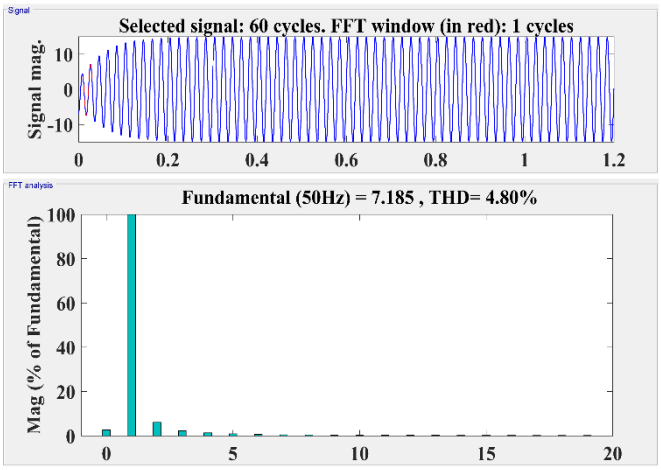


Figure 21. THD of the Grid current waveform

From Figure 20 and Figure 21, it is observed that the THD of the grid voltage is 0.06% and he THD of the grid current is 4.8% respectively, which is less than 5% and highly acceptable according to IEEE519 standards.

7. CONCLUSIONS

An asymmetric 15-level inverter with 7-switches, 3-diodes had been developed in this paper to optimize the size of the design topology. The inverter also operated 7-level and 11-level operation with a proper choice of dc source selection. The lower order dominant harmonics in the inverter output had been minimized using a low-frequency switching modulation (SHEPWM). The transcendental equations generated in SHEPWM had been solved using the Newton Raphson method to obtain the switching angles. The THD of the inverter output had been analyzed for 7-level, 11-level and 15-level operations using equal magnitude, un-equal magnitude and binary approaches of dc sources respectively. The fifteen-level operation had given a minimum of 7.3%, compared to other levels of operation without using filter at the inverter output. Also the proposed inverter is integrated to grid connected solar photovoltaic system, which given the grid voltage is 0.06% and he THD of the grid current is 4.8% respectively which is acceptable according to IEEE519 standard.

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