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Pixel Optimization Using Iterative Pixel Compression Algorithm for Complementary Metal Oxide Semiconductor Image Sensors

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ABSTRACT

The research presents a unique approach to the iterative pixel compression method for pixel optimization by reducing noise with a motion-guided backdrop. Image resolution and precision are increased by using a complementary metal oxide semiconductor (CMOS) image sensor. Researchers offer a dispersed equivalent implementation of the Iterative Pixel Compression technique for CMOS image sensors in order to successfully handle the expanded data. The current frame is handled by the buffer circuit in the CMOS image sensor. The registered bank is related to subsequent frames. It consists of a collection of registers that retain information on the grey levels of the acquired pictures' pixels. The image DE noising signal process is applied to the input picture, which contains noise. The pixel averaging filter is used in image DE noising to enhance picture quality and produce a better estimate. Pixel ordering identifies misplaced areas of photos due to the use of an iterative pixel reduction method. It allocates the best existing pixel feasible. Peak signal-to-noise ratio (PSNR) assess the image's quality through and Mean Square Error (MSE). When compared to previous approaches, our results demonstrate a 2% improvement in PSNR and a 1% reduction in MSE.

1. INTRODUCTION

Computerized photographical process includes a lot of computations to overcome the drawbacks of the conventional film camera [1]. The computational technique encompasses the method of changing of the image parameters while capturing for refined reconstruction with indirect measurement. The realistic guide in the process of image capturing and manipulating methods is to generate compelling pictures using computer graphics, but also to extract scene properties from computer vision along with various illustrations [2].

Photographers are not accustomed to new algorithms for taking high dynamic range pictures. The researchers can study about the image processing and how the images have been captured through the noise issues. The novel capturing technique includes a sophisticated sensor, electromechanical actuator, and onboard process [3]. Capturing multiple images with different device attributes and altering the flash enlightenment attributes is one of the innovative modernization techniques that are developed [4]. As the CMOS image sensors offer better features, it has been most widely used than (charge coupled device) CCD based image sensors.

A complementary metal oxide semiconductor (CMOS) sensor is an IC with an array of pixel sensors. It consists of four major parts, namely, color filter, digital controller, pixel array, and the analog-to digital converter as depicted in Figure 1.

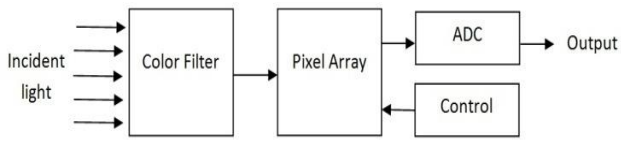

Figure 1. CMOS image sensor

Micro lenses channel the light onto the photosensitive part of each pixel. The photon passes through a color filter array. This color filter captures the color information. Separate measurements of R, G, and B are enabled by the color filter [5]. It filters out the unwanted colors and allows specific colors to a pixel array. Every pixel sensor converts the incoming light's sensitivity into voltage. The voltage signal is then fed to the analog to digital converter to convert into the digital signal.

Salt and pepper noise is generated by the errors during the analog to digital conversion process [6]. This salt and pepper noise can be reduced by using pixel-averaging filter and the pixels are optimized by an iterative pixel compression algorithm. The image is applied for filtering in order to

minimize noise and for extracting structural information. The images are found to be spatially invariant or may be variant kernels [7]. Spatially invariant kernel enables effective filtering processing [8].

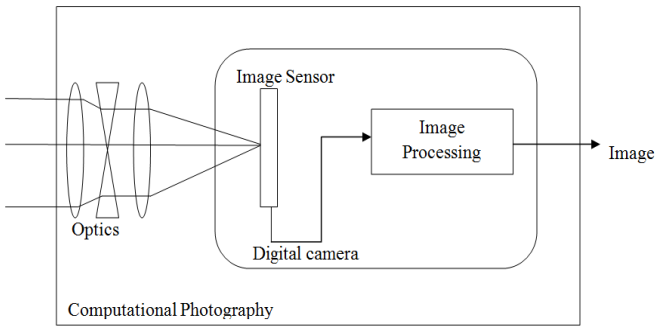

Figure 2. Computational photography

The Filtering of images uses guidance signals. The method of guided or collaborative image filtering is utilized in a number of computational photography and computer vision techniques. The data depending the framework does not view the structural differences in the guidance and input picture. Figure 2 represents the Computational Photography framework.

2. LITERATURE SURVEY

Zhang et al. [9] proposed three approaches to optimize pixels. The result of the optical characteristics of 1.05-µm pixel post optimization is as good as that of the 1.75-µm pixel. Harold Christopher Burger offered a method for DE noising astronomical images [10]. He treated each pixel of a camera sensor independently so that the faint stars and nebula are sealed. The author provided a gentle introduction to coded photography. He used Principal Component Analysis technique and produced a reasonably better quality fused deburred image [11]. Rithe [12] demonstrated a scalable reconfigurable bilateral filtering processor on a chip. The 40-nm CMOS chip processing 13 megapixels achieved significant energy reduction.

Steve Mann proposed a method for generating volumetric 3D sculptures called Topo sculpting. In order to eliminate shape and form from a moving object, depth cameras were utilized [13]. Wave front coding and lattice focal lens imaging are two methods used to increase the depth of field of an imaging system, and David Stoker compared their results [14]. At a rate of 2lp/mm, the field depth was successfully increased. Performance across a certain frequency is crucial for recognition applications. The authors presented an approach of designing an n-in-n ATLAS pixel sensor. A new configuration was proposed to optimize its layout parameters [15].

Venter and Sinha [16] proposed 4-T pixel structure to reduce the fixed pattern noise. Jung et al. [17] optimized an FFS pixel structure for the application of nLC to higher resolution mobile phone displays. Electro optical characteristics were improved by varying the structure of the pixel from VOT structure to POT structure. Jinping Gu proposed a distributed parallel optimization of the PPI algorithm [18]. Ashwani Kumar analyzed a hybrid CMOS OxRAM pixel circuit [19]. The dynamic array of the pixel was improved by a factor of nearly two and half. Luo [20] presented a CMOS design which geared up the binary temporal optical encoding. The pixel occupied an area roughly 10.5µm X 10.5µm with a fill factor 42%.

Toshiki [21] suggested a CMOS-based image sensor and showed how to use it to achieve high-speed images without rolling shutter effects. The architecture of a digital pixel sensor was modelled at the system level by Radpour and Sayedi [22]. An illuminating light's energy can be captured by it. He has demonstrated that there is good agreement between the experimental findings of photodiodes and the system level model of the manufactured photodiodes (0.18 m CMOS standard technology).

According to Boukhayma's [23] proof, a full VGA APS can produce deep subelectron noise. Francisco Calderon proposed a Modular Robot to satisfy the diversity of image perception tasks [24]. It was capable of solving the problems of search, rescue, land mine detection, unexploded ordnance detection, and exploration. Sara Marconi designed a bigger pixel readout chip. He has achieved optimized power results, reduced switching activity, optimized area, and power. Holography and photography have approximately similar noise performance, as demonstrated by Marks et al. [25].

The projected optimization of kidney image based on Sparse Deep Neural Network. For easy identification, the kidney abnormality classification in the image was shown in colour. It provided a heuristic method to optimize the design of a pixel antenna. It condensed the load by over 65 % and achieved a broader coverage of bandwidth. Cecilia Aguerrebere suggested using hyperprior to model the image patches in order to stabilise the estimation process [26]. His findings indicate that, for a variety of image restoration issues, HBE outperforms a number of cutting-edge restoration techniques. Bumsub Ham introduced a joint filtering framework that was widely applicable to computational photography and computer vision tasks. This model did't have a closed form solution.

Berzins et al. [27] demonstrated sub-micrometer dielectric nanostructure. It was based on RGB filters by means of high angle tolerance. He has achieved the reduced filter size, which is less than 0.55 µm by improving fabrication techniques. Xie and Theuwissen [28] proposed a variety of on-chip smart temperature sensors. It intends to thermal recompense of CMOS image sensors' dark current. According to the experimental findings, the MOS-based temperature sensors used 36 and 40 W of power, respectively [29]. Using four different chips, both managed to reach 3-sigma () errors of less than 0.75°C. The conversion time is 16 ms, and the temperature ranges from -20°C to 80°C. According to the experimental findings, the MOS-based temperature sensors used 36 and 40 W of power, respectively. Using four different chips, both managed to reach 3-sigma () errors of less than 0.75°C. The conversion time is 16 ms, and the temperature ranges from -20°C to 80°C.

Keiichiro Kagawa proposed a dual mode 303 times compressive computational using a CMOS image sensor [30]. Image sensor is able to operate in dual modes. To increases the compression ratio and reduce the image reproduction time, Deep Neural Network can be used for further development.

Horio et al. [31] suggested multi-path interference in a compressive TOF when combined with a multi-tap macro-pixel CMOS image sensor in order to compare and enhance the absolute magnitude of the mean error in a single path scenario.

3. PROPOSED METHODOLOGY

The following Figure 3 shows the block diagram of our iterative pixel compression algorithm. It gives improved accuracy than other algorithms. It consists of a buffer circuit, register bank, and pixel averaging filter. Successive frames are associated with the register bank. Pixel averaging filter is used to find the phase of the image DE noising [32]. The input image, which consists of noise, is applied to the image DE noising process. Subsequently, pixel averaging filter technique is applied to get better image quality and estimation of an image.

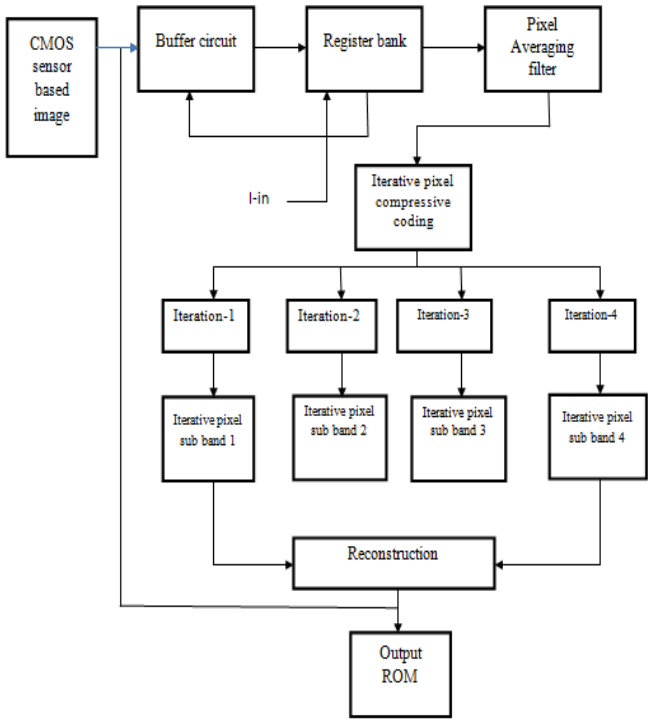

Figure 3. Block diagram of the proposed iterative pixel compression algorithm

The design process is as follows here. It is constructed in Simulink and the building blocks are taken from XSG (Xilinx system generator). It is simulated for ensuring the conformity of the algorithm. XSG Building blocks are behavior oriented. It allows quick simulations. They are also capable of combining with the usual Simulink blockers for constructing the entire design.

Place the entire system fMAX and latency between the high level Simulink design descriptions. XSG analyses the description of Simulink. It develops both the HDL coding and the optional bit stream of targeted FPGA devices. By default, it sums in the pipeline registers as well as the needed amount of time division multiplexing for satisfying the design specifications.

3.1 De-noising using pixel averaging filter

Because of the coherent processing of the backscattered signal, the image is meant by spatial noise. These spatial noises degrade the quality of the unprocessed images. During relentless weather circumstances, the images will be with noises like salt & pepper noise. It may be due to the visibility of scattered light. Therefore, DE noising becomes essential to remove the noise. To enhance the image quality, a pixel averaging filtering technique is used here.

The edge of the image with the least contrast is selected using the pixel averaging filter, which is composed of the average generator module. The average filter is constructed with 18 |ADD|, eight shifter components and one multiplier. Mean of the luminance calculations of a pixel that prepares the minute directional distinction Dmin is achieved using conventional generators, as given in Figure 4. pi, j-1, pi, j+1, pi+1, j-1; pi+1, j and pi+1, j+1 are absolutely implicit to be the best possible pixels. The final Multiplexer output (a+bx2+c)/4. Then the multiplexer outputs the value of the mean of the pixels that prepares Dmin. Certain directional contrast was determined by four-pixel value and hence it's reconstructive value of four pixels. The two-level adder and shifter blocks are used to cease the estimation.

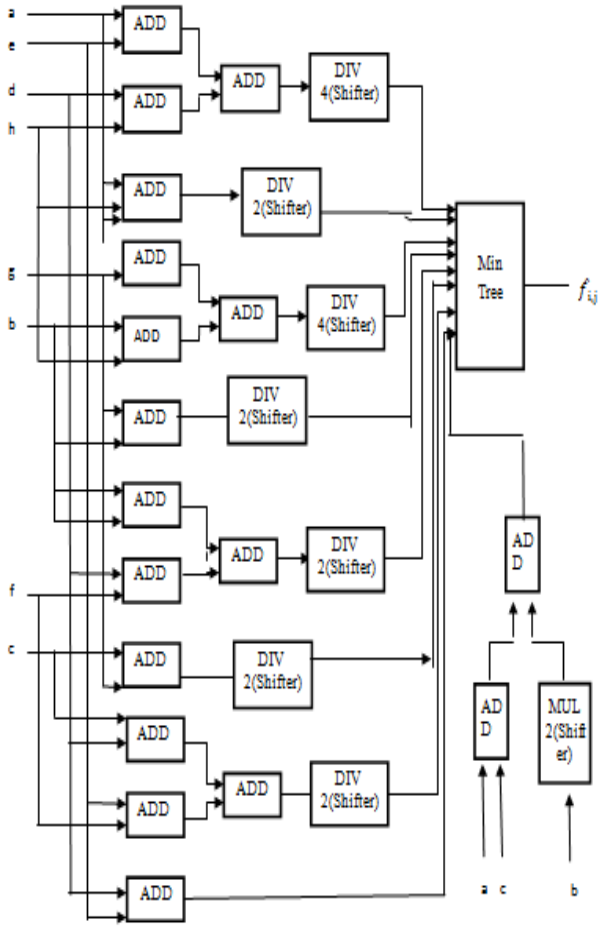

Figure 4. Architecture diagram of an average generator

Pertaining to the usage of chips, the silicon region of a multiplier is bigger compared to a shifter. Here, the shifter unit for bringing down the equipment costs can replace the entire multipliers. Post estimation, the next iteration of input pixels are b, d, e, and g altogether processed.

The recalculated value $\hat{f}_{i,j}$ acquired from the pixel averaging filter shall be given in Eq. (1).

$$\bar{f}_{i,j} = \begin{cases} SortFour2, & if\left(SortFour2 > \bar{f}_{i,j}\right) \\ SortFour3, & if\left(SortFour3 < \bar{f}_{i,j}\right) \\ \bar{f}_{i,j}, & Otherwise. \end{cases} \quad (1)$$

3.2 IPC imaging scheme

The technique proposed is based on the coding of Iterative Pixel Compression. The spatial idleness shall be eliminated by Discrete Wavelet transform- based decomposition. Wavelet Transforms are becoming significant techniques for image compressing as it provides an extensive enhancement in the quality of the picture at a high compression ratio using energy compaction properties.

It divides an image to a set of functions called wavelets from a unit prototype wavelet that is named as mother wavelet by dilation along with shifting. Later, the transform coefficient is calculated individually for various segments of time domain signals at several frequencies. At the time of DWT process, every filter is used flatly on every row of images, trailed by the vertical applications for every column of prior images that were filtered. After the first level decomposition, four subbands are found to be developed. For the first level of the original image (K=1), the 2D wavelet transform is used. Here stands for the Gaussian estimation of averaging filter's standard deviation. The mean and variance of the noise distribution for the majority of pixels will be equal. These metrics need to be taken into consideration:

Wmin=minimum gray value in Txy
Wflex=average gray value in Txy
Wmax=maximum gray value in Wxy
WXY=gray level at the coordinates (x,y)
Tmax=maximum possible size of Txy

Procedure of our proposed scheme

Step 1: Starting iteration

Step 2: Stage A: If W(min)<Wmed<Wmax, and then Wmed is not a correlated impulse

Step 3: Goto stage B and check if Wxy is the correlate impulse

Step 4: Ensure whether Wmed is a correlated impulse. If so, scale of the window is increased. Stage A is recurrent until (a) Wmed is not correlate with impulse, then move to stage B or (b) If Tmax is reached, then the output is Wxy

Step 5: Stage B: If Wmin<Wxy<Wmax, then Wxy is't-correlated impulse. The output will be Wxy (reduced distortion)

Step 6: Check either Wxy= Wmin or Wxy= Wmax. Output will be Wmed. Wmed is't correlated impulse (from stage A)

Step 7: Exit

The following Figure 5 shows the hardware structure of the IPC imaging with the help of using Xilinx XSG with MATLAB.

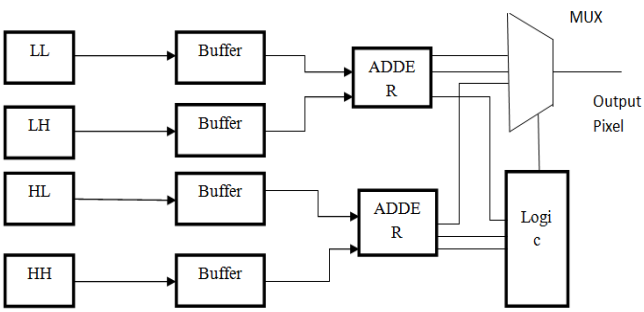

Figure 5. Hardware structure of the IPC algorithm

A hardware design with parallel operations and histogram estimation is made possible by the improvement of the IPC algorithm. The following can be used to represent the histogram estimation's mean: Assume mean of the histogram can be obtained from Eq. (2).

$$\mu = \frac{1}{2N}\sum_{i} i.hs(i) \tag{2}$$

where, $hs(i)$ refers to the sum of the histogram in a rectangular grid. Which means that the count (i) gray level is found from the summation image over the domain D. Hence, $i.hs(i)$ is substituted in Eq. (2) by "i" adding $hs(i)$ as shown in Eq. (3):

$$\mu = \frac{1}{2N}\sum_{i}\sum_{m=1}^{hs(i)} i \tag{3}$$

Eq. (3). can be rewritten by replacing the summations and replacing "i" by (K, l) is possible in Eq. (4).

$$\mu = \frac{1}{2N}\sum_{k\in D}\sum_{k\in D} I_S(k,l) \tag{4}$$

In all cases, most assurance notices the alteration to all spatial areas in "D" permitting for finding the value of the mean component in the histogram that utilizes the supplementary memory.

3.3 Results and discussions

The proposed IPC algorithm has been accomplished on Vertex 2 Pro FPGA using VHDL & Matlab. Our proposed method is implemented and evaluated using parameters. Datasets are valued in natural and raw images by taking hundreds of images that are processed using Matlab and Xilinx XSG with the support of HDL and System C language. The results produced by this method are discussed in Table 1.

Table 1. Evaluation parameters

Parameter	Value
Data Set	Natural & raw images
Number of images	Hundred
Tools Used	Matlab 2017a, Xilinx XSG
Name of the device	FPGA - Vertex 2 Pro
Languages used	HDL, System C

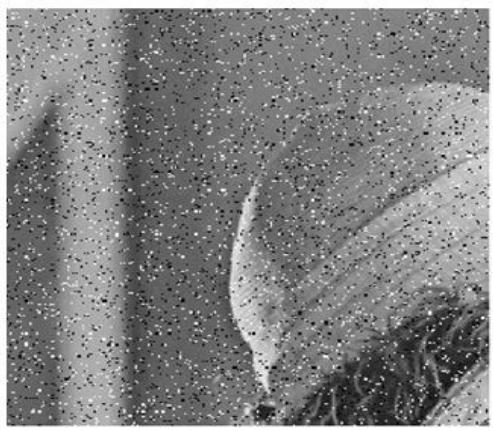

Figure 6(a). Input image

Figure 6(b). Filtered image

Figure 6(a) depicts the input image and Figure 6(b) represents the filtered output images which are produced by our proposed algorithm.

The performance result of the proposed implementation is depicted in Table 2 for various sizes of image displacement. In specific, the four display the process time for every application where the variation in the time unit is explicit. Regarding FPGA, the processing is parallel, and its iterative pixel numbers allow for reaching the minimal processing duration. From the final column, a high speed factor is achieved. It is also found that the speed up and the number of displacements are directly proportional.

This result also highlights that the total count of movements has no impact on the process time in FPGA. In contrast to the PC solution, the process time depends on the count of movements. In addition, PC solutions are found to be simple and help quick implementation dissimilar to FGPA. The image quality and filter performance can be determined using the two measured Mean Square Error and Peak Signal-to-Noise Ratio.

Table 2. Summary of proposed implementation

Size of the image (in pixel)	Number of display	Processing time (in seconds)	Processing time to Capture (in ms)	Speed up Factor
320X240	1	0.3	7.6	39.0
640X480	1	1.2	30.7	39.3
640X480	4	4.6	30.7	152.3
640X480	8	9.2	30.7	300.1
640X480	16	18.4	30.7	600.9
1024X768	1	2.7	78.6	34.5

The Mean Square Error (MSE) refers to the collective squared error between the original and output images. The value of the peak error is referred to as the Peak Signal-to-Noise Ratio (PSNR). The mistake is also less when the MSE value is low. The PSNR and MSE can be found using Eq. (5) and Eq. (6):

$$PSNR = 10 \log_{10}\left(\frac{R^2}{MSE}\right) \quad (5)$$

$$MSE = \frac{\sum_{M,N}[I_1(m,n) - I_2(m,n)]^2}{M * N} \quad (6)$$

where, M & N are the total count of rows as well as columns in the original image. R refers to the highest variation found in the input image.

Table 3 depicts the comparison of parameters like PSNR and MSE for various methods over various noise levels.

Figure 7 shows the properties of DE noise parameters that can be compared, such as the PSNR values of various approaches under various noise levels.

Table 3. Performance metrics

Noise level	PSNR			MSE		
	DCT	DWT	IPC	DCT	DWT	IPC
10%	41.398	41.466	45.466	0.025	0.024	0.022
20%	39.084	41.421	43.421	0.040	0.037	0.035
30%	37.847	39.964	41.964	0.054	0.051	0.050
40%	36.773	38.782	40.782	0.068	0.067	0.065
50%	35.708	37.861	39.861	0.082	0.081	0.080
60%	35.080	37.272	39.272	0.096	0.099	0.097
70%	33.579	35.540	38.540	0.112	0.112	0.111
80%	33.976	35.122	38.122	0.126	0.125	0.123
90%	33.550	35.555	37.555	0.145	0.141	0.140

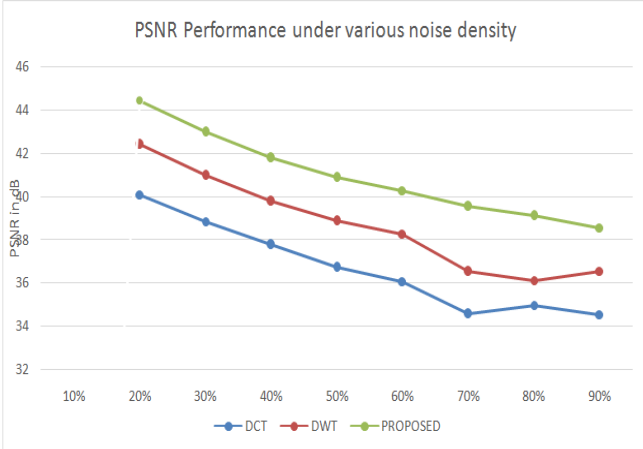

Figure 7. Comparison of PSNR performance at various noise densities

Table 4 indicates the comparison between the use of logic in dual-clutch transmission, and 131 inputs are used in that the bonded IOBs are 117 out of 190 within a minimum period of 20.650ns. Minimum input arrival time is 21.750ns and the maximum output time is 4.880ns upon processing the maximum combinational path delay is 15.153ns. Digital wavelet transform 131 inputs are used in that the bonded IOBs are 116 out of 190 within a minimum period of 15.520ns. Minimum input arrival time is 17.510ns and the maximum output time is 4.283ns upon processing maximum combinational path delay is 15.113ns and Image processing core 130 inputs are used in that the bonded IOBs are 111 out of 190 within a minimum period of 10.120ns. Minimum input arrival time is 11.821ns and the maximum output time is 03.982ns on processing the maximum combinational path delay is 15.101ns. Figure 8 depicts the comparison of area and

power consumption. It is observed that the proposed algorithm produces lesser power overhead and lesser area complexity over other methods.

Table 4. Comparison of the use of logic

Use of logic	DCT	DWT	IPC
Number of I/Os	131	131	130
Number of Bonded IOBs	117 out of 190	116 out of 190	111 out of 190
Minimum Period	20.650ns	15.520ns	10.120ns
Minimum Input Arrival time	21.750ns	17.510ns	11.821ns
Maximum Output Required time	4.880ns	4.283ns	3.982ns
Maximum Combinational Path Delay	15.153ns	15.113ns	15.101ns

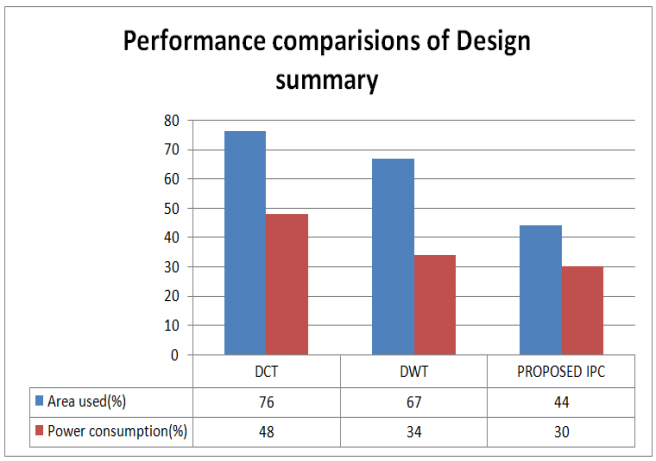

Figure 8. Evaluation of area & power consumption

4. CONCLUSIONS

The CMOS image sensor's space and power consumption are reduced by the suggested iterative pixel compression technique. For better visual quality, a multiresolution structure employs an averaging filter. The iterative coefficient is ordered according to how few bits are required to represent its magnitude in binary form. Since the transformation, iterative pixel compression coding has been used for all bits in the row with comparable contents. The transmitting of bits in each row successively is referred to as the efficient sequence for continuous transmission. The predicted pixel-averaging filter structure is smaller and uses less energy. In contrast to the current algorithms is the proposed approach. Experimental results show a 2% increment in PSNR and a 2% reduction in MSE. The further enhancement will be focusing on the reconstruction of damaged images in existing datasets to create new versions using digital image processing in deep learning technologies.

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