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# I_V Characteristic of Vertical Double Diffused Metal Oxide Semiconductor (VDMOS) Power Transistor Using Silvaco-TCAD

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*VDMOS transistor, threshold voltage, work function, software Silvaco-TCAD*

**ABSTRACT**

Today's electronics scenario finds itself with the advancement in the field of foremost important component MOSFET. Though one-step ahead of MOSFET, power MOS transistor such as VDMOS has recently begun to rival bipolar devices in power handling capability. In this paper, the results of simulation of VDMOS transistor have been presented. Additionally, the transfer characteristics of the VDMOS transistor are simulated. The drain current (Ids) as a function of the gate voltage and of the drain voltage was simulated for different work function values as well as for several oxide thickness and gate lengths, respectively. The results obtained show that when the work function and the oxide thickness as well as the gate length increase, the threshold voltage also increases. The VDMOS transistor is virtually fabricated using ATHENA software and simulation is done with help of ATLAS software and all graphs are plotted using Tonyplot in Silvaco.

## 1. INTRODUCTION

The microelectronics of today, like that of tomorrow, will be one of the crucial engines in the construction of the new information and communication society of the 21st century. Because it consists in the miniaturized realization of increasingly complex electronic functions on a single support (silicon in general). At first, the objective of microelectronics was to reduce the weight and volume of devices, but these two criteria have become secondary in the face of improving reliability and the integration density and speed of circuits. It has been largely dominated for years by CMOS integrated circuit technology [1-4]. CMOS technology is a planar technology intended for the development of very high-scale integration systems. VLSI (Very large scale integration). Thanks to the properties of complementary MOS transistors (rated CMOS for Complementary Metal Oxide Silicon), this technology is based on n-MOSFET and p-MOSFET transistors [5, 6].

The constant progress of technological processes concerning microelectronics currently allows enormous advances to be made in the field of integration. In the same system, control components operating under a few volts (CMOS) and so-called power switches that can switch tens of volts and conduct currents of several amperes (LDMOS, IGBT or VDMOS). This type of integration is called "Smart Power Integrated circuit", which can be translated as "intelligent" power integrated circuit [7-10]. In power electronics, bipolar transistors [11] and Thyristors [12] were the first command power devices that can be used in several power applications, but these devices are not suitable for high frequency switching applications. On the other hand, the evolution of technologies in the field of integrated circuits has allowed the development of power MOSFET transistors capable of operating at high frequency, such as VDMOS transistors [13], LDMOS [14].

The VDMOS transistor is a power transistor fabricated using the MOS double diffusion process. The source and the gate are located on the surface of the chip while the drain is located at the back of the chip. This transistor can amplify electric energy and quickly interrupt the flow of electric current at high speeds, while itself consuming less amount of energy. The VDMOS makes it possible to ensure, thanks to its vertical structure, a passage of strong currents by the parallel connection of a very large number of elementary cells (source-gate). This slide also has the advantage of a high switching speed linked to the absence of storage of minority carriers. And it has a high input impedance and therefore ease of control by the isolated gate. On the other hand, the voltage drop is relatively high in the on state. This is due to the absence of a strong injection plasma zone in the N zone [15-17]. So the VDMOS transistor became Stronger in different applications, such as in high frequency devices, drive power, multiplex bus system and motor drive [18, 19].

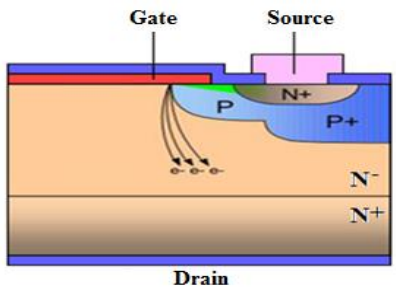


**Figure 1.** VDMOS transistor

In this paper is a presented characteristic of VDMOS transistor of electrical parameters like drain current, gate voltage employing the ATHENA fabrication simulator to fabricate while ATLAS simulator to characterize the device electrically [20]. In ATLAS, the transfer characteristic was generated by fixing the drain voltage (Vds) at a fixed value, e.g., 5V and 15V, and then ramping the gate voltage from 0V to 10V with the step of 0.2V using a sequence of SOLVE statement of the program. In addition, the impact of work function, oxide thickness and gate length on drain current are presented.

## 2. VDMOS: PROCESS SIMULATION

The VDMOS transistor used in this study were fabricated on P-type (100) wafer, which ensures a better quality of gate oxide. We will describe the process of this manufacture by the following steps: The first step consists in the oxidation of the substrate to have a layer of silicon oxide $SiO_2$ (range between 0.5 and 2 nm), from which a temperature is applied in an interval, which goes from 800 to 1000°C for 35min in order to define the oxide of gate.-The second step consists in depositing a layer of polysilicon with a thickness of 500nm by adding by diffusion a layer of passivation with a thickness of 50nm of silicon oxide ($SiO_2$). -Then, the third step is based on the deposition of nitrided silicon by the PECVD method with a layer thickness of 500nm, followed by dry etching of silicon nitride.-The next step is to dope uniformly by the ion implantation method, the etch part using boron with a dose of 5*1013 /cm$^3$ and an energy of 100 Kev to have the body P, after in fact a thermal annealing, then we move on to the diffusion of boron impurities to have a doping depth of 2 µm leaving our pattern under a temperature of 1100°C for 60 min.

After that, we do a dry oxidation to have a layer of silicon oxide, under a temperature of 800°C up to 1050°C with the use of 6.2*10$^7$ of $O_2$ for 5 to 20 minutes. Moreover, at the end, we make a diffusion using phosphorus impurities under a temperature of 800 to 900 °C for 10 to 20 minutes.

***Photo lithogravure-1***: This operation consists of depositing a photosensitive resin in a thin and uniform film with a thickness of 0.2 µm followed by a step of etching the resin of the unprotected region. The last technological step consists in depositing a thickness of 0.75µm of aluminum.

***Photo lithogravure-2:*** This step consists of depositing a resin on aluminum followed by an etching of the unwanted regions to have contact with the source.

The final result of the fabrication process is shown in Figure 2.

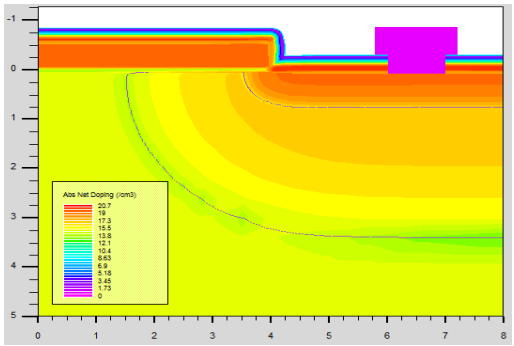

**Figure 2.** Simulated net doping of power VDMOS using Silvaco tool

The net doping profile of the VDMOS structure is shown on Figure 3.

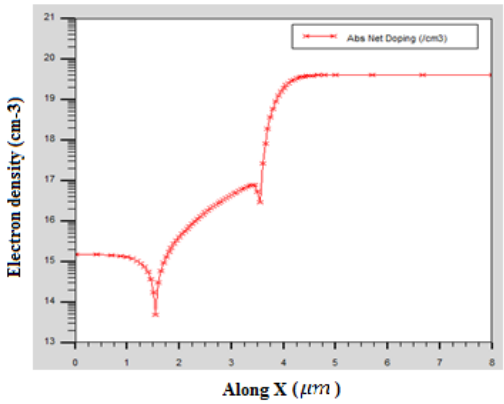


**Figure 3.** Simulated net doping profile

## 3. VDMOS: DEVICE SIMULATION

### 3.1 I_V characteristics

The software Silvaco-Atlas was used to construct and simulate the structure and characteristics electrical of the VDMOS structure (Figure 1).

In Figure 4, $I_{ds}$-$V_{gs}$ transfer characteristic is shown on a linear scale for VDMOS transistor. On Figure 4 in linear region extracting threshold voltage the value is 3.34 $V$ at $V_{ds}$=10V. Threshold voltage of the device is an important parameter, which decides the device performance. The threshold voltage expression in case of VDMOS transistor can be expressed by Marcault et al. [21-23]:

$$V_t = \frac{t_{ox}\sqrt{4\varepsilon_{si}kTln(^{n_{AP}}/_{n_i})}}{\varepsilon_{ox}} + 2\emptyset_m \quad (1)$$

where, $\emptyset_m = \frac{kT}{q} ln\left(\frac{n_{AP}}{n_i}\right)$, semiconductor work function, $t_{ox}$ is the gate oxide thickness, $\varepsilon_{si}$ and $\varepsilon_{ox}$ are, respectively, silicon and oxide permitivities, $n_{AP}$ is the doping concentration and $n_i$ is the intrinsic concentration.

The drain current can be calculated in saturation region by Surbhi Sharma Vani and Shivani [24]:

$$I_{ds} = \mu_n \frac{w}{L}(V_{gs} - V_t)C_{ox}V_{ch} - \frac{1}{2}V_{ch}^2 \quad (2)$$

And for the high drain voltage, can be expressed by [10]:

$$I_{ds} = \frac{1}{2}\mu_n \frac{w}{L}C_{ox}(V_{gs} - V_t)^2 \quad (3)$$

where, $\mu_n$ is the electron channel mobility (cm$^2$/(V.s)); $L$ is the channel length (µm); $w$ is the channel width (µm); $C_{ox}$ is the capacitance of gate oxide (µF); $V_{ch}$ is the voltage drop along the channel inversion (V).

Figure 5 shows the transfer characteristic of the VDMOS transistor, for different drain voltages such as $V_{ds}$=5V up to $V_{ds}$=30V.

In Figure 5, it is observed that as the gate voltage increases above the threshold voltage, the conductance increases. As a

result, a larger current will flow when the gate voltage is higher than the threshold voltage and the drain voltage is increased.

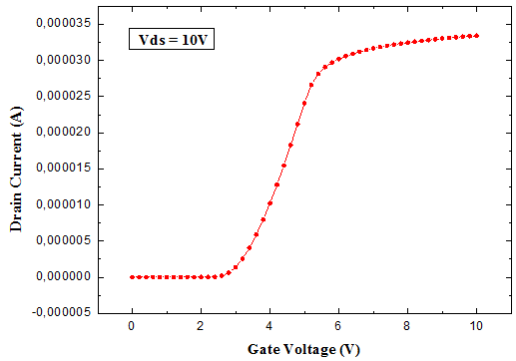


**Figure 4.** Transfer characteristic at Vds=10V

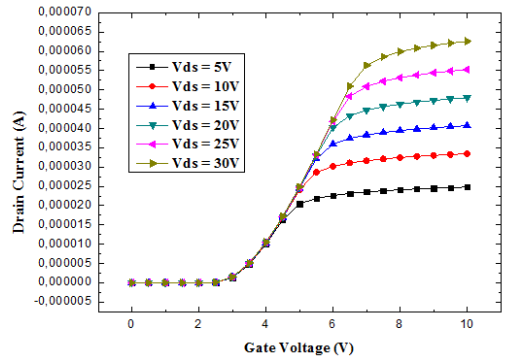


**Figure 5.** Transfer characteristic for different drain voltage

The drain current as a function of the drain voltage for different gate voltages is shown in Figure 6. The effect of the gate voltage on the output characteristics ($I_{ds}$-$V_{ds}$) was also observed.

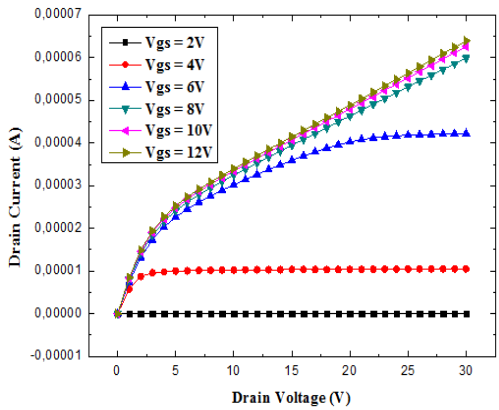


**Figure 6.** Output characteristic for different gate voltages

The results obtained clearly show a good saturation region of the device at higher gate bias, and the drain current is larger for gate voltages increase.

### 3.2 Work function effect

It is very useful to consider the impact of output work on device current and performance.

In Figure 7, we present the effect of output work for different gate voltages. We notice that the lower the output work, the greater the drain current.

Since the work function of the metal is low, this causes the number of carriers, which cross the metal-semiconductor barrier to become greater. And we notice the more the low output work the threshold voltage decreases (Figure 8).

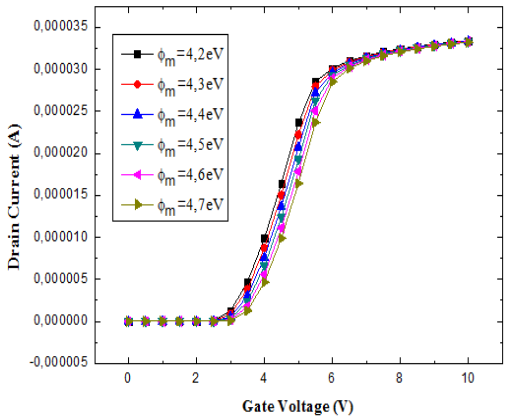


**Figure 7.** Influence of the gate work function on the drain current for different gate voltage

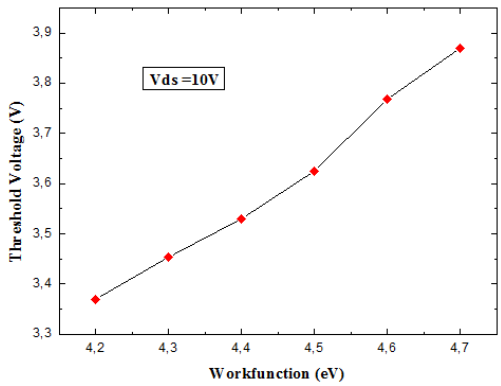


**Figure 8.** Threshold voltage versus gate work function

### 3.3 Gate length effect

The drain current in dependence on the bias voltages, canal length has been carefully investigated. Figure 9 represent $I_{ds}$ ($V_{gs}$) characteristics for different channel lengths. It can observe that when channel length decrease, drain current increase.

In addition, we can observe too, influence the channel length on threshold voltage represented on Figure 10.

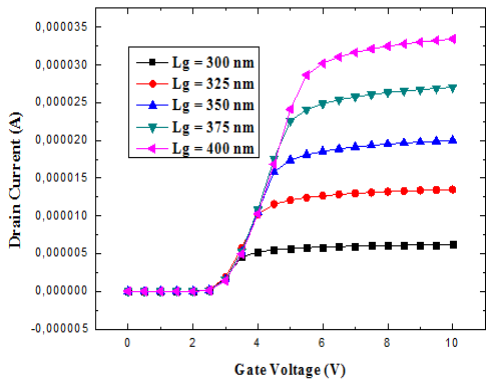


**Figure 9.** Influence of the channel length on the drain current

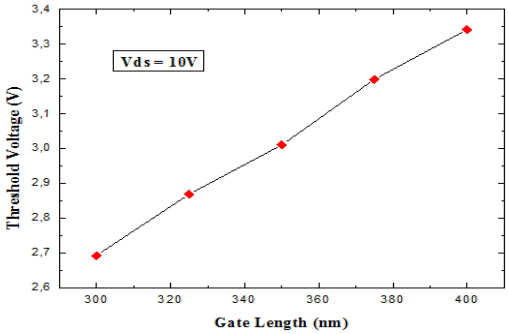


**Figure 10.** Threshold voltage versus gate length

### 3.4 Oxide thickness effect

Figure 11 presents the drain current versus the gate voltage for different oxide thickness for the VDMOS transistor. It can be seen that when the oxide thickness increases the drain current decease. This is because electric field responsible for drain current increase with increases in gate voltage and decrease with oxide thickness. Also, Figure 12 presents the threshold voltage versus oxide thickness. We can observe the increase of threshold voltage when the oxide thickness increases thus means that there is a linear relationship between the two parameters studied.

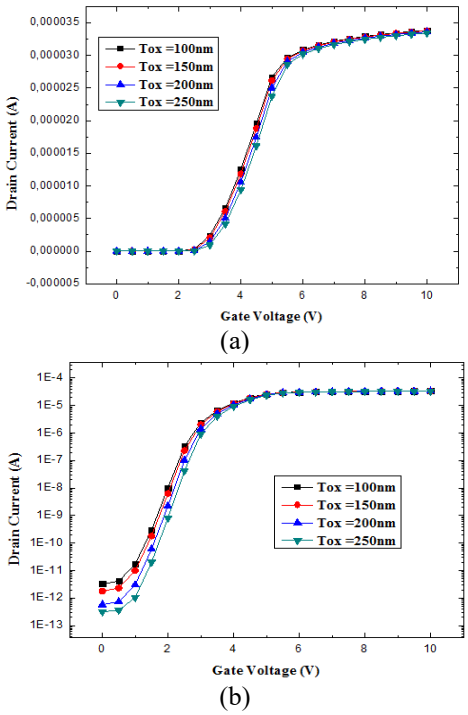


**Figure 11.** Influence of the oxide thickness on the drain current lineair (a) and log scale (b)

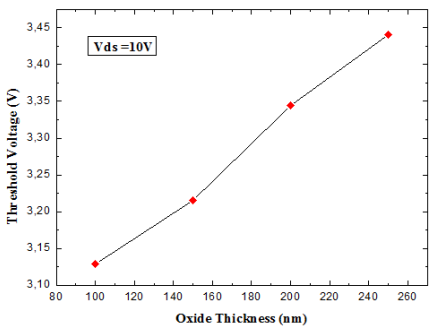


**Figure 12.** Threshold voltage versus oxide thickness

## 4. CONCLUSIONS

In this paper, results of the simulate I_V characteristics of VDMOS transistor using Silvaco-TCAD are presented. According to these simulation results, it is found that when channel length decrease, drain current increase; as well as lead to a decrease of the threshold voltage dramatically. In order to have an acceptable threshold voltage we study the influence of the gate function and conclude for optimize the threshold voltage, the solution is to choose a gate metal with a high value of work function.

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