



Capacitor Converter DC Circuit Breaker with Current Limiting Function

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ABSTRACT

DC circuit breaker is the core equipment for the safe and stable operation of DC transmission system. In order to design a DC circuit breaker with low cost and current limiting function, a capacitor converter DC circuit breaker with current limiting function is proposed in this paper. The topology uses capacitance to replace IGBT to realize the switching of circuit state, which greatly reduces the number of IGBT, moreover, through the use of current limiting branch, the peak value and rate of current are restrained, the requirements of energy absorption capacity of lightning arrester are reduced, the fault cut-off time is shortened, and the cost and technical difficulty are greatly reduced. In this paper, the working principle of the extracted topology is studied and analyzed in stages, and then the parameters are designed. Finally, the system simulation model is built by using PSCAD software to verify the simulation model. Compared with the typical circuit breaker design scheme, the rationality and superiority of the proposed scheme are proved.

1. INTRODUCTION

At present, the flexible DC power grid technology of modular multilevel converter (MMC) has gradually developed into one of the important choices of new energy power generation [1]. Overhead line transmission is the main transmission mode of DC Power Grid Group [2]. With the increasing application of new energy power generation year by year, the scale of HVDC transmission system continues to expand because HVDC can more effectively improve the utilization efficiency of renewable new energy [3]. However, due to the increasingly complex structure of DC transmission system, it has brought great potential safety hazards to the operation of the system and converter station [4]. As the core equipment to protect the safe and stable operation of DC system, the impedance of DC power grid is very low. In case of fault, the current will rise rapidly within a few milliseconds, which seriously threatens the safety of power grid. Therefore, the fault must be removed quickly and effectively [5].

High voltage DC circuit breakers are divided into mechanical DC circuit breakers, all solid state DC circuit breakers and Hybrid DC circuit breakers [6]. Hybrid DCCB combines the first two technologies, which can perfectly meet the requirements of fast DC breaking speed and reduce DC on state loss [7]. In 2012, abb of Switzerland researched and manufactured Hybrid DC circuit breaker for the first time [8]. In 2014, the global energy Internet Research Institute developed a hybrid DCCB based on fast mechanical switch and full bridge module cascade, and the circuit breaker was applied in Zhoushan flexible DC transmission project in 2016 [9]. In 2019, in the experiment of Zhangbei flexible DC power grid, the DC circuit breaker with voltage level up to 535 kV passed the acceptance test [10]. Since then, various types of hybrid HVDC circuit breaker topologies have been proposed one after another.

Due to the increasing voltage of DC power transmission, the

application of fault current limiter is proposed in order to reduce the current borne by the circuit breaker during fault [11]. The current limiter can not only limit the rise rate of fault current after fault, but also reduce the peak value of fault current, so as to reduce the current capacity borne by the circuit breaker. The resistance current limiter proposed in Ref. [12] applies superconducting technology. Due to the high cost of superconducting technology and high requirements in practical application, it is difficult to be applied to engineering. The topologies proposed by Zhang et al. [13] are all added with pre charging capacitors. After the fault current is cut off, the voltage polarity of the capacitor changes, but it is difficult to restore its original polarity. Therefore, pre charging is required when reclosing. The working principle of the multi branch current limiting circuit breaker proposed in the literature [14, 15] is that when the line fails, the current inductance is converted from parallel to series to realize the current limiting capacity, and the current limiting effect is good. However, because it is divided into multiple branches, the number of IGBTs and the cost of circuit breakers soar. Moreover, a large number of IGBTs in series have the problem of dynamic voltage equalization, which makes the scheme more difficult [16]; The H-bridge structure adopted in Ref. [17] not only enables the circuit breaker to realize bidirectional shutdown, but also halves the number of IGBT used, but also suppresses the rise rate and peak value of fault current. However, a large number of IGBT devices need to be connected in series and parallel, and the cost is still high.

In order to better reduce the cost of DC circuit breaker and strengthen the current limiting capacity of circuit breaker, a capacitor converter DC circuit breaker (CCL-DCCB) topology with current limiting function is proposed in this paper. The topology uses the converter capacitor to replace the IGBT of the transfer branch in the traditional Hybrid DC circuit breaker, and the topology uses the bypass branch to reduce the energy absorbed by the arrester. The current limiting branch is

designed in the form of the combination of resistance, inductance and capacitance to effectively suppress the fault current. In addition, the current limiting branch can realize internal self charging without configuring charging equipment.

2. TOPOLOGY AND WORKING PRINCIPLE

2.1 Topology

1) Current conducting branch: it is composed of ultra fast mechanical switch (UFMS) and load transfer switch (LCS). When the circuit operates normally, the only path of current.

2) Current limiting branch: it is composed of four groups of thyristors, a group of freewheeling diode D, capacitor C_1 , current limiting inductance L and current limiting resistance R_L . The suppression of the circuit current is realized by the charge and discharge of capacitor C_1 and the limitation of inductance L on the current.

3) Breaking current branch: it is composed of energy discharge resistance R_2 , thyristor group T_5 , converter capacitor C_2 , metal oxide arrester MOV, thyristor T_5 and resistance R_2 in series in parallel. This part is used to carry and break the fault current, and use the lightning arrester to dissipate the energy on the non fault side.

4) Drainage current branch: it is composed of unloading resistor R_{by} and unloading thyristor T_{by} in series. When the arrester mov starts to act, the fault side inductance L_{dc} is removed by the bypass, and the energy unloading resistance R_{by} in the bypass branch absorbs and dissipates the energy on the fault side, reducing the energy absorbed by the arrester MOV (Figure 1).

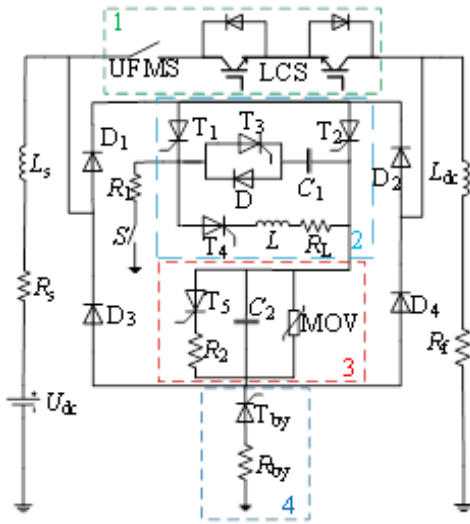


Figure 1. CCL-DCCB topological structure

2.2 Working principle

According to the Ref. [18], due to the small error, MMC can be simplified as the series equivalent of power supply U_{dc} , resistance R_s and inductance L_s . The fault current transfer path of CCL-DCCB is shown in Figure 2. The flat wave reactance is L_{dc} , and the equivalent resistance is expressed in R_f .

1) Pre-charge process ($t_0 < t < t_1$)

From t_0 to t_1 , the DC system operates stably and normally. During this period, the initial charging of capacitor C_1 is completed through the conduction of T_2 and S . The charging

principle diagram of capacitor C_1 is shown in Figure 2(a). The function of large resistance R_1 is to limit the charging current value. When the capacitor C_1 is charged, the current flowing through T_2 decreases to zero and T_2 is successfully turned off. At this point, the pre-charge of capacitor C_1 is completed.

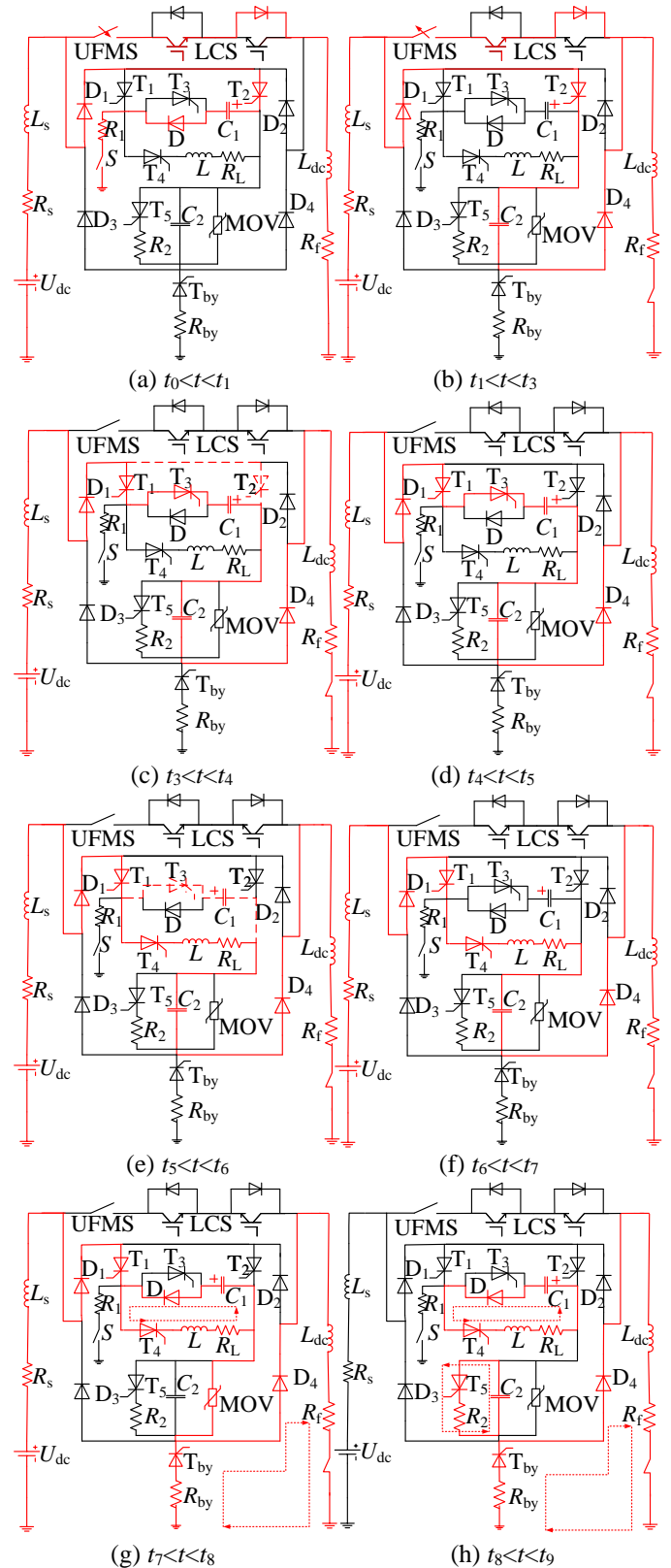


Figure 2. Fault current transfer path of CCL-DCCB

2) Current limiting preparation process ($t_1 < t < t_3$)

When a fault occurs at t_1 , the current of the through-current branch increases rapidly. Since no fault is detected, the

through-current branch is still on, and the other branches are still in the off bypass state. At time t_2 , a short-circuit fault is detected, the LCS in the current branch is quickly shut down, and a shut-off signal is given to the UFMS, and the UFMS starts to open distance. Turn on T_2 in the current passing branch and the converter capacitor C_2 in the current breaking branch, the fault current begins to transfer from the current passing branch to the circuit breaker, and the converter capacitor C_2 begins to charge, ensuring that the current branch does not need to bear high voltage. At time t_3 , UFMS reaches the rated opening distance (generally 2 ms). The current path in this period is shown in Figure 2(b).

($t_1 < t < t_2$): during t_1 to t_2 time period, the DC line fails, but due to the delay, only the smoothing reactance L_{dc} suppresses the fault current. According to KVL, the equation can be obtained:

$$U_{dc} = L_0 \frac{di_{dc}}{dt} + R_0 i_{dc} \quad (1)$$

The initial value of i_{dc} in the equation is the current value before the fault occurs, that is $i_{dc}(t_0) = I_n$. The solution is as follows:

$$i_{dc} = \frac{U_{dc}}{R_0} (I_n - e^{-(t-t_0)/\tau}) \quad (2)$$

where: $\tau = L_0 / R_0$; $R_0 = R_s + R_f$; $L_0 = L_s + L_{dc}$.

($t_2 < t < t_3$): At time t_2 , the conduction of converter capacitor C_2 can be obtained from the equation according to KVL:

$$\begin{cases} U_{dc} = L_0 \frac{di_{dc}}{dt} + R_0 i_{dc} + u_{C_2} \\ i_{C_2} = i_{dc} = C_2 \frac{du_{C_2}}{dt} \end{cases} \quad (3)$$

It can be seen from equation (2) that the current value of the line is $i_{dc}(t_2) = i_{C_2}(t_2) = I_2$, which can be obtained by substituting into Eq. (3):

$$i_{C_2} = i_{dc} = e^{-\alpha(t-t_2)} (U_{dc} C_1 \omega \sin(\omega(t-t_2)) - I_2 \sin(\omega(t-t_2) - \beta)) \quad (4)$$

where:

$$\alpha = R_s / 2(L_s + L_{dc}); \beta = \arctan(\omega / \alpha); \omega = 1 / \sqrt{C_2 L_0}; R_0 = R_s + R_f; L_0 = L_s + L_{dc}.$$

3) Current limiting process ($t_3 < t < t_8$)

($t_3 < t < t_4$): At time t_3 , after the UFMS is fully open, the signal is sent to T_1 , and T_1 immediately turns on (T_2 has been successfully turned on at time t_3). By analyzing the circuit composed of C_1 , T_3 , T_1 and T_2 , it can be seen that T_1 is successfully turned on after giving T_1 turn on signal because T_1 bears positive pressure before turning on, the capacitor C_1 and puts it into operation. Since the anode voltage direction of capacitor C_1 is opposite to the short-circuit current direction, the capacitor discharges first, the voltage released by capacitor C_1 makes T_3 turn on, and T_2 turns to bear the back voltage. Therefore, the initial anode current of T_2 decreases rapidly,

and the current flowing to T_2 is gradually transferred to T_1 . Until t_4 , the current flowing through T_2 decreases to zero, and T_2 is successfully turned off by T_1 . The current path in this period is shown in Figure 2(c).

($t_4 < t < t_5$): At t_4 , T_2 is turned off, but the discharge of capacitor C_1 is not over. At t_5 , the discharge of converter capacitor C_1 is over. The current path in this period is shown in Figure 2(d).

The dynamic process of C_1 discharge is described as follows:

$$\begin{cases} U_{dc} = L_0 \frac{di_{C_1}}{dt} + R_0 i_{C_1} - u_{C_1} + u_{C_2} \\ i_{C_1} = i_{dc} = i_{C_2} = -C_1 \frac{dU_{C_1}}{dt} \end{cases} \quad (5)$$

Let the initial charging value of capacitor C_1 be the voltage value U_0 during pre-charge. Since T_2 turns off rapidly, it can be ignored, that is, it is considered that all the current is transferred to T_3 branch at t_3 time. The initial value of the current flowing through the capacitor C_1 is the current value obtained by taking the time t_3 into Eq. (4). Assuming that the current value $i(t_3) = i_{dc}(t_3) = I_3$ at this time, substituting into the Eq. (5), it can be solved that the capacitor voltage and capacitor branch current in this stage are:

$$U_{C_1} = (U_{dc} + U_{C_1}) \cos(\gamma(t-t_3)) - \frac{I_3}{C_1 \gamma} \sin(\gamma(t-t_3)) - U_{dc} \quad (6)$$

$$i_{C_1} = (U_{dc} + U_{C_1}) C_1 \gamma \sin(\gamma(t-t_3)) + I_3 \cos(\gamma(t-t_3)) \quad (7)$$

where, $\gamma = \sqrt{\frac{C_1 + C_2}{C_1 C_2 L_0}}$; $L_0 = L_s + L_{dc}$.

($t_5 < t < t_6$): At t_5 , the discharge of capacitor C_1 ends. At this time, the initial voltage value of capacitor C_1 is 0, that is $u_{C_1}(t_5) = 0$.

$$\begin{cases} U_{dc} = L_0 \frac{di_{C_1}}{dt} + R_L i_L + u_{C_1} + u_{C_2} \\ u_{C_1} = -L \frac{di_L}{dt} - R_L i_L \\ i_L = -C_1 \frac{du_{C_1}}{dt} \\ i_{C_2} = i_{dc} = i_{C_1} + i_L \end{cases} \quad (8)$$

Simplification:

$$\frac{C_1 C_2}{C_1 + C_2} L_0 \frac{d^2 u_C}{dt^2} + \left(\frac{L_0 + L}{L} \right) u_C + U_{dc} = 0 \quad (9)$$

According to Eq. (7), the initial value of current at t_5 is $i_{C_1}(t_5) = i_{dc}(t_5) = I_5$. Substitute the initial value $U_{C_1}(t_5) = 0$ into the Eq. (8).

$$\begin{cases} i_{C_1} = AC_1\lambda \sin[\lambda(t-t_5)] + I_5 \cos[\lambda(t-t_5)] \\ u_{C_1} = \frac{-I_5}{\lambda C_1} \sin[\lambda(t-t_5)] + A[\cos \lambda(t-t_5) - 1] \\ i_L = -\frac{A}{\lambda} [\sin(\lambda(t-t_5)) - \lambda(t-t_5)] \\ \quad + B[1 - \cos(\lambda(t-t_5))] \end{cases} \quad (10)$$

where: $A = \sqrt{LU_{dc}/(L+L_0)}$; $C = \frac{C_1 C_2}{(C_1 + C_2)}$; $B = \frac{I_5}{LC} \lambda^2$; $\lambda = \sqrt{(L+L_0)/L_0 LC}$; $L_0 = L_s + L_{dc}$.

With the reverse charging of capacitor C_1 , the longer the charging time, the smaller the current I_{C_1} flowing through capacitor C_1 and the greater the voltage u_{C_1} . At time t_6 , u_{C_1} rises to the system voltage and capacitor C_1 is disconnected. The current path in this period is shown in Figure 2(e).

($t_6 < t < t_7$): After t_6 , the resistance sensing branch is fully put into operation. According to Eq. (10), the initial value of current at t_6 is $i_{dc}(t_6) = i_L(t_6) = I_6$. From KVL and KCL, the instantaneous current i_L in the resistance sensing branch is:

$$i_L = I_6 e^{-(t-t_6)/\tau_0} + \frac{U_{dc}}{R_\Sigma} (1 - e^{-(t-t_6)/\tau_0}) \quad (11)$$

where: $\tau_0 = (L_0 + L)/R_L$; $R_\Sigma = R_L + R_s + R_f$.

When the current limiting impedance L branch is turned on, the current rise rate decreases. The current path in this period is shown in Figure 2(f).

4) Cut off process ($t_7 < t < t_8$)

At t_7 , when the arrester mov reaches the working voltage, the arrester MOV is turned on and operated, the converter capacitor C_2 is turned off, and the drainage branch is turned on and grounded. After the arrester MOV is put into operation, it starts to absorb the energy on the non fault side and limit the overvoltage. The reactance on the fault side begins to discharge to the grounding resistance R_{by} through the thyristor T_{by} of the drainage branch. The operation of the drainage branch reduces the energy consumption demand of the arrester. The capacitor C_1 forms a charge discharge circuit through diode D , current limiting inductance and current limiting resistance. The capacitor C_1 is discharged through the circuit first and then charged, so that the capacitor current returns to the state after pre-charge, so that it is not necessary to recharge the capacitor C_1 for each subsequent disconnection fault current. At t_8 , the current flowing through the arrester is zero, the energy absorption of the arrester is completed, and the fault line is cut off successfully. The current path in this period is shown in Figure 2(g).

The recording $t_7 \sim t_8$ period is the energy absorption time of the arrester Δt . According to Eq. (11), the initial value of current at t_7 is $i_{dc}(t_7) = i_L(t_7) = I_7$, and the action voltage is U_{MOV} , which is obtained from KVL:

$$i_{dc} = I_7 e^{-\Delta t/\tau_1} + \frac{U_{dc} - U_{MOV}}{R_s + R_L} (1 - e^{-\Delta t/\tau_1}) \quad (12)$$

The solution is as follows:

$$\Delta t = -\frac{L + L_s}{R_L + R_s} \ln \frac{\Delta U}{(R_L + R_s)I_7 - \Delta U} \quad (13)$$

where: $\tau_1 = (L + L_s)/(R_L + R_s)$; $\Delta U = U_{dc} - U_{MOV}$.

5) Energy release process ($t_8 < t < t_9$)

At t_8 , the energy absorption of the arrester ends and the current on the non fault side drops to zero. The energy on the fault side is exhausted through the grounding resistance R_{by} . At the same time, the capacitor C_1 also continues to charge and discharge through the diode D and the resistance sensing branch to form a discharge circuit. Turn on the signal to the thyristor T_5 , and the converter capacitor C_2 discharges through the energy discharge resistance R_2 . At time t_9 , all circuits are completed. The current path in this period is shown in Figure 2 (h).

When the capacitor C_1 is charged and discharged through the diode D with the current limiting inductance and current limiting resistance, there is no oscillation process due to the unidirectional conductivity of the diode. From Eq. (10), $u_{C_1}(t_6) = U_6$, from Eq. (11), $i_{dc}(t_7) = i_L(t_7) = I_7$, the KVL equation is:

$$LC_1 \frac{d^2 U_{C_1}}{dt^2} + R_L C_1 \frac{dU_{C_1}}{dt} + U_{C_1} = 0 \quad (14)$$

The charging current of the capacitor is:

$$i_{C_1} = \theta \sqrt{\frac{C_1}{L}} e^{-\tau_2(t-t_7)} \sin(\chi t + \delta) \quad (15)$$

where: $\tau_2 = \frac{R_L}{2L}$; $\chi = \sqrt{\frac{1}{LC_1 - \frac{R_L^2}{4L^2}}}$; $\theta = \frac{\sqrt{U_7^2 + (\tau_2 U_7 / \chi - I_7 / \chi C_1)^2}}{\sqrt{LC_1 - \frac{R_L^2}{4L^2}}}$; $\sigma = \arctan[U_7 / (\tau_2 U_7 \chi - I_7 / \chi C_1)]$.

3. DEVICE PARAMETER DESIGN

The equivalent rated voltage of DC power grid in this paper is 500 kV. The device selection and analysis of circuit breaker are based on the voltage of 500 kV. In this section, the current limiting inductance L , current limiting resistance R_L , discharge resistance R_2 and capacitors C_1 and C_2 of the circuit breaker are analyzed to ensure that CCL-DCCB can realize optimal shutdown.

3.1 Parameter design of current limiting inductance L

The use of current limiting reactance in the circuit suppresses the rising rate of current. The larger the reactance, the more obvious the suppression effect, but it will prolong the time when the current limiting inductor L is fully put into operation and prolong the fault breaking time. The current limiting inductor L is put into operation from t_5 , fully operational at t_6 . At this time, $i_C = 0$ is brought into Eq. (10) to obtain the time required for the resistance sensing branch to be fully put into the fault circuit Δt_0 is:

$$\Delta t_0 = t_6 - t_5 = \frac{\pi - \eta}{\rho} \quad (16)$$

where: $\eta = \arctan \left[\frac{I_4(L_0+L)(C_1+C_2)}{U_{dc} L C_1 C_2 \rho} \right]$; $\rho = \frac{1}{\sqrt{L_0 C_2}}$.

According to the analytical formula (16), The value of Δt_0 is affected by inductance L , capacitance C_1 and C_2 . When it is determined that the values of capacitors C_1 and C_2 remain unchanged, it can be seen that the value of Δt_0 will increase with the increase of inductance L ; Moreover, when the fault current flowing through it reaches a steady state, the larger the reactance L , the more energy stored by the reactance L itself. Figure 3(a) is obtained according to Eq. (16), Δt_0 follows the variation law of current limiting inductance L .

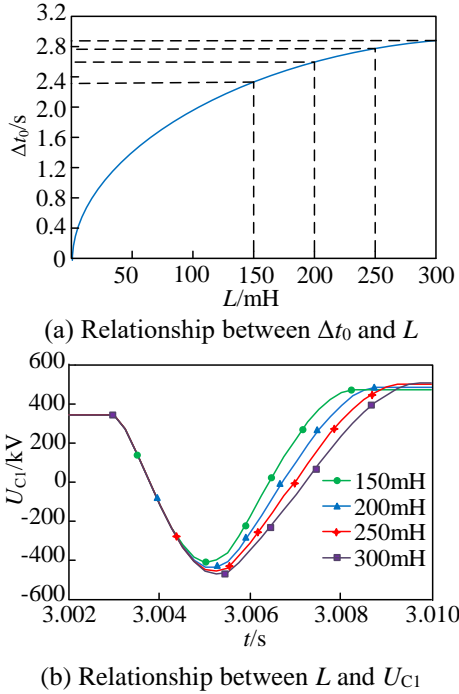


Figure 3. Influence of inductance L value

Since the size of smoothing reactor L_{dc} currently used in the project is 150 mH [13], combined with the fact that the rated voltage of DC power grid is 500 kV, the actual value of given current limiting inductance is between 150-300 mH. As shown in Figure 3(b), the larger the value of inductance L , the longer the time required for capacitor C_1 to reverse charge to the highest voltage. This shows that the larger the inductance value, the longer the time it takes for the branch where the current limiting inductance is fully put into operation, and the greater the voltage value of capacitor C_1 ; And the high-voltage reactance is expensive. Therefore, for 500 kV DC system, the resistance inductance branch adopts 200 MH current limiting inductance.

3.2 Parameter design of current limiting resistance R_L

The current limiting resistor R_L limits the rising amplitude of fault current after the resistance sensing branch is turned on; In the circuit composed of current limiting inductor L and capacitor C_1 , the energy of L is dispersed into R_L and C_1 . By changing the resistance value of current limiting resistor R_L , the charging voltage and circuit discharge time constant of C_1 can be adjusted. As can be seen from Figure 4(a), the

resistance value of R_L is inversely proportional to the voltage of capacitor C_1 ; The greater the resistance, the smaller the capacitor voltage. It can be seen from Figure 4(b) that the size of resistance R_L has no obvious effect on the size of fault current. And for high-power resistors, it is necessary to consider the limitations of their own volume and heat dissipation performance, so the resistance value cannot be increased indefinitely. Therefore, the current limiting resistor with resistance value of 10 Ω is adopted in this scheme.

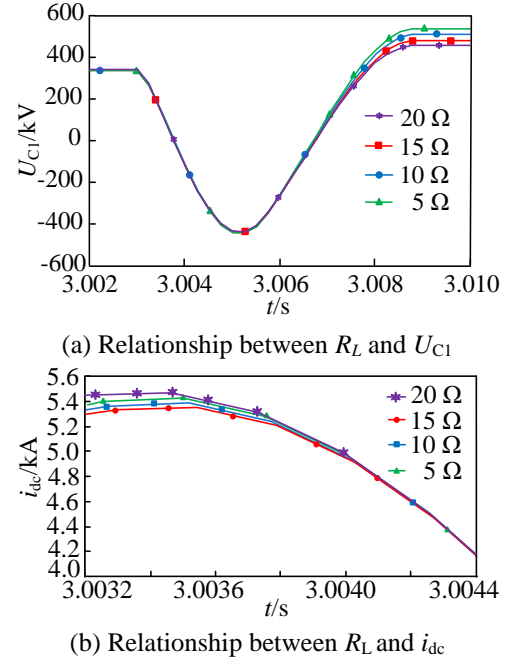


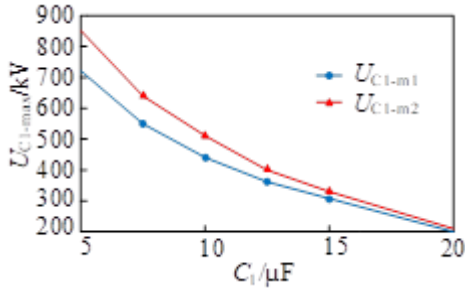
Figure 4. Influence of resistance R_L value

3.3 Parameter design of capacitor C_1 and C_2

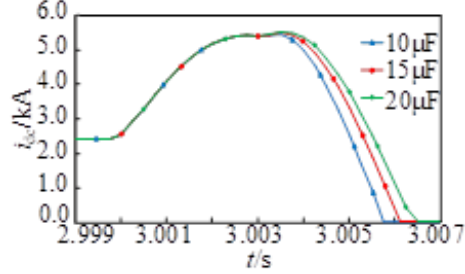
3.3.1 Parameter design of capacitor C_1

When designing the value of capacitor C_1 , the withstand voltage capacity of the capacitor during charging should be considered first. The CCL-DCCB topology proposed in this paper controls the on-off of the branch where capacitor C_1 is located through thyristor $T_1(T_2)$, and the charge and discharge of capacitor C_1 also controls the off of thyristor $T_2(T_1)$. Therefore, the voltage that capacitor C_1 can withstand is greater than the peak value of capacitor reverse voltage U_{C1m1} . The relationship between the peak value of reverse voltage U_{C1m1} and the value of capacitance C_1 is shown in Figure 5(a). Secondly, it is necessary to consider the second charging process of capacitor C_1 through the resistance inductance branch. When all the energy in the current limiting inductor is transferred to the capacitor, the capacitor voltage reaches the peak U_{C1m2} . The relationship between the capacitance voltage peak U_{C1m2} and the capacitance C_1 value is shown in Figure 5(a). It can be seen from the figure that the value of capacitance should be 10 μF -20 μF .

This paper takes 500kV DC system as the research object. By comparing the changes of line current when different capacitance values change in Figure 5(b), The smaller the C_1 value of the capacitor, the faster the charging of the capacitor, the lower the peak current, the shorter the time required for the branch where the resistance and reactance are fully put into operation, and the shorter the time required for the shutdown of the fault line. Considering comprehensively, the value of capacitance C_1 is 10 μF .



(a) Relationship between C_1 and U_{C1-max}



(b) Relationship between C_1 and i_{dc}

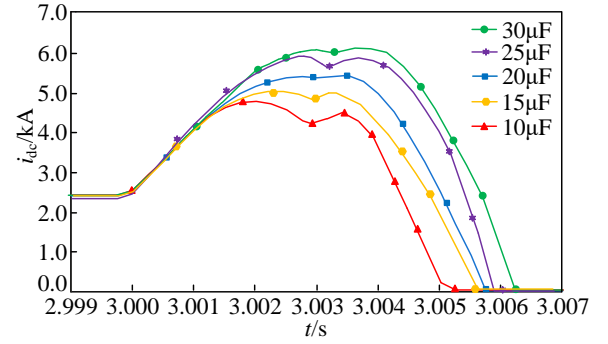
Figure 5. Influence of capacitance C_1 value

3.3.2 Parameter design of capacitor C_2

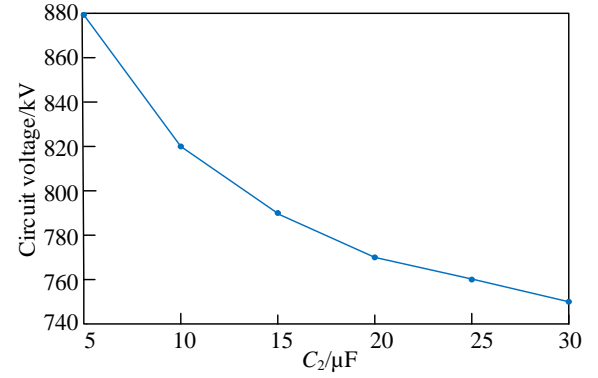
The converter capacitor C_2 is the key equipment to complete the switching in the circuit breaker design. When the voltage at both ends of C_2 reaches the MOV starting voltage, the current is transferred to MOV and the converter capacitor C_2 is disconnected. Therefore, the voltage of the whole circuit breaker is the starting voltage of MOV. Set the MOV starting voltage as U_{tig} , and the size of U_{tig} has a great impact on the converter capacitor C_2 . The larger the U_{tig} , the higher the voltage peak of the converter capacitor C_2 , the higher the requirements for the withstand voltage level of the capacitor, and the cost increases accordingly; The higher the U_{tig} , the longer the charging time of capacitor C_2 and the longer the off time of circuit breaker. In practical engineering application, the starting voltage of the arrester is 1.6 times of the rated voltage [18], that is $U_{tig} = 1.6U_{dc}$. Before the arrester reaches the starting voltage, the instantaneous voltage of the converter capacitor C_2 is shown in Eq. (17).

$$U_{C_2}(t) = \frac{1}{C_2} \int_{t_2}^t i_{dc}(t) dt \quad t_2 < t < t_7 \quad (17)$$

It can be seen from Eq. (17) that if U_{tig} is within 5 ms [19], the upper limit of capacitance C_2 brought in by system parameters $U_{C2-max}=30 \mu F$. The traditional hybrid DCCB requires U_{tig} to be less than 5 ms because the traditional hybrid DCCB uses IGBT to turn off the current, and the continuous growth of the current will cause permanent damage to power electronic devices. Although CCL-DCCB mentioned in this text replaces C_2 with converter capacitor, since the whole circuit breaker has other power electronic devices, in order to ensure the normal use of all devices, the selection of converter capacitor should be within 30 μF . As can be seen from Figure 6, the larger the value of capacitor C_2 , the longer the starting time of arrester, the larger the value of fault current, and the longer the time that the fault line is turned off. However, the smaller the value of capacitor C_2 , the greater the voltage stress of power electronic valve group in the circuit. Considering comprehensively, the converter capacitor C_2 is taken as 30 μF .



(a) Relationship between C_2 and i_{dc}



(b) Relationship between C_2 and Circuit voltage

Figure 6. Influence of capacitance C_2 value

3.4 Parameter design of energy discharge resistance R_2

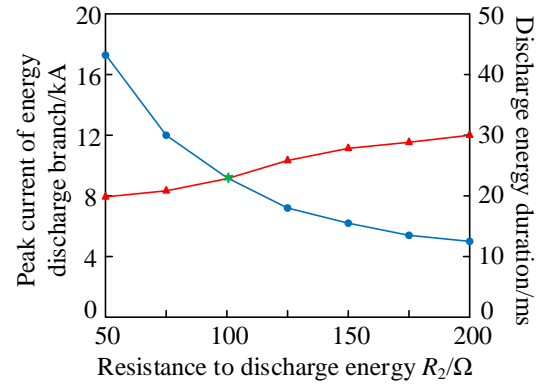


Figure 7. Influence of energy discharge resistance R_2 value

After the fault is successfully isolated, the thyristor T_5 is turned on and the converter capacitor C_2 is discharged through the energy discharge resistance R_2 . When the current flowing through the energy discharge resistance circuit decreases to zero, the thyristor T_5 is disconnected and the CCL-DCCB returns to the initial state. The greater the value of R_2 , the less likely the overcurrent phenomenon of the circuit is. However, the greater the value of R_2 , the longer the discharge time of the converter capacitor C_2 . Due to the limitation of its own volume and heat dissipation performance, the resistance value cannot be improved indefinitely. Therefore, the peak current should also be considered when designing resistance R_2 . The variation of peak current and discharge time of energy discharge branch with energy discharge resistance R_2 is shown in Figure 7. As can be seen from Figure 7, the peak current of the energy discharge branch is inversely proportional to the size of the energy discharge resistance R_2 , but the energy discharge time

is directly proportional to the size of the energy discharge resistance R_2 . Therefore, when selecting the energy discharge resistance R_2 , its resistance value cannot be too small or too large. As can be seen from Figure 7, the energy discharge resistance at the intersection of the two curves is $R_2=100 \Omega$, so the value of energy discharge resistance in this paper is 100Ω .

4. SIMULATION ANALYSIS

4.1 Simulation system parameters

Figure 8 shows the simulation model of four terminal flexible DC power grid built through PSCAD, and its parameters are shown in Table 1. When selecting various devices, first consider the actual models produced by ABB. The rated voltage and current of IGBT is $4.5 \text{ kV}/3 \text{ kA}$, the rated voltage and current of thyristor is $8.5 \text{ kV}/4.5 \text{ kA}$, and the rated voltage and current of diode is $4.5 \text{ kV}/3.8 \text{ kA}$. In the CCL-DCCB topology, the current limiting capacitor C_1 is designed as $10 \mu\text{F}$. The current limiting resistance R_L is designed to be 10Ω , the current limiting inductance L is designed to be 200 mH , and the converter capacitor C_2 is designed to be $20 \mu\text{F}$. The energy discharge resistance R_2 is designed to be 150Ω .

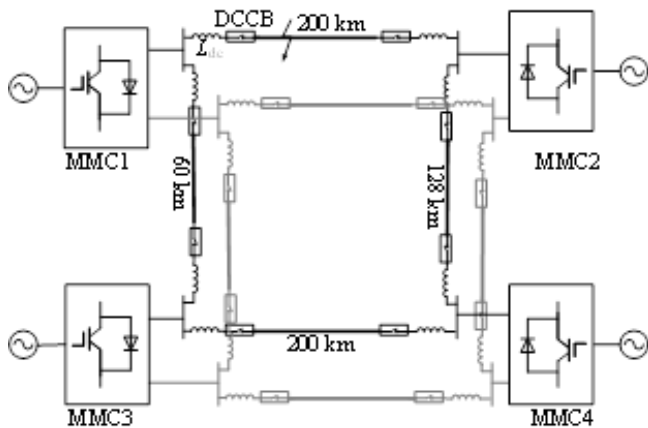


Figure 8. Simulation model of DC power grid

Table 1. Simulation parameters of DC power grid

System parameter	MMC1	MMC2	MMC3	MMC4
Converter capacity/MW	1500	500	3000	1500
Sub module capacitance/mF	7	15	15	7
Bridge arm inductance/mH	100	50	50	100
Reactance level/mH	150	150	150	150

4.2 Fault clearing simulation

Figure 9 shows the current transfer diagram of CCL-DCCB breaking fault in case of fault.

When $t=3.0 \text{ s}$ (time t_1), the system has a short-circuit fault. After a delay of 1 ms , the fault is detected when $t=3.001 \text{ s}$ (time t_2) and the current transfer begins. The LCS is turned off immediately, the thyristor T_2 and the converter capacitor C_2 are turned on at the same time, and the UFMS starts to open. After 2 ms , i.e. when $t=3.0030 \text{ s}$ (time t_3), UFMS reaches the rated opening distance and completely turns off, and gives T_3

conduction signal at the same time. At this time, T_1 is turned on under the forward voltage and the capacitor C_1 begins to discharge. When $t=3.0031 \text{ s}$ (time t_4), T_2 is turned off due to backpressure. When $t=3.0033 \text{ s}$ (time t_5), the discharge of capacitor C_1 ends, reverse charging begins, T_4 is turned on, and the branch where current limiting reactance L is located is put into use. At time $t=3.0045 \text{ s}$ (time t_6), the branch where the current limiting reactance L is located is fully put into operation, the capacitor branch is turned off, and the current rising speed is reduced. When $t=3.0049 \text{ s}$ (time t_7), the voltage at both ends of the arrester reaches the opening voltage, the arrester starts to consume energy, and the converter capacitor C_2 is bypassed; At the same time, the thyristor T_{by} of the bypass branch is on, and the bypass branch consumes the energy on the fault side; The circuit composed of resistance sensing branch and capacitor C_1 starts to charge the capacitor. When $t=3.0057 \text{ s}$ (time t_8), the fault side current is 0 and the circuit fault is cleared; Bypass branch resistance R_{by} still consumes energy at fault side; The circuit composed of resistance sensing branch and capacitor C_1 is still charging the capacitor; At the same time, the thyristor T_5 is turned on, and the converter capacitor C_2 begins to discharge through the energy discharge resistance R_2 until 3.009 s (time t_9).

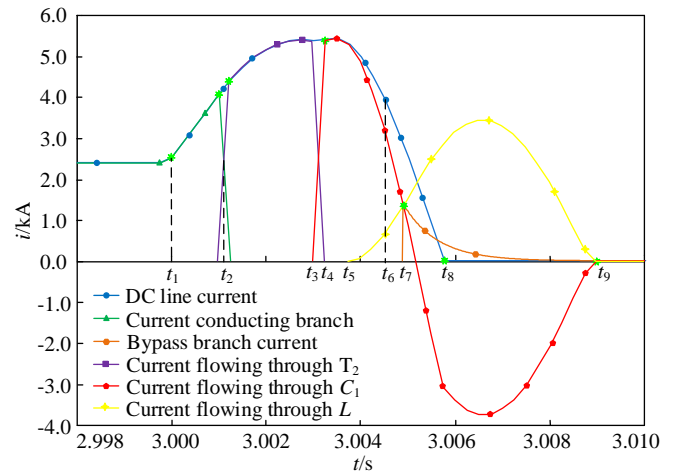


Figure 9. Simulation waveform

5. PERFORMANCE COMPARISON

In order to objectively analyze the breaking performance of the circuit breaker proposed in this paper, this paper is simulated and compared with other schemes. Scheme 1 is the traditional hybrid DCCB proposed by ABB in document [20], and scheme 2 is the current limiting hybrid HVDC circuit breaker proposed in document [21], scheme 3 is the capacitor converter DC circuit breaker proposed in document [22], and scheme 4 is the capacitor converter DC circuit breaker with current limiting function proposed in this scheme. The obtained simulation comparison diagram is shown in Figure 10.

Scheme one has no ability to suppress the fault current. Before the arrester does not act, the fault current increases rapidly to the peak value. Moreover, since the output current cannot be effectively controlled, the fault elimination time is also long, and it takes 10 ms ; At the same time, the energy absorption of the arrester is increased by 7.5 ms , and the turn-off time of the arrester is significantly reduced; The biggest difference between scheme 3 and schemes 1 and 2 is that it

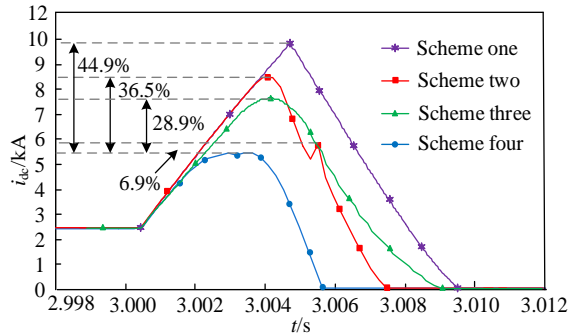
replaces IGBT power electronic devices with capacitors in the current breaking branch, which saves the cost, but the current peak value and turn-off time are improved compared with scheme 1, and the turn-off time is reduced by 1 ms to 9.0 ms compared with scheme 1; In scheme 4, on the basis of replacing IGBT with capacitor, a current limiting device is added to the circuit breaker to reduce the amplitude of breaking current, and a bypass current branch is added. Since the energy stored in the current limiting inductor is transferred to the current limiting capacitor and resistance, the energy absorbed by the arrester is reduced, the breaking speed of the circuit breaker is enhanced, and the closing time is 5.8 ms.

UFMS, 10 IGBT and 10 diodes are required. T_1 and T_4 thyristor valve groups in the current limiting branch bear 800 kV, and T_2 and T_3 thyristor valve groups bear 500 kV; the pressure bearing capacity of thyristor valve group in bypass branch is 500 kV; the pressure of thyristor valve group in the cut-off branch is 800 kV. The current demand of all thyristors is 5.4 kA, and the number of thyristors required is 924. In the scheme, the pressure bearing of diodes distributed on the bridge circuit is 800 kV, but the pressure bearing of diodes in the circuit composed of resistance sensing branch and capacitor C_1 is 500 kV, so the number of diodes required is 1252. Therefore, the scheme requires a total of 1 UFMS, 10 IGBT, 924 thyristors and 1262 diodes. The number of devices required for each scheme is shown in Table 2.

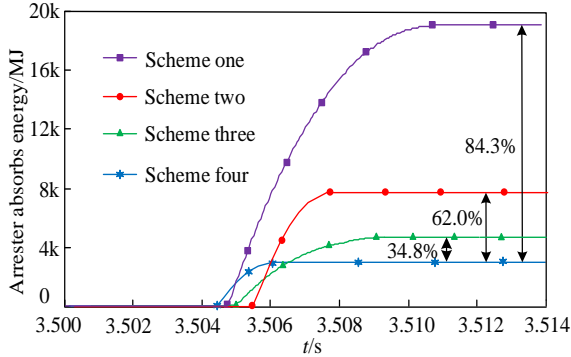
In terms of technical difficulty, the failure rate of a single IGBT is 0.0119 times/cycle, and there is a problem of dynamic voltage sharing in large-scale IGBT Series. The circuit breaker described in this paper replaces IGBT with capacitor, and the fault rate of capacitor is 0.000916 times/cycle, which is lower than that of IGBT. Almost all the circuit breakers use thyristors to complete line breaking, and the thyristor series parallel technology is mature, so the technical difficulty of large-scale use is lower than that of large-scale use of IGBT. In addition, in terms of the cost of the device itself, the price of IGBT is 5 times that of thyristor and 10 times that of diode [23]. Therefore, this scheme is high in cost performance, reliability and stability.

Table 2. Simulation parameters

Project	Scheme one	Scheme two	Scheme three	Scheme four
Number of IGBT/piece	1424	884	10	10
Number of thyristors/piece	0	627	2577	924
Number of diodes/piece	10	0	10	1262
MOV energy consumption /MJ	19.1	7.9	4.6	3.0



(a) Line current comparison diagram



(b) Comparison diagram of energy absorption of lightning arrester

Figure 10. Schemes comparison

Compared with scheme one, the peak current of scheme 4 decreases by 44.9%; Compared with scheme two phase scheme, the peak current decreases by 44.9%; Compared with the three-phase scheme, the peak current drop is 28.9%. Due to the same reference voltage of the arrester, the energy absorbed by the arrester in the scheme proposed in this paper is 84.3% lower than that in scheme one; Scheme two reduced by 62.0%; It is 34.8% lower than scheme three. However, compared with the other three schemes, the discharge time of the arrester is very short, and it can quickly recover to the rated voltage of the system after the energy absorption process. To sum up, the scheme proposed in this paper has positive significance for the development of DC circuit breaker. The comparative analysis of breaking performance parameters of the four schemes is shown in Table 2.

By comparing the number of devices used in each scheme and the energy absorption of lightning arrester, the device specifications selected in scheme 1, 2 and 3 are the same as those in this paper.

In the scheme described in this paper, all IGBT are applied to the through flow current branch. The pressure of the IGBT valve group is 22.5 kV and the through flow is 4.05 kA. 1

6. CONCLUSIONS

After analyzing the structure, principle, parameter design and simulation verification of CCL-DCCB proposed in this paper, the following conclusions are obtained.

1) CCL-DCCB replaces the traditional hybrid IGBT with converter capacitor. Compared with the traditional Hybrid DC circuit breaker, the number of IGBT is sharply reduced, and the energy consumption of lightning arrester is reduced by 84.3%, greatly reducing the cost.

2) CCL-DCCB topology uses the thyristor as the switching device, adopts the bridge structure to realize the two-way shutdown, realizes the pre charging of the circuit breaker through the DC power grid, and the addition of the current limiting device reduces the peak value of the fault current, which has good economic performance and lays a good foundation for the large-scale use of the circuit breaker.

3) The CCL-DCCB topology proposed in this paper makes full use of the power supply and charges the converter capacitor through the power supply equipment of the circuit. Moreover, the capacitor is charged through the circuit of capacitor and resistance sensing branch, so that the capacitor can be reused indefinitely after only one charge, which solves

the technical problem that it is necessary to configure charging device for pre-energy storage capacitor separately, so as to effectively reduce the volume and cost of the whole circuit breaker.

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