DC Component Extraction of Notch Filter Algorithm for Active Power Filters

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ABSTRACT

This work presents a way to handle the DC component of input signals for PLL and notch filter applications, which are utilized for filtering and synchronization. The input signal of a DC component may be due to some sort of malfunction, or it may be the result of the structure and restrictions of the measurement/conversion procedures. This part makes the system's loop oscillate at low frequencies and no filter can fully filter them out because that would significantly harm the system's dynamic response. The proposal involves augmenting the PLL structure with a new loop. It is basic architecturally and in contrast to a currently presented method and it does not detract from the algorithm's high-frequency filtering level. This Orthogonal Signal Generators (OSG) control algorithm is used for active power filter to maintain unity power factor, neutral current compensation using star/three single transformer & current harmonics mitigation. The MATLAB/Simulink results are demonstrated for the above stated Power Quality (PQ) problems.

1. INTRODUCTION

One of the most essential issues in the present distribution system is compensating of reactive power from non-linear and/or inadequate power factor loads. The problem is exacerbated by unbalanced loads. Any reactive power demand that is too high will make the feeder losses and active power flow capacity of the distribution system suffer, while causing transformer and generator damage due to a lack of balance [1]. Various load compensation solutions have been presented during the past two decades. Unbalanced and distorted currents can be corrected with these methods as can the power factor at the load bus [2]. It's important to note that all of these systems are predicated on the assumption. As a result of this, it is possible that the upstream source voltages are imbalanced or in such instances, sensitive loads must be safeguarded by a compensator that can modulate the bus voltage to give a balanced sinusoidal voltage of a predetermined magnitude [3]. Active Power Filters are widely utilized in the distribution system for reactive power compensation, load balancing, and harmonic mitigation.

There are APFs that can be used to compensate nonlinear loads for harmonic currents [4]. In either case, they can be coupled, either as a harmonic solution next to a nonlinear load or as a global solution at the Point of Common Coupling (PCC). It is typically determined by the performance, stability of network, and mitigation harmonic efficiency sought and also taken into account for cost.

As soon as the APF detects the harmonic spectrum of the load current, it generates an output current with a similar harmonic spectrum to that of the load current.

The APF does this, so the power system can concentrate on providing a fundamental current component [5].

Advancements in various control devices and algorithms make this possible. In addition to laboratory testing, these factors allowed APFs to be applied to real-life situations. An APF is more efficient than a shunt passive filter because the real power consumption is lower. Unlike shunt passive filters, there is no need to connect multiple branches to mitigate multiple harmonic orders at once [6].

One APF can shield upto a 30th–50th order harmonic, satisfying actual regulatory standards [7]. However, even if voltage imbalances and pre-distortions are avoided, APFs can still maintain the same high-quality harmonic current. The Total Harmonic Distortion (THDi) is estimated to be 5-7% with an APF and 10-15% with a passive filter. It is also more expensive (in terms of equipment, installation and maintenance) than traditional passive filters [8, 9].

An APF can be improved without changing its design by adding more power-quality features such as compensating for voltage imbalance, dips, surges, flickers and dampening circuit resonances [10, 11]. Even though the foregoing considerations raise the cost of harmonic mitigation, the additional energy requirements of the APF's inverter can be carried. DC-link and power inverter capabilities will be improved with a larger energy storage DC-link as well as an increase in the IGBT, boost filter size, heat-sink and ventilation [12-14].

Power systems use the SRF-PLL, commonly known as the dqo-PLL. When the input signal is imbalanced, the SRF-PLL suffers from double-frequency inaccuracy [15]. As a result, A Low-Pass Filter (LPF) can be used to reduce or eliminate the error whereas dual structures for negative and zero components can be used to eliminate the error [16-18].

A building block for OSG has been created with the usage of the Second-Order Generalised Integrator (SOGI) [19]. In

addition to using a DQ system, you can use an orthogonal signal in a frequency locked loop (FLL) to estimate frequency [20, 21]. This approach aligns with the idea of an adjustable notch filter (ANF) [22]. These tools have applications in control, filtering and frequency These tools are useful for frequency estimates, control, filtering, harmonics estimation, grid synchronization, as well as for three-phase applications [23, 24]. The frequency predicted by these approaches is inaccurate when the input signal has some DC [25].

This study proposes and studies an OSG control algorithm based APF for mitigating harmonics and unity power factor maintenance. For neutral current compensation is achieved by connecting star/three I-Ø transformers [26]. The proposed 6-leg VSC based Active Power Filter model is developed by using MATLAB/SIMULINK.

2. SYSTEM CONFIGURATION

Line diagram of Active Power Filter system with inductive load attached to distribution lines is shown in Figure 1. To keep the link voltage constant, a capacitor is attached to the input of the VSC. To maintain dc bus voltage and voltage regulation, Cdc generators and PI controllers are used, which in conjunction with the PWM Current Controller give switching signals for the VSC. There is a switch that allows you to regulate source currents so that at the load end, an ac capacitor bank is connected to lower the rating of Active Power Filter.

The DC capacitor, ripple filter, and IGBTs were selected according to the design of an APF. The line voltage of 415V is at the source, and the capacitor voltage is considered to be 700V. The choice of 3,000µF capacitor is considered as DC bus capacitor. The voltage of a DC capacitor is ascertained with the assistance of a star/three I-Ø transformer. The neutral is balanced by the use of a star/three I-Ø transformers to minimise the DC link voltage of the voltage source converter.

3. NOTCH FILTER BASED ON OSG CONTROL ALGORITHM

A. Unit Templates Estimation

The in-phase unit templates x_{pa}, x_{pb} and x_{pc} are

$$x_{ap} = \frac{v_{sa}}{v_{st}} \; ; x_{bp} = \frac{v_{sb}}{v_{st}} \; ; x_{cp} = \frac{v_{sc}}{v_{st}} \; ; \tag{1}$$

Then the terminal source current (v_{st}) is calculated as follows:

$$v_{st} = \sqrt{\frac{2}{3}} (v_{sa}^2 + v_{sb}^2 + v_{sc}^2)^{0.5} \tag{2}$$

To measure the voltage error, subtract V_{dc} from the reference dc connection voltage V_{dc}^* as follows:

$$V_{dre} = -V_{dc}(m) + V_{dc}^*(m) \tag{3}$$

K_{pd} is a proportional gain and K_{id} is an integral gain, which is used to determine the dc loss component, I_{lss}.

$$I_{lss}(m) = I_{lss}(m-1) + K_{pd}\{V_{dre}(m)\}$$
$$+K_{id}\{V_{dre}(m) - V_{dre}(m-1)\} \tag{4}$$

B. Source Current Estimation

A method for rejecting quadrature signal DC offset is presented in Figure 1. To remove the input signal from the integrator, it adds the third state variable, x0, with the second state variable, x1.
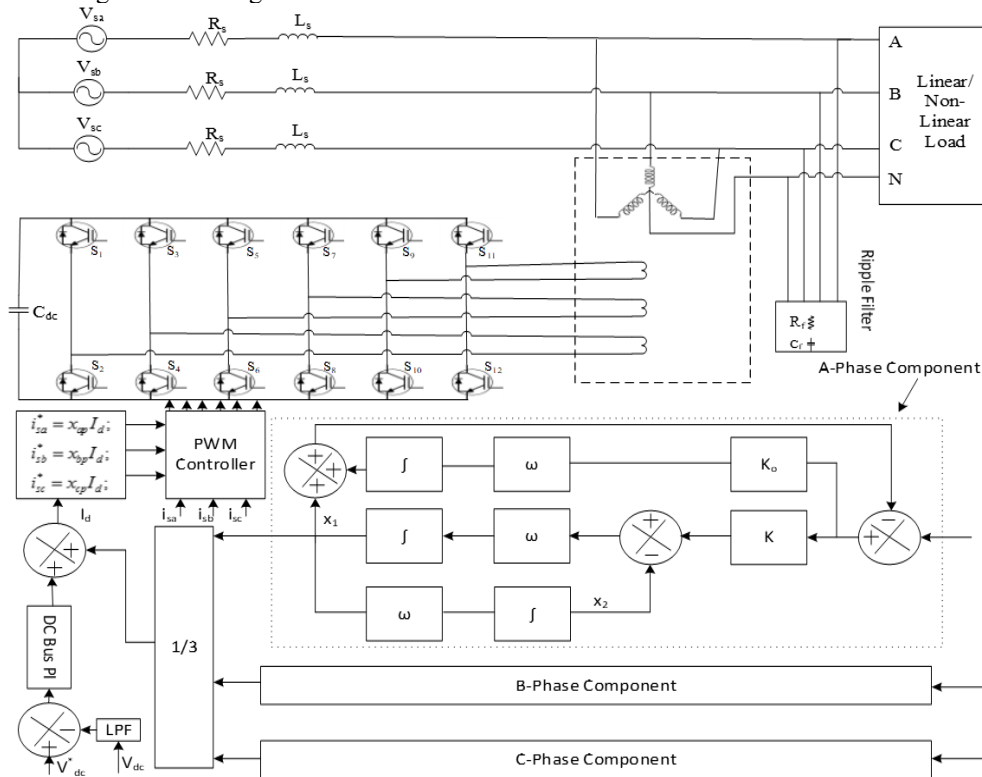

Figure 1. APF power circuit configuration and control algorithm

To reject the quadrature signal's DC off-set, the method proposed in Figure 1 has been developed. To subtract the input signal from the integrator, it adds the third state variable, x0, with the second state variable, x1. Transfer functions for this system include:

$$TF = \frac{X_1(s)}{V(s)} = \frac{w_o s^2 k}{\Delta(s)}; \qquad (5)$$

$$\frac{X_2(s)}{V(s)} = \frac{w_o s^2 k}{\Delta(s)}; \qquad (6)$$

$$\frac{X_o(s)}{V(s)} = \frac{w_o(s^2 + w_o^2)k_o}{\Delta(s)}; \qquad (7)$$

where, $\Delta(s) = s^3 + (k_o + k)w_o s^2 + w_o^2 s + k_o w_o^3$ where $\Delta(jw_o) = -k_o w_o^3$ as a result, it is determined that x1 is a filtered band pass variation of the input signal that does not have a phase shift, whereas x2 is a filtered band pass variation of the input signal that has a 90° phase shift and x0 will be a low-pass/notch-filtered variation of the input signal. So, as far as dc offset is concerned, x1 and x2 have none and x0 is equal to the dc input signal.

An improved single-phase PLL with dq-based single-phase OSG, shown in Figure 1, can be employed to correct this problem.

It is possible to extract the fundamental power component of phase 'a' source current from Figure 1 and similarly for phase 'b' and source phase 'c' components are extracted.

The average value of current is estimated as:

$$I_{davg} = \frac{(I_{dsa} + I_{dsb} + I_{dsc})}{3} \qquad (8)$$

The average values of individual phase components is added to loss component of current.

$$I_d = I_{davg} + I_{lss} \qquad (9)$$

Active power filter reference source currents are estimated as:

$$i_{sa}^* = x_{ap}I_d; i_{sb}^* = x_{bp}I_d; i_{sc}^* = x_{cp}I_d; \qquad (10)$$

In order to measure the error currents for the 6-leg VSC, reference currents are compared with the estimated currents. This type of gate generation uses a triangle wave signal to create unipolar pulses.

$i_{ea}>i_{tr}$ (left leg phase 'a' upper switching device is activated);
$i_{ea}< i_{tr}$ (left leg phase 'a' lower switching device is activated);
$-i_{ea}>i_{tr}$ (right leg phase 'a' upper switching device is activated);
$-i_{ea}\leq i_{tr}$ (right leg phase 'a' lower switching device is activated).

In a similar manner, the other two H-bridge VSCs in the last phase of the system change their operating mode when the PWM switching frequency is doubled and the filter requirement is reduced.

C. Computation of PI Controller Gains

The DC and AC PI controller gains constants obtained using the Ziegler–Nichols step response technique. A step input of amplitude (U) is applied and the output response of the dc bus voltage is obtained for the open-loop system. The maximum gradient (G) and the point at which the line of maximum gradient crosses the time axis (T) are computed. The gains of the controller are computed using the following equations:

$$K_p = |1.2U / GT| \qquad (11)$$

$$K_p = |0.6U / GT^2| \qquad (12)$$

The gain values for both the DC and AC PI controllers are computed and are given in the Appendix.

4. RESULTS AND DISCUSSION

These Figures 2 and 3 show the performance of OSG control algorithm for Active Power Filter (APF) with six legs. In addition to power factor correction, harmonic suppression and neutral current compensation, the MATLAB simulation results of the proposed APF are shown.

A. Performance of the OSG algorithm based Active Power Filter with linear loads

A 6-leg VSC-based Active Power Filter with linear loads performance parameters are depicted in Figure 2. In Figure 2, variations in the source voltages (v_{source}), source currents (I_{source}), compensator currents (I_{comp}), load currents (I_{load}), dc bus voltage (v_{dc}), compensator neutral current (I_{cn}) and source neutral current (I_{sn}) between t=1.15 sec to 1.4 sec are observed. To begin with, one phase of the load is detached for 1.2 sec before reapplying it for 1.35 sec. Source voltages (v_{source}) and source currents (I_{source}) are reported to have the same power factor under a variety of load circumstances. harmonic-free and balanced changes in the source voltages (v_{source}) and source currents (I_{source}) are observed. Active Power Filter using star/three I-Ø transformers compensate the unbalanced load neutral current, while the source neutral current (I_{sn}) is zero. As a result of this, the DC bus voltage (v_{dc}) is kept constant at 400V.

B. Performance of the OSG algorithm based Active Power Filter with non-linear loads

A 6-leg VSC-based Active Power Filter with non-linear loads performance parameters are depicted in Figure 3. In Figure 3, variations in the source voltages (v_{source}), source currents (I_{source}), compensator currents (I_{comp}), load currents (I_{load}), dc bus voltage (vdc), compensator neutral current (I_{cn}) and source neutral current (I_{sn}) between t=1.15 sec to 1.4 sec are observed. To begin with, one phase of the load is detached for 1.2 sec before reapplying it for 1.35 sec. Source voltages (v_{source}) and source currents (I_{source}) are reported to have the same power factor under a variety of load circumstances. Harmonic-free and balanced changes in the source voltages (v_{source}) and source currents (I_{source}) are observed. Active Power Filter using star/three I-Ø transformers compensates the unbalanced load neutral current, while the source neutral current (I_{sn}) is zero. As a result of this, the DC bus voltage (v_{dc}) is kept constant at 400V.
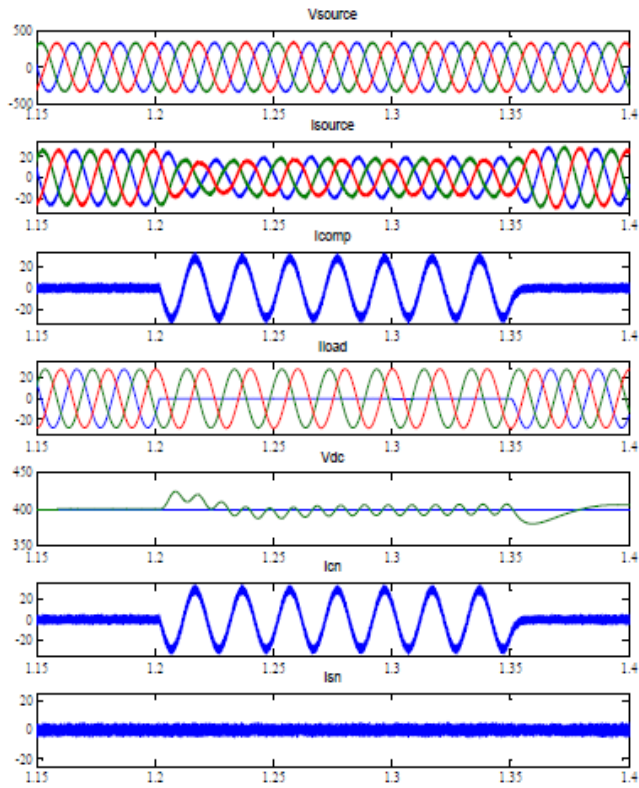
Figure 2. Performance of OSG algorithm based active power filter with linear loads
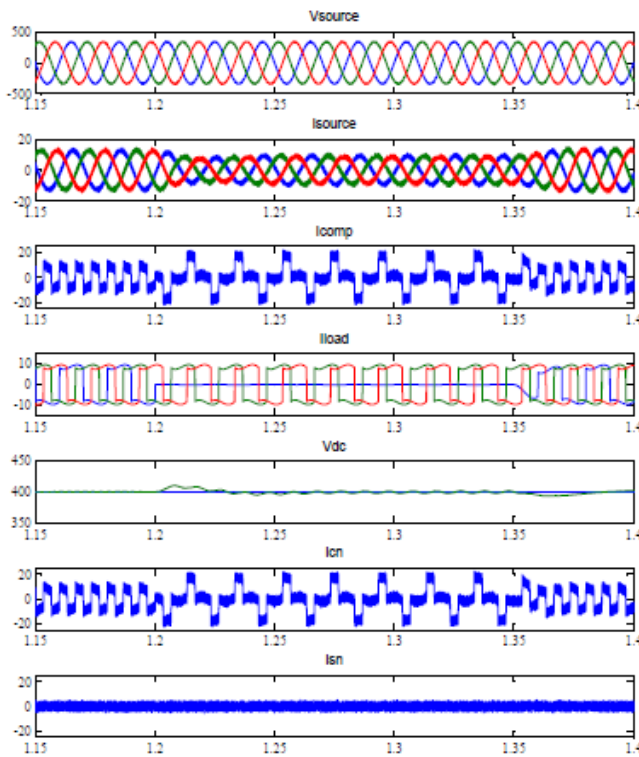

Figure 3. Performance of OSG algorithm based active power filter with non-linear loads

5. CONCLUSION

The dynamic performance of OSG control algorithm for 6-

leg VSC-based Active Power Filter has been satisfactory. Three-phase 4-wire linear/non-linear loads are used for harmonic removal, neutral current regulation, as well as for unity power factor maintenance (While the 3-leg IGBT employs bi-polar switching, the 6-leg IGBT-based VSC uses unipolar switching, which will increase the PWM switching).
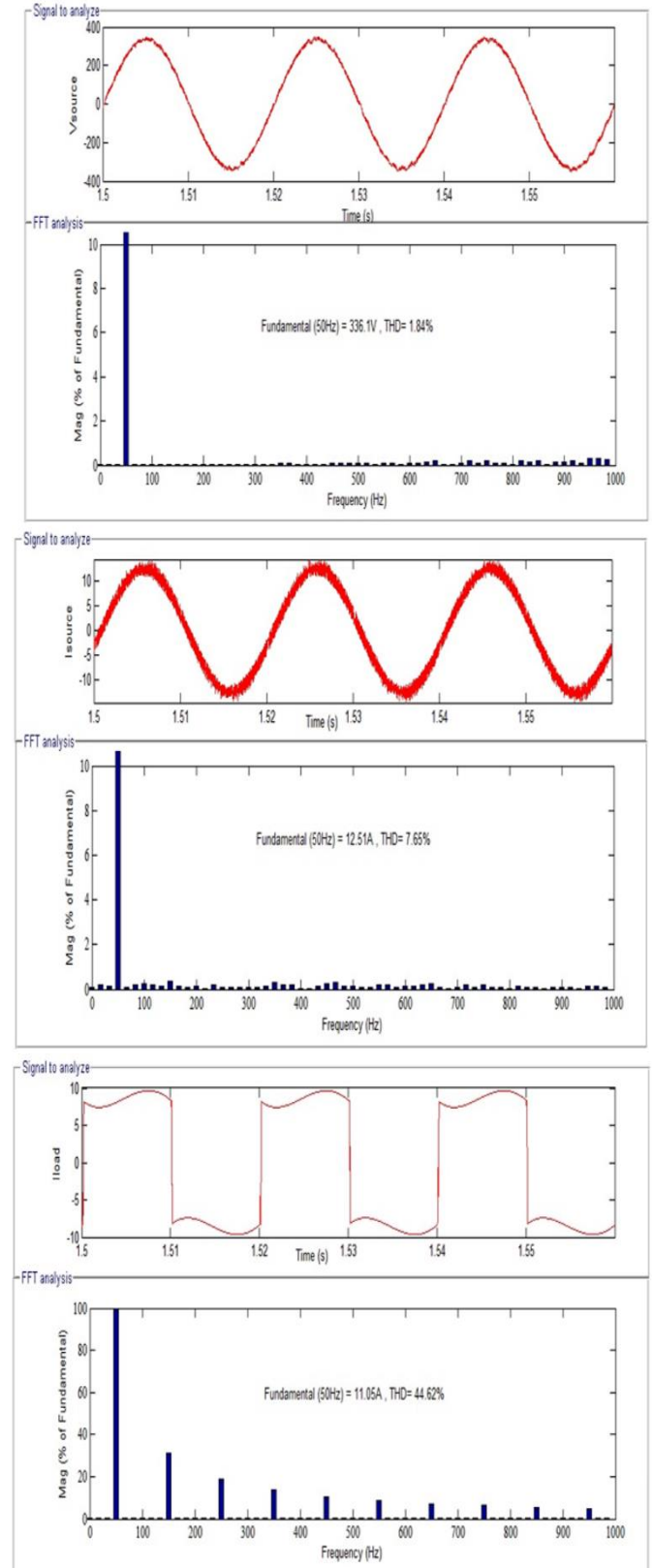

Figure 4. Harmonic spectra of source voltage, source current and load current

The frequency of PWM switching can be increased, decreasing the requirements of the filter and improving performance in the process. The proposed OSG control method for active power filter requires the elimination of the PLL, and it produces source voltages and currents with THD values of 1.84 percent and 7.65 percent respectively are shown in Figure 4, which comply with IEEE-519.

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