European Journal of Electrical Engineering
Vol. 21, No. 2, April, 2019, pp. 199-206
Journal homepage: http://iieta.org/journals/ejee

A Novel Switched Capacitor Boost Derived Multilevel Hybrid Converter Modeling and Analysis

Segaran Jeyasudha*, Balakrishnan Geethalakshmi

Department of Electrical and Electronics Engineering, Pondicherry Engineering College, Pondicherry Central University, Puducherry, India

Corresponding Author Email: jeyasudha_s@pec.edu

https://doi.org/10.18280/ejee.210211

Received: 12 January 2019
Accepted: 9 March 2019

Keywords:
boost converter, boost derived hybrid converter, multilevel inverter, switched capacitor converter, PI controller

ABSTRACT

This paper investigates a novel high gain low power converter called switched capacitor boost derived multilevel hybrid converter (SCBDMHC) which produces dc and multilevel ac outputs simultaneously for solar PV application. The mathematical modelling of the SCBDMHC is derived using state space analysis and verified with the simulated results. A closed loop control scheme of the circuit is implemented by the PI control logic. The robustness of the converter is tested with source variation, load variation and reference variation. The simulation results prove that the SCBDMHC produces the higher ac gain which is $\frac{2-\delta}{1-\delta}$ times more than the conventional MLI. So this SCBDMHC may implement for the high gain converter of the solar PV system.

1. INTRODUCTION

The solar photovoltaic system is a promising and predominant system among all the renewable energy sources [1]. The low output voltage provided by the SPV system has to be boosted and inverted for dc and ac applications respectively [2]. The output of a single voltage source inverter is not adequate for medium and high power applications as it depends on the amplitude of the input source voltage. For such applications, VSI is cascaded as a multilevel inverter [3] and solar photovoltaic-based cascaded multilevel inverter is a serious research in the recent days. Compared to neural point clamped MLI and flying capacitor MLI, the cascaded configuration uses lesser number of devices for an increase in number of levels [4-5]. Nowadays researchers mainly focus on the design of reduced switch cascaded MLI [6] and hybrid MLI [7] topologies to extract the higher number of output voltage levels. Boost derived multilevel hybrid converter is one of the hybrid MLI proposed in [8] which produces multilevel ac output along with dc output. It is formed by cascading two or more BDHC [9]. A switched capacitor (SC) cell is connected in front of the BDHC is called as SCBDHC. For achieving higher ac gain in the multilevel configuration, SCBDHC units are connected serially and the configuration is referred as switched capacitor boost derived multilevel hybrid converter (SCBDMHC).

The SCBDMHC is a triple output and single input converter, which produces multilevel ac output and two boosted dc outputs simultaneously. This paper explains the proposed circuit configuration, its modes of operation, dynamic model and the closed loop control scheme. The robustness of the SCBDMHC is verified with load, line and reference variation.

This paper is structured into seven sections. Section 2 describes the circuit operation while Section 3 focuses on switching strategy. Section 4 explains the dynamic model of the converter and Section 5 presents closed loop PI controller design. The simulated results are explained in Section 6. Section 7 provides a fair summing of all the Sections.

2. PROPOSED CONVERTER - SCBDMHC

2.1 Circuit configuration

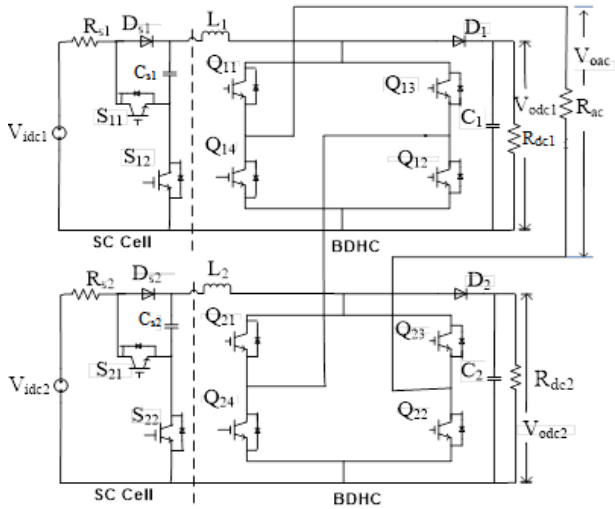


Figure 1. Proposed SCBDMHC circuit

In the configuration of the proposed converter depicted in Figure 1, two SCBDHC units are connected in series to produce the five level ac output and separate dc outputs simultaneously. The switched capacitor cell has two switches S_{11} and S_{12}, a capacitor $C_{s1,}$ a diode D_{s1} and a source resistor R_{s1} for first level circuit. The input sources V_{idc1} and V_{idc2}, bridge network switches Q_{11} to Q_{14}, Q_{21} to Q_{24} and SC cell switches S_{11}, S_{12}, S_{21}, and S_{22} are operated for both ac and dc operations. In the conventional multilevel inverter, the output

phase voltage is the sum of the input voltages where as in the proposed SCBDMHC, as the input voltages are boosted by the switched capacitor cell which present in the input side, the output phase voltage is the boosted sum of the input voltages. Besides, each bridge along with the switched capacitor circuit produces separate boosted dc output along with the multilevel ac output.

2.2 Modes of operation

The circuit is operated with two modes: boosting mode and inverting mode.

2.2.1 Boosting mode

Boosting mode is a high frequency switching mode, which is further divided into shoot-through interval mode ($0 < t < \delta T$) and power interval mode ($\delta T < t < (1-\delta)\ T$) where δ is the duty ratio. When the same leg of switches Q_{11}, Q_{14} and the SC cell switch S_{12} are ON as shown in the Figure 2, the converter operates in shoot-through interval mode and when the switches Q_{11}, Q_{12} and S_{11} are ON as shown in the Figure 3, the converter operates in power interval mode. During shoot-through interval, the capacitors C_{s1} and C_{s2} get charged and the inductors L_1 and L_2 store energy from the source. The diode D_1 and D_2 get reverse biased. Hence no current flows from source to dc load as well as ac load. During the power interval mode, the source current is divided and flowing through the dc and ac loads.

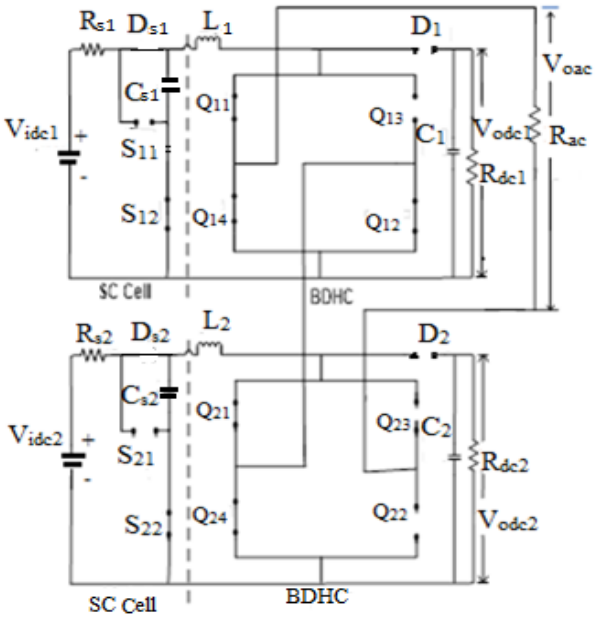


Figure 2. Shoot-through interval mode of SCBDMHC

2.2.2 Inverting mode

The inverting mode is a low frequency switching mode. This mode is further divided into level 1 and level 2 intervals. During level 1 interval, the switches Q_{11}, Q_{12} and Q_{21} conduct and the first input source V_{idc1} connects with the ac load, which provides three level output across R_{ac}. During level 2 interval, the switches Q_{11}, Q_{12}, Q_{21} and Q_{22} conduct and the input sources V_{idc1} and V_{idc2} connect with the ac load, which provides five level output across R_{ac}. Each phase level internally consists of boosting operation.

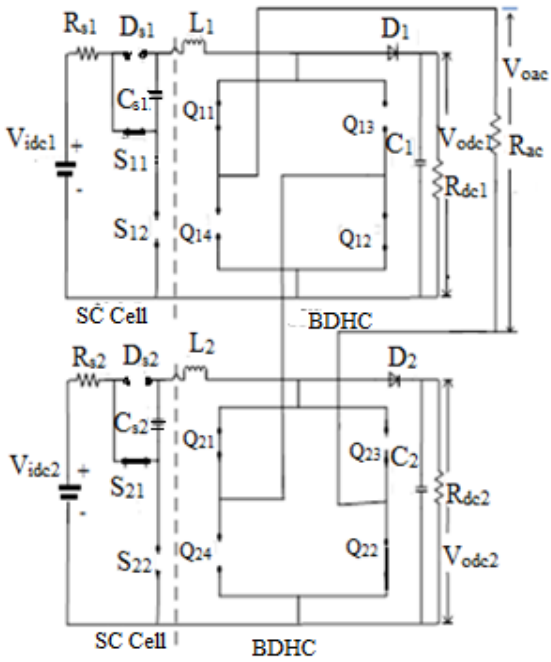


Figure 3. Power interval mode of SCBDMHC

2.3 Output voltages of SCBDMHC

In SCBDMHC, identical elements in each cell are assumed to have same values, for e.g. $L_1 = L_2$, $R_{dc1} = R_{dc2}$ *etc.* The number of voltage levels (m) in the phase voltage of SCBDMHC is *m*=(2N+1), where N is the number of SCBDHC units. The SCBDMHC dc output voltage of each cell is given in the equation (1):

$$V_{odc1}(t) = \frac{(2-\delta)V_{idc1}(t)}{1-\delta}\ ;\ V_{odc2}(t) = \frac{(2-\delta)V_{idc2}(t)}{1-\delta} \qquad (1)$$

The five level SCBDMHC ac peak output voltage is given in the equation (2):

$$v_{oac}(t) = \frac{(2-\delta)V_{idc1}(t)}{1-\delta} + \frac{(2-\delta)V_{idc2}(t)}{1-\delta} \qquad (2)$$

In general, it is expressed as:

$$v_{oac}(t) = \sum_{m=1}^{N} \frac{(2-\delta)V_{idcm}(t)}{1-\delta} = \sum_{m=1}^{N} V_{odcm}(t) \qquad (3)$$

From the equations (1) to (3), it is understood that the dc and ac outputs of SCBDMHC is controlled by the duty cycle δ and the ac peak voltage depends on the dc output voltage.

3. SWITCHING STRATEGY

The switching sequence adopted for the SCBDMHC is tabulated in the Table 1. The reference voltage is a sinusoidal waveform with the frequency f_0 and the amplitude m_a, called modulation index. For SCBDMHC the m_a has the range of $0 < m_a < 0.5$. The output phase voltage has its fundamental component $v_f(t)$ at f_0 and can be expressed as in (4):

$$v_f(t) = m_a N V_{idc}\ sin(2\pi f_0 t) \qquad (4)$$

Table 1. Switching sequence of SCBDMHC

		Switching sequences								AC Output Voltage
		Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{21}	Q_{22}	Q_{23}	Q_{24}	V_{oac}
Positive Half	0	B	0	0	B	B	0	0	B	0V
	1	1	1	0	B	1	B	0	B	$\frac{(2-\delta)V_{idc1}}{1-\delta}$
	2	1	1	0	B	1	1	0	B	$\frac{(V_{idc1}+V_{idc2})(2-\delta)}{1-\delta}$
Negative Half	0	0	B	B	0	0	B	B	0	0V
	1	0	B	1	1	0	B	1	0	$\frac{-(2-\delta)V_{idc1}}{1-\delta}$
	2	0	B	1	1	0	B	1	1	$\frac{-(V_{idc1}+V_{idc2})(2-\delta)}{1-\delta}$

(B- High frequency boosting condition, 1-ON condition, 0- OFF condition)

This reference signal is compared with the two dc constants V_{a1}, V_{a2} as shown in the Figure 4 to control the level of the SCBDMHC. A triangular carrier pulse V_{tri} is compared with a dc signal $V_{d,}$ as shown in Figure 5, which controls the boosting period of SCBDMHC. The signals so generated separately for inverter operation and boost operation are logically added as shown in the Figure 6, and the appropriate gate pulses G_{11} to G_{14} and G_{21} to G_{24} are produced.

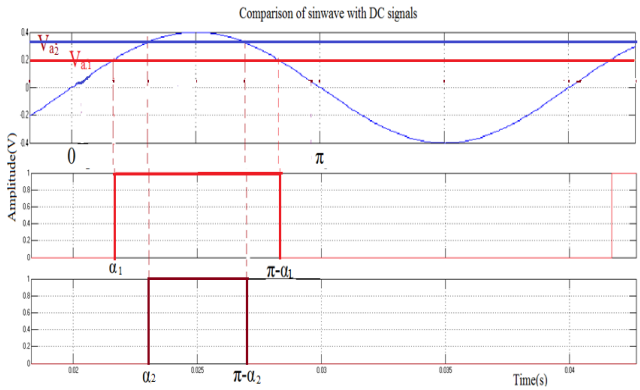


Figure 4. Generation of pulses for inverting operation of SCBDMHC

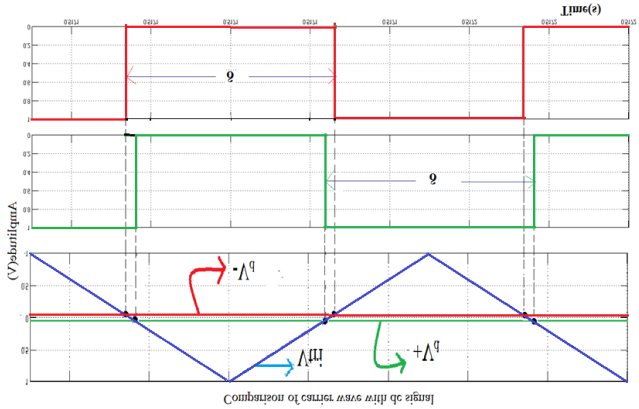


Figure 5. Generation of pulses for boosting operation of SCBDMHC

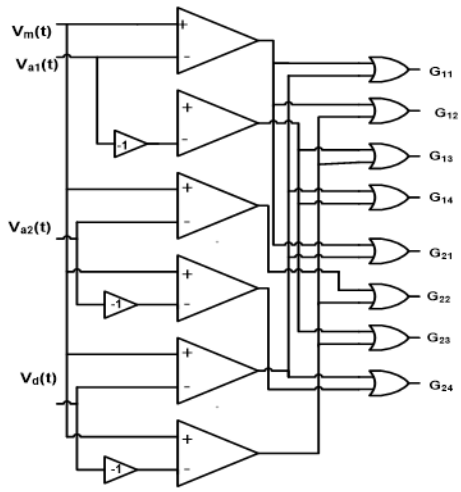


Figure 6. Logic diagram for gate pulses of SCBDMHC

4. DYNAMIC MODEL OF SCBDMHC

4.1 Mathematical modeling of the SCBDMHC

4.1.1 Level1 equations

The dynamic model of the SCBDMHC is derived to develop the transfer function of the system. Level 1 represents the first source that is connected with the ac load by operating the corresponding switches as given in the Table 1. The shoot-through interval mode and power interval mode dynamic equations are derived by applying the KVL and KCL, and are described in (5) to (8):

During shoot-through interval $(0 < t < \delta T)$

$$C_{s1}\frac{dv_{cs1}(t)}{dt} = \frac{V_{idc1}(t)}{R_{s1}} - \frac{v_{cs1}(t)}{R_{s1}} - i_{L1}(t)$$
$$C_{s2}\frac{dv_{cs2}(t)}{dt} = \frac{V_{idc2}(t)}{R_{s2}} - \frac{v_{cs2}(t)}{R_{s2}} - i_{L2}(t),$$
$$L_1\frac{diL_1(t)}{dt} = v_{cs1}(t),\ L_2\frac{diL_2(t)}{dt} = v_{cs2}(t)$$
$$C_1\frac{dv_{odc1}(t)}{dt} = -\frac{V_{odc1}(t)}{R_{dc1}},\ C_2\frac{dV_{odc2}(t)}{dt} = -\frac{V_{odc2}(t)}{R_{dc2}} \quad (5)$$

During power interval $(\delta T < t < (1-\delta)T)$

$$C_{s1}\frac{dv_{cs1}(t)}{dt} = i_{L1}(t),\ C_{s2}\frac{dv_{cs2(t)}}{dt} = i_{L2}(t),$$
$$L_1\frac{di_{L1}(t)}{dt} = V_{idc1}(t) + v_{cs1}(t) - V_{odc1}(t)$$
$$L_2\frac{diL_2(t)}{dt} = V_{idc2}(t) + v_{cs2}(t) - V_{odc2}(t)$$
$$C_1\frac{dV_{odc1}(t)}{dt} = i_{L1}(t) - i_{ac}(t) - \frac{V_{odc1}(t)}{R_{dc1}}$$
$$C_2\frac{dV_{odc2}(t)}{dt} = i_{L2}(t) - i_{ac}(t) - \frac{V_{odc2}(t)}{R_{dc2}} \quad (6)$$

where i_{L1}, i_{L2} are the input current through the inductor L_1 and L_2 respectively. The inverter side equation is given in (7):

$$L_1 \frac{di_{ac}(t)}{dt} = V_{idc1}(t) + v_{cs1}(t) - R_{ac} i_{ac}(t) \qquad (7)$$

4.1.2 Level 2 equations

For the level 2, the boosting mode equations are similar as in the equations (5) and (6), the inverting side equation is given in (8):

$$V_{idc1}(t) + V_{idc2}(t) + v_{cs1}(t) + v_{cs2}(t) - R_{ac} i_{ac}(t) \qquad (8)$$

4.2 State-space representation

The system descriptive equations (5) to (8) are rearranged in the form of state equations. The level 1 averaged state equation is given in (9). Similarly the level 2 state and output equations are given in (10) and (11) respectively. In general, the level n state and output equations for SCBDMHC are given in the equations (12) and (13) respectively.

$$(L_1 + L_2)\frac{di_{ac}(t)}{dt} =$$

$$\begin{pmatrix} \frac{dv_{cs1}}{dt} \\ \frac{dv_{cs2}}{dt} \\ \frac{diL_1}{dt} \\ \frac{diL_2}{dt} \\ \frac{dV_{odc1}}{dt} \\ \frac{dV_{odc2}}{dt} \\ \frac{di_{ac}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-\delta}{R_{s1}C_{s1}} & 0 & \frac{1-2\delta}{C_{s1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-\delta}{R_{s2}C_{s2}} & 0 & \frac{1-2\delta}{C_{s2}} & 0 & 0 & 0 \\ \frac{1}{L_1} & 0 & 0 & 0 & \frac{-(1-\delta)}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 & 0 & \frac{-(1-\delta)}{L_2} & 0 \\ 0 & 0 & \frac{(1-\delta)}{C_1} & 0 & \frac{-1}{C_1 R_{dc1}} & 0 & -\frac{(1-\delta)}{C_1} \\ 0 & 0 & 0 & \frac{(1-\delta)}{C_2} & 0 & \frac{-1}{C_2 R_{dc2}} & -\frac{(1-\delta)}{C_1} \\ \frac{(1-\delta)}{L_1} & 0 & 0 & 0 & 0 & 0 & \frac{-(1-\delta)R_{ac}}{L_1} \end{pmatrix} \begin{pmatrix} v_{cs1} \\ v_{cs2} \\ i_{L1} \\ i_{L2} \\ V_{odc1} \\ V_{odc2} \\ i_{ac} \end{pmatrix} + \begin{pmatrix} \frac{\delta}{R_{s1}C_{s1}} & 0 \\ 0 & \frac{\delta}{R_{s2}C_{s2}} \\ \frac{(1-\delta)}{L_1} & 0 \\ 0 & \frac{(1-\delta)}{L_2} \\ 0 & 0 \\ 0 & 0 \\ \frac{(1-\delta)}{L_1} & 0 \end{pmatrix} \begin{pmatrix} V_{idc1} \\ V_{idc2} \end{pmatrix} \qquad (9)$$

$$\begin{pmatrix} \frac{dv_{cs1}}{dt} \\ \frac{dv_{cs2}}{dt} \\ \frac{diL_1}{dt} \\ \frac{diL_2}{dt} \\ \frac{dV_{odc1}}{dt} \\ \frac{dV_{odc2}}{dt} \\ \frac{di_{ac}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-\delta}{R_{s1}C_{s1}} & 0 & \frac{1-2\delta}{C_{s1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-\delta}{R_{s2}C_{s2}} & 0 & \frac{1-2\delta}{C_{s2}} & 0 & 0 & 0 \\ \frac{1}{L_1} & 0 & 0 & 0 & \frac{-(1-\delta)}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 & 0 & \frac{-(1-\delta)}{L_2} & 0 \\ 0 & 0 & \frac{(1-\delta)}{C_1} & 0 & \frac{-1}{C_1 R_{dc1}} & 0 & \frac{-(1-\delta)}{C_1} \\ 0 & 0 & 0 & \frac{(1-\delta)}{C_2} & 0 & \frac{-1}{C_2 R_{dc2}} & \frac{-(1-\delta)}{C_1} \\ \frac{(1-\delta)}{L_1+L_2} & 0 & 0 & 0 & 0 & 0 & \frac{-(1-\delta)R_{ac}}{L_1+L_2} \end{pmatrix} \begin{pmatrix} v_{cs1} \\ v_{cs2} \\ i_{L1} \\ i_{L2} \\ V_{odc1} \\ V_{odc2} \\ i_{ac} \end{pmatrix} + \begin{pmatrix} \frac{\delta}{R_{s1}C_{s1}} & 0 \\ 0 & \frac{\delta}{R_{s2}C_{s2}} \\ \frac{(1-\delta)}{L_1} & 0 \\ 0 & \frac{(1-\delta)}{L_2} \\ 0 & 0 \\ 0 & 0 \\ \frac{(1-\delta)}{L_1+L_2} & \frac{(1-\delta)}{L_1+L_2} \end{pmatrix} \begin{pmatrix} V_{idc1} \\ V_{idc2} \end{pmatrix} \qquad (10)$$

$$y(t) = \begin{pmatrix} 1 & 1 & 0 & 0 & 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} v_{cs1} \\ v_{cs2} \\ i_{L1} \\ i_{L2} \\ V_{odc1} \\ V_{odc2} \\ i_{ac} \end{pmatrix} \qquad (11)$$

$$\begin{pmatrix} \frac{dv_{cs1}}{dt} \\ \frac{dv_{cs2}}{dt} \\ \vdots \\ \frac{dv_{csn}}{dt} \\ \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \vdots \\ \frac{diL_n}{dt} \\ \frac{dV_{odc1}}{dt} \\ \frac{dV_{odc2}}{dt} \\ \vdots \\ \frac{dV_{odcn}}{dt} \\ \frac{di_{ac}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-\delta}{R_{s1}C_{s1}} & 0 & \frac{1-2\delta}{C_{s1}} & 0 & 0 & 0 & 0 & \dots & 0 \\ 0 & \frac{-\delta}{R_{s2}C_{s2}} & 0 & \frac{1-2\delta}{C_{s2}} & 0 & 0 & 0 & \dots & 0 \\ 0 & 0 & \ddots & \vdots & \ddots & \vdots & 0 & \dots & \vdots \\ 0 & 0 & \dots & \frac{-\delta}{R_{s2}C_{sn}} & \dots & \frac{1-2\delta}{C_{sn}} & 0 & \dots & 0 \\ \frac{1}{L_1} & 0 & 0 & 0 & \frac{-(1-\delta)}{L_1} & 0 & 0 & \dots & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 & 0 & \frac{-(1-\delta)}{L_1} & 0 & \dots & 0 \\ 0 & 0 & \ddots & \vdots & 0 & 0 & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & \frac{1}{L_n} & 0 & 0 & \dots & \frac{-(1-\delta)}{L_n} & 0 \\ 0 & 0 & \frac{(1-\delta)}{C_1} & 0 & \frac{-1}{C_1 R_{dc1}} & 0 & 0 & 0 & \frac{-(1-\delta)}{C_1} \\ 0 & 0 & 0 & \frac{(1-\delta)}{C_2} & 0 & \frac{-1}{C_2 R_{dc2}} & 0 & 0 & \frac{-(1-\delta)}{C_2} \\ 0 & 0 & 0 & 0 & \ddots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \dots & \frac{(1-\delta)}{C_n} & \dots & \frac{-1}{C_n R_{dcn}} & \frac{(1-\delta)}{C_n} \\ \frac{(1-\delta)}{L_1+L_2+\dots+L_n} & 0 & 0 & 0 & 0 & 0 & 0 & \dots & \frac{-(1-\delta)R_{ac}}{L_1+L_2+\dots+L_n} \end{pmatrix}$$

$$\times \begin{pmatrix} v_{cs1} \\ v_{cs2} \\ \vdots \\ v_{csn} \\ i_{L1} \\ i_{L2} \\ \vdots \\ i_{Ln} \\ V_{odc1} \\ V_{odc2} \\ \vdots \\ V_{odcn} \\ i_{ac} \end{pmatrix} + \begin{pmatrix} \frac{\delta}{R_{s1}C_{s1}} & 0 & \dots & 0 \\ 0 & \frac{\delta}{R_{s2}C_{s2}} & \dots & 0 \\ 0 & 0 & \ddots & \vdots \\ 0 & 0 & \dots & \frac{\delta}{R_{s2}C_{s2}} \\ \frac{(1-\delta)}{L_1} & 0 & \dots & 0 \\ 0 & \frac{(1-\delta)}{L_1} & \dots & 0 \\ 0 & 0 & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{(1-\delta)}{L_1} \\ 0 & 0 & \dots & 0 \\ 0 & 0 & \dots & 0 \\ 0 & 0 & \ddots & \vdots \\ 0 & 0 & \dots & 0 \\ \frac{(1-\delta)}{L_1+L_2+\cdots+L_n} & \frac{(1-\delta)}{L_1+L_2+\cdots+L_n} & \dots & \frac{(1-\delta)}{L_1+L_2+\cdots+L_n} \end{pmatrix} \begin{pmatrix} V_{idc1} \\ V_{idc2} \\ \vdots \\ V_{idcn} \end{pmatrix} \tag{12}$$

$$(t) = (1 \ \cdots \ 1 \ \ 0 \cdots \ 0 \ \ 1 \cdots \ 1 \ \ 0) \begin{pmatrix} v_{cs1} \\ v_{cs2} \\ \vdots \\ v_{csn} \\ i_{L1} \\ i_{L2} \\ \vdots \\ i_{Ln} \\ V_{odc1} \\ V_{odc2} \\ \vdots \\ V_{odcn} \\ i_{ac} \end{pmatrix} \tag{13}$$

Linearizing (5) to (8) by adding the small perturbation in the input, output and state variables, around the equilibrium point and separating the dynamic ac small signal terms from the dc steady state component as in [10], the following dynamic model (14) is obtained:

$$\dot{x}(t) = A\hat{x}(t) + B\hat{u}(t) + E\hat{\delta}(t) \tag{14}$$

where the state matrix A and the input matrix B are given in (10). E matrix corresponding to $\hat{\delta}(t)$, $\hat{x}(t)$ and $\hat{u}(t)$ are given in (15):

$$E = \begin{pmatrix} \frac{V_{idc1} - V_{cs1}}{R_{s1}C_{s1}} - \frac{2I_{L1}}{C_{s1}} \\ \frac{V_{idc2} - V_{cs2}}{R_{s2}C_{s2}} - \frac{2I_{L2}}{C_{s2}} \\ -\frac{V_{idc1}}{L1} + \frac{V_{odc1}}{L1} \\ -\frac{V_{idc2}}{L2} + \frac{V_{odc2}}{L2} \\ \frac{-I_{L1} + I_{ac}}{C_1} \\ \frac{-I_{L2} + I_{ac}}{C_2} \\ \frac{-V_{idc1} - V_{idc2} - V_{cs1} - V_{cs2} + R_{ac}I_{ac}}{L_1 + L_2} \end{pmatrix} \hat{x}(t) = \begin{pmatrix} \hat{v}_{cs1} \\ \hat{v}_{cs2} \\ \hat{\imath}_{L1} \\ \hat{\imath}_{L2} \\ \hat{v}_{odc1} \\ \hat{v}_{odc2} \\ \hat{\imath}_{ac} \end{pmatrix}$$

$$\hat{u}(t) = \begin{pmatrix} \hat{v}_{idc1} \\ \hat{v}_{idc2} \end{pmatrix} \tag{15}$$

4.3 Numerical validation

The parameters considered for the simulation of SCBDMHC are specified in Table 2. These values are substituted in the equation (10) and the resultant state and input matrices obtained are given in equation (16).

Table 2. Parameters of SCBDMHC

Paraameters	Values
Input Voltage (V_{idc1} and V_{idc_2})	40V
Input Inductor (L_1 and L_2)	5mH
DC Capacitor (C_1 and C_2)	1mF
DC load resistor (R_{dc1} and R_{dc2})	20Ω
AC load resistor (R_{ac})	50Ω
Switching frequency (f)	10KHz
Switched capacitor (C_{s1} and C_{s2})	1mF
Source Resistor (R_{s1} and R_{s2})	0.01 Ω

$$A = \begin{pmatrix} -51000 & 0 & -20 & 0 & 0 & 0 & 0 \\ 0 & -51000 & 0 & -20 & 0 & 0 & 0 \\ 200 & 0 & 0 & 0 & -98 & 0 & 0 \\ 0 & 200 & 0 & 0 & 0 & -98 & 0 \\ 0 & 0 & 490 & 0 & -50 & 0 & -490 \\ 0 & 0 & 0 & 490 & 0 & -50 & -490 \\ 49 & 0 & 0 & 0 & 0 & 0 & -2450 \end{pmatrix}$$

$$B = \begin{pmatrix} 51000 & 0 \\ 0 & 51000 \\ 98 & 0 \\ 0 & 98 \\ 0 & 0 \\ 0 & 0 \\ 98 & 98 \end{pmatrix} \quad U = \begin{pmatrix} 40 \\ 40 \end{pmatrix}$$

$$C = (1 \ \ 1 \ \ 0 \ \ 0 \ \ 1 \ \ 1 \ \ 0), \ D = (0) \tag{16}$$

To solve the state equations, m-file programming in MATLAB is used and the state values obtained is given in equation (17):

$$x(t) = (v_{cs1}(t) \ \ v_{cs2}(t) \ \ i_{L1}(t) \ \ i_{L2}(t) \ \ V_{odc_1}(t) \ \ V_{odc_2}(t) \ \ i_{ac}(t))^T$$

$$x(t) = (39.9936V \quad 39.9936V \quad 16.41A \quad 16.41A \quad 121.6195V \quad 121.6195V \quad 3.9A)^T \qquad (17)$$

In order to validate the developed model of the system, the circuit is simulated using MATLAB/Simulink with the same parameters specified in Table 2. Input voltage is set to 40V with the duty ratio of 0.51 and modulation index of 0.49. The simulated output voltage across the loads and current through the loads observed are depicted in the Figure 7 and Figure 8 respectively. These results are tabulated in the Table 3 and compared with the values obtained from the mathematical model.

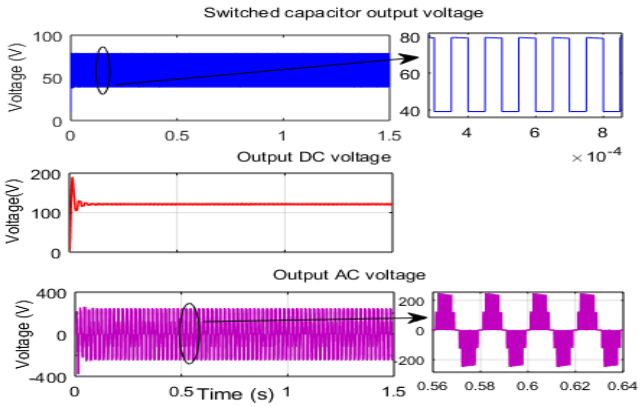


Figure 7. Open loop input and output voltage waveforms

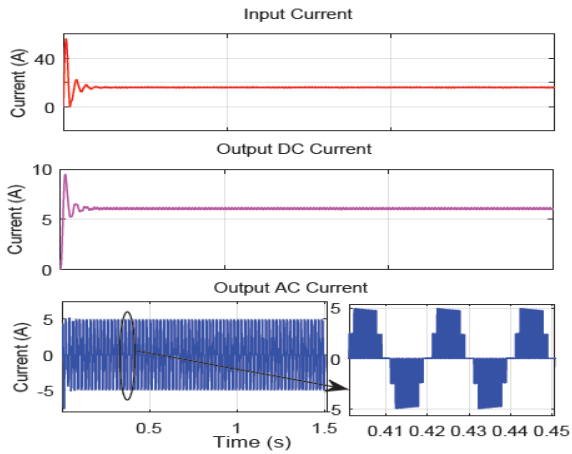


Figure 8. Open loop input and output current waveforms

Table 3. Model validation of SCBDMHC

Parameters	Values	
	Theoretical	Simulated
Output dc voltage (V_{odc1} to V_{odc_2})	121V	121.62 V
Output ac voltage (v_{oac})	195V	179V
Input Current (i_{L1} to i_{L2})	16.4A	17.4 A
Output dc current (i_{dc1} to i_{dc2})	6.08 A	6.0 A
Output ac current (i_{ac})	3.9A	3.54A

From the Figure 7 the output dc voltage is found to be 121.62 V and the ac voltage is 179 V. Similarly from Figure 8 the input current is noted as 17.4 A, the dc output current is 6 A and ac the output current is 3.54 A.

The proposed SCBDMHC output voltage is compared with the conventional MLI. When 40 V dc is supplied as input for the five level multilevel inverter, it produces the ac peak output of 80 V, whereas the five level SCBDMHC, produced the ac output peak voltage of 243 V. This will be $\frac{2-\delta}{1-\delta}$ times higher than the conventional MLI output.

4.4 Transfer function

Using the equations (14) and the Table 2 the dc output voltage to control transfer function (18) is developed.

$$\frac{V_{odc}(s)}{\delta(s)} = \frac{\begin{matrix}-1.25\times10^{4}s^{6}-1.3\times10^{9}s^{5}-3.8\times10^{13}s^{4}\\ -1.48\times10^{17}s^{3}+4.15\times10^{19}s^{2}\\ -4.5\times10^{21}s+2.43\times10^{24}\end{matrix}}{\begin{matrix}s^{7}+104550s^{6}+2.861\times10^{9}s^{5}+\\ 6.668\times10^{12}s^{4}+9.197\times10^{14}s^{3}\\ +6.42\times10^{17}s^{2}+3.727\times10^{19}s+1.47\times10^{22}\end{matrix}} \qquad (18)$$

5. CLOSED LOOP SCHEME OF SCBDMHC

Figure 9 shows the closed loop control scheme of the switched capacitor boost derived multilevel hybrid converter. A part of dc output voltage is fed back from the SCBDMHC and compared with the set point value, and the error occurred is processed by the PI controller [11] whose parameters are tuned using Zeigler Nichols oscillation method. The controller parameters K_p=0.0072 and K_i=5.01 are obtained. The simulation results with the closed loop circuit is discussed in the next section.

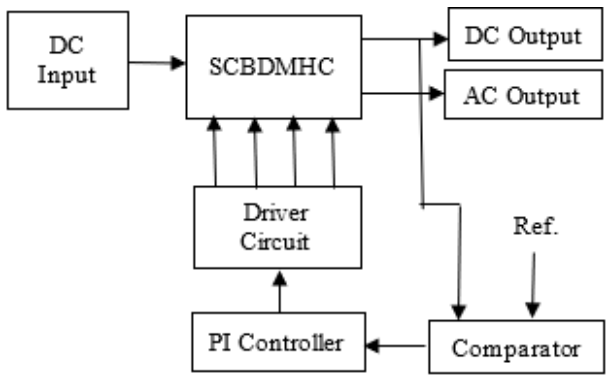


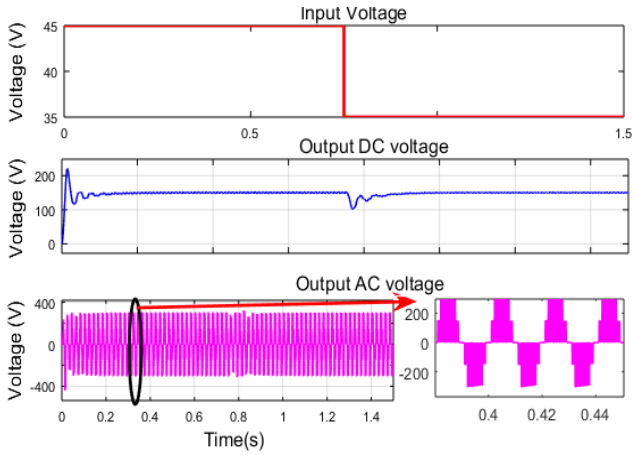
Figure 9. Closed loop scheme of SCBDMHC

6. SIMULATION RESULTS AND ANALYSIS

The closed loop system of the SCBDMHC is tested with line regulation, load regulation and reference variation.

6.1 Line regulation of SCBDMHC

To verify the performance of the controller under supply variations, the load resistance is kept at a fixed value of R_{dc}=20 Ω and R_{ac}=50 Ω, variation is incorporated only in the supply side. The reference voltage across the dc load is set as 150 V. The supply voltage is maintained at 45V until t=0.75s and a step change is given to vary the input voltage to 35 V. The corresponding dc output voltage is regulated to 150 V as depicted in Figure 10. The ac output voltage is also regulated for 230 V as shown in the Figure 6c

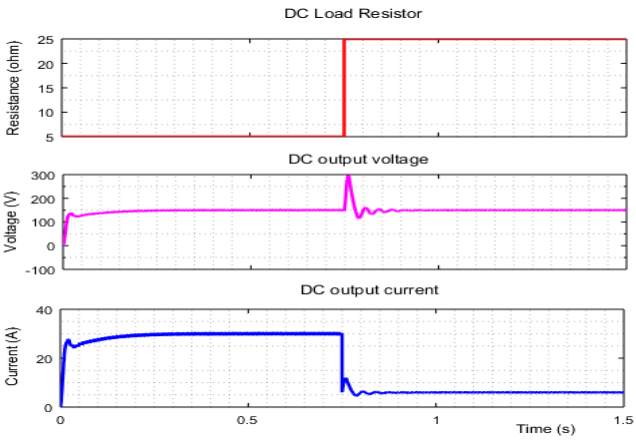


(a) Supply voltage (b) Output dc voltage (c) Output ac voltage

Figure 10. Supply variation - SCBDMHC

6.2 Load regulation of SCBDMHC

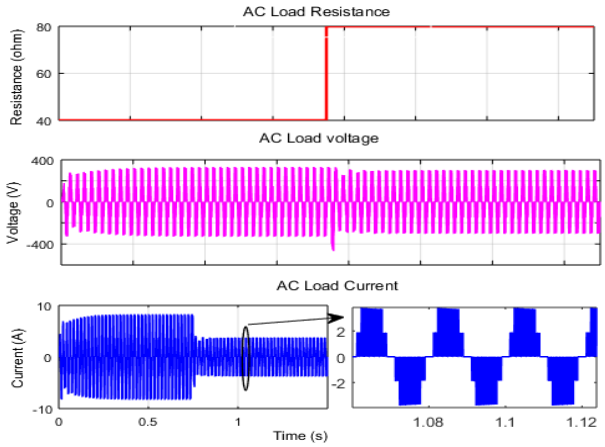
The input voltage is set as 40 V and the reference dc output voltage is at 150 V and ac output voltage is at 230 V. Under this condition, the dc load is varied from 5 Ω to 25 Ω at 0.75 sec as shown in the Figure 11(a).



(a) Load resistance variation (b) DC output voltage (c) DC output current

Figure 11. DC load variation – SCBDMHC

The sudden rise in the load resistance, results in a corresponding peak overshoot to 250V in the output voltage, which gives a significant variation from the desired set value of 150 V. The controller responds instantaneously and adjusts the duty ratio in order to generate an output voltage to the desired set reference value, within a settling time of t_s=0.25 sec as depicted in Figure 11(b). To support this result, the corresponding variation in the load current has also been presented in Figure 11(c) and it decreases from 30 A to 6 A. Similarly, ac load resistance R_{ac} is varied from 40 Ω to 80 Ω at the time t=0.75 sec. For a sudden increase in load, the controller responds effectively and it is observed that the output voltage is maintained constant, irrespective of the change in load providing load regulation as shown in Figure 12(b). The corresponding variation in the load current is presented in Figure 12(c) and it is reduced from 5.75 A to 2.8 A.



(a) AC Load resistance variation (b) AC output voltage (c) AC output curren

Figure 12. AC load variation - SCBDMHC

6.3 Reference variation of SCBDMHC

Here both the input supply voltage and load resistance are maintained constant and the controller performance is verified by varying the reference value. DC input voltage is fixed at 40 V and load resistance values are maintained at R_{dc}=20 Ω and R_{ac}=50 Ω. For dc side, initially, the reference voltage is set at 200V and the reference value is changed to 150 V at t=0.75 sec. Similarly the ac output voltage reference varies from 282.9 V to 212.1 V rms at t=0.75 sec. The dc and ac output voltage waveforms depicted in Figure 13, reveal the controller performance in tracking the respective set reference values.

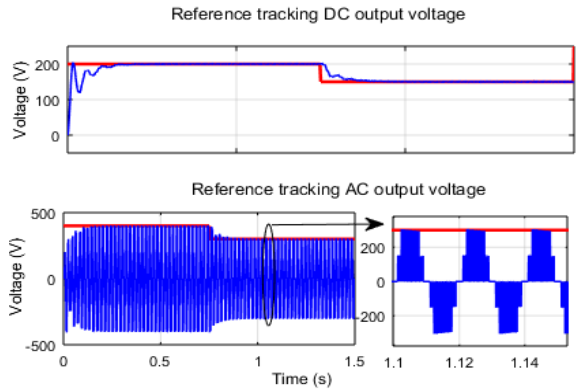


Figure 13. Reference variation - SCBDMHC

7. CONCLUSION

In this paper, a novel switched capacitor boost derived multilevel hybrid converter is proposed which is capable of supplying boosted dc and multilevel ac output simultaneously for SPV application. The state-space modeling equations are derived and validated with the simulated results. A closed loop scheme for the SCBDMHC has been developed and to prove its robustness the system performance is tested with line regulation, load regulation and reference variation. From the results, it is concluded that the SCBDMHC has the higher ac gain which is $\frac{2-\delta}{1-\delta}$ times more than the conventional MLI.

REFERENCES

[1] Pires, V.F., Foito, D., Baptista, F.R.B., Silva, J.F. (2016). A photovoltaic generator system with a DC/DC converter based on an integrated Boost-Ćuk topology. Solar Energy, 136: 1-9.

[2] Li, W.H., He, X.N. (2011). Review of non isolated high-step-up DC/DC converters in photovoltaic grid connected applications. IEEE Transactions on Industrial Electronics, 58(4): 1239-1250. http://dx.doi.org/10.1109/TIE.2010.2049715

[3] Chattopadhyay, S.K., Chakraborty, C. (2014). A new multilevel inverter topology with self-balancing level doubling network. IEEE Transactions on Industrial Electronics, 61(9): 4622-4631. http://dx.doi.org/10.1109/TIE.2013.2290751

[4] Babaei, E., Buccella, C., Saeedifard, M. (2016). Recent advances in multilevel inverters and their applications-part I. IEEE Transactions on Industrial Electronics, 63(11): 7145-7147. http://dx.doi.org/10.1109/TIE.2016.2602270

[5] Du, S., Liu, J., Lin, J., He, Y. (2013). A novel DC voltage control method for STATCOM based on hybrid multilevel H-bridge converter. IEEE Transactions on Power Electronics, 28(1): 101-111. https://doi.org/10.1109/TPEL.2012.2195508

[6] Colak, I., Kabalci, E., Bayindir, R. (2011). Review of multilevel voltage source inverter topologies and control schemes. Energy Conversion and Management, 52(2): 1114-1128. https://doi.org/10.1016/j.enconman.2010.09.006

[7] Hasan, M.M., Abu-Siada, A., Islam, S.M., Dahidah, M.S. (2018). A new cascaded multilevel inverter topology with galvanic isolation. IEEE Transactions on Industry Applications, 54(4): 3463-3472. https://doi.org/10.1109/TIA.2018.2818061

[8] Jeyasudha, S., Geethalakshmi, B. (2017). Modeling and analysis of a novel boost derived multilevel hybrid converter. Energy Procedia, 117: 19-26. https://doi.org/10.1016/j.egypro.2017.05.102

[9] Ray, O., Mishra, S. (2014). Boost-derived hybrid converter with simultaneous DC and AC outputs. IEEE Transactions on Industry Applications, 50(2): 1082-1093. https://doi.org/10.1109/TIA.2013.2271874

[10] Jeyasudha, S., Geethalakshmi, B. (2017). Modeling and control of integrated photovoltaic module and converter systems. Proceedings IEEE Inter. Conf. on Innovations in Power and Advanced Computing Technologies. http://dx.doi.org/10.1109/IPACT.2017.8245044

[11] Ogata, K. (2005). Modern Control Engineering. PHI learning Pvt. Ltd, New Delhi India.

NOMENCLATURE

V_{idc1}, V_{idc2}	Input sources
v(t)	A dc signal
V_1, V_2	dc reference signals for level triggering V
L_1, L_2	Inductors H
m	Number of input phase voltage
m_a	Modulation index
x	State vector matrix
V_{odc}	Output voltage of the DC load V
V_{oac}	Output voltage of the AC load V
Q_{11} to Q_{14}	Bridge network switches for I stage
Q_{21} to Q_{24}	Bridge network switches for II stage
R_{ac}	AC load resistor
R_{dc}	DC load resistor
s	Laplace Transform factor
T	Simulation time period
V_{odc1}, V_{odc3}	Voltage across capacitors C_1 to C_3
$\hat{v}(t)$	Small signal AC variations for V(t)

Greek symbol

δ	Duty ratio

Subscripts

odc	Output dc
oac	Output ac