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A Comprehensive Review of Low Density Parity Check Encoder Techniques

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ABSTRACT

This paper presents a survey on various technologies of low density parity check encoder. LDPC codes are capable to handle high speed communication channel, by reducing attenuation, hazards and efficiently rectifying the linear error correction. Various coding technologies used in new generation communication system, such as turbo code, hamming code, low-density parity check (LDPC) code and Bose–Chaudhuri–Hocquenghem (BHC) code, are widely used in recent communication system. The LDPC has technical remarkable advantages and better performance in high speed communication process compared to turbo code. This paper deals with study of LDPC encoding techniques with various methods of detecting error and its correction. Here classification and performance analysis of LDPC encoding techniques on the basis of resources utilization, systematic, non-systematic approaches and consumer data right etc. have been analyzed in this paper. Apart from above mentioned criteria, this study deals with hardware and software architecture of LDPC encoder in rectification of forward error correction, parallel execution of instruction set. This study and analysis could offer scalability, the future scope of improving the performance of LDPC encoder in all aspects of the next generation communication process. This paper gives overview of various LDPC encoder applications, drawbacks and solution to overcome it.

1. INTRODUCTION

The Low-density parity-check code is widely used in non-cooperative communication but faces more difficulty to be handled in cooperative communication process using existing LDPC encoding techniques. The major research gaps have been identified by an extensive survey carried out on LDPC encoder techniques. Existing LDPC encoder Techniques generate inaccurate bit error rates when it operated in Binary Phase Shift Keying (BPSK) signal over the additive white Gaussian Noise (AWGN) channel and it is requiring more parallel switching operation when LDPC encoder operates in sort code words. it consists of high authenticated data packets in accordance with the LPDC encoder and needs to set threshold parameters. in this situation, the existing LDPC encoding techniques such as turbo code, Hamming code, BHC face technical problems like parallel operation gate switching speed, required more iterations, and low weight code words. Motivation: In recent days more digital payment amount transactions have been made by customers, and 5G communication process has been used in cellular networks and in high security military applications. It requires more authentication, fast processing and long distance parallel communication. Hence LDPC encoder techniques is very useful for next generation communication process and security.

The LDPC code is a linear error correcting code. This code transmits the message in a noisy transmission channel effectively. This course was introduced by Robert G Gallager in his research work. Compared to the decoding process, the LDPC encoding is complex in nature. Since LDPC can offer a reliable data transmission, they have special attention by the researchers in the field of research. The error correcting capability of these codes is exceptionally high. Since there are only a few 1's in the parity check matrix in comparison to the number of 0's, they are called Low-Density Parity-Check codes. LDPC encoding process is carried out with the creation of a parity check matrix. This matrix should be a sparse matrix with predetermined value of columns and rows which depends on the code word size and employed code rate respectively. The complete binary data vector, upon multiplication, with a generator matrix (obtained from parity check matrix) gives the encoded data sequence [1]. The encoding process of LDPC block diagram is shown in Figure 1. The LDPC codes are flexible in nature and have lower decoding complexity in comparison to the turbo codes. Hardware implementation is made possible because of the parallel capability of the codes. The throughput is high which allows faster decoding. In the prior art, several methods and algorithms have been proposed in order to minimize the number of ones in the parity check matrix, such as lower triangular method, straight forward method and modified lower triangular method [2-6]. Two different methods are available to symbolize the LDPC codes: Matrix method and graphical representation.

The LDPC codes have many advantages, of which the important ones include lower complexity in process of iterative decoding and lacking of low weight code. The codes which are low weight are avoided in a straightforward manner and it also helps in reduction of bit error rates. The concept of

parity check trellis graph is used by these codes. Some of the LDPC codes are regular in nature. This classification is made based on weight on H matrix. The matrix H in regular LDPC codes having identical column and row weight. However, in an irregular LDPC code, the weight of column and row of matrix are different. Similarly non-binary and binary is another method of classification of the LDPC code. This classification is made according to the elements present in the H matrix. The binary LDPC quotes are formed by using 1 and 0, whereas a non-binary LDPC code is formed from the finite q elements ($GF(q)$) where $q=2p$ for some integer$p$.

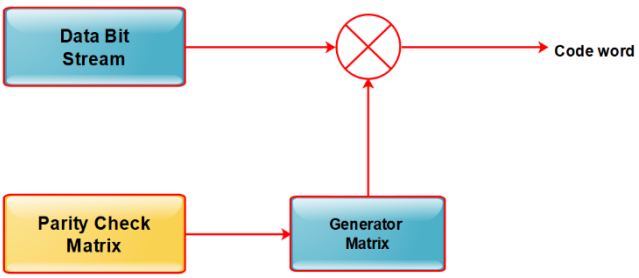

Figure 1. Basic LDPC encoder block diagram

2. LITERATURE SURVEY

The authors [7] have presented different approaches to perform search and optimization of the codes using their sparse parity check matrices. The method incorporates replacing the non-zero elements of h matrix by circulating the elements in a GF (2 m) finite field, and obtaining the LDPC block codes and Quasi cyclic BPC block codes. To compare the Quasi cyclic BPC block codes, we can find the better performance on the optimized convolution LDPC block by witnessing coding delay and decoding complexity. The author proposed the technique which is capable of finding better performance of LDPC codes in different applications. The optimization of the codes can be done as explained: Base Matrix Optimization and labelling Optimization. The practical restrictions have been demonstrated which include delay compatibility and low encoding complexity [8, 9]. The authors [10] have proposed a code known as systematic quasi cyclic LDPC code. The construction of this systematic code is done by the technique of row reduction which is different in comparison to the conventional Gaussian row reduction method. Row reduction technique is actually easy to implement in comparison to method of gaussian row reduction. The structure of quasi cyclic is retained in this work. The parity check matrix H, of QC LDPC has also been retained in addition to introduction to a low complexity approach for generator matrix design. This method offers an efficient BER performance for high rate quotes and retains less complexity in the encoder circuit [11-15].

2.1 Systematic and non-systematic QC-LDPC methods

The proposed systematic construction performs similar to the field partition for low values of SNR and has a better performance for higher values of SNR, as seen in Figure 2. The authors [4] have proposed the LDPC encoder design with the use of a lower triangular code check matrix. The matrix is designed using Lab-view programming language. The 3 sub block sizes and 4 code rates are obtained with the help of a unified architecture. On the basis of 802.11 wireless standards, calculation of the redundancy bits was done to generate 12 different code words. The design of Mask Matrix was used to differentiate space and zero in the code check matrix. The code words transposed is used with the code check matrix product to determine the accuracy of the codes. An encoder of lower triangular and code check matrices is designed by using four code rates and three Z values which results in generating the 12 code check matrices. The authors [16] have utilized in encoding operation using rows and columns of LDPC parity Matrix.

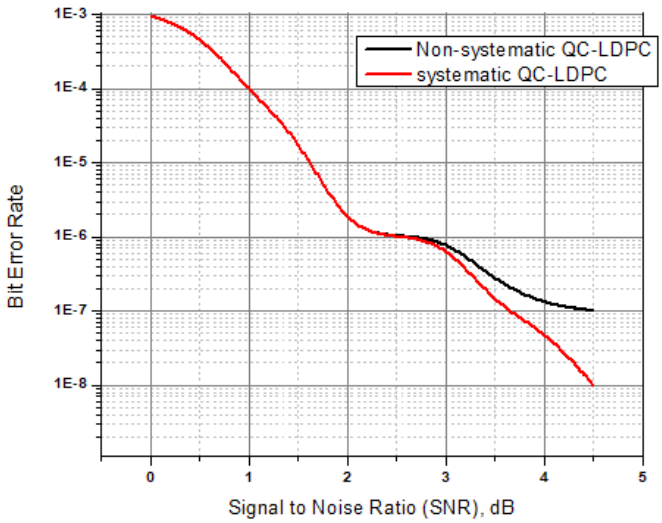

Figure 2. Nonsystematic QC-LDPC (744, 573) comparison with systematic QC-LDPC (806, 620)

2.2 LDPC encoder and decoder resource utilization protocols

The parity check encoder and decoder are proposed and implemented on Xilinx platform. The simulated results shows that the implemented design consumes low power, minimum number of resources and produce high accuracy [17]. Table 1 shows resource usage report of the implemented design. The proposed encoder utilizes the 13% of RAM resources, and 17% of slices. This shows that the designed encoder is suitable for implementation of the hardware.

Table 1. LDPC implementation resource utilization

Processor Logic Utilization	Available Resource	Used Resource	Utilization Resource in percentage
No's of BUFG/BUFGCTRLs	16	1	6%
No's of Block (First in First out) FIFO/ (Random Access Memory) RAM	268	36	13%
No's of Slice Registers	184304	323313	17%
No's of bonded IOBs	296	8	2%
No's of Slice Look-up Table (LUTs)	92152	32479	35%
No's of fully used Look-up Table Flip-flop (LUTs-FF) pairs	39400	25392	64%

In this study, the Model-Sim and MATLAB software can be used to establish a joint platform as per the characteristic of quasi-cyclic and in CDR standard for LDPC encoder. The Figures 3 and 4 shows block diagram and Graphical representation of LDPC implementation respectively [18-20]. LDPC code is very essentially used in China digital radio (CDR). it is a frequency modulation radio broadcast standard (87 MHz to 108 MHz). The CDR signal strength is attenuated due to noise generated by various parameters, as shown in Figure 5. Figure 6 shows the LDPC code performance analysis which has been done on various communication encoding techniques such as OFDM with Forward Error Correction (FEC), Fast Information Channel (FIC), Mobile switching centers (MSC) Level 2 using Digital Audio Broadcasting standard channels with a conventional code rate of 3/8 with a code length of 1152 bits.

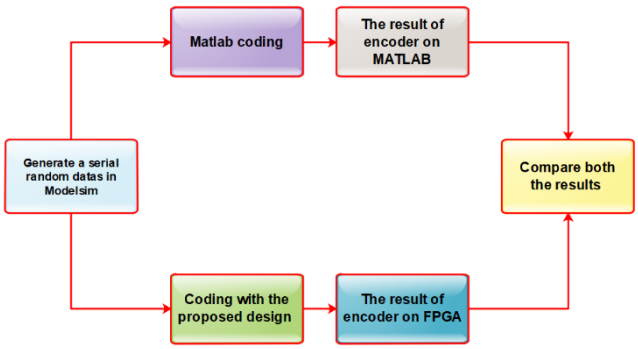

Figure 3. LDPC Encoder protocol verification block diagram

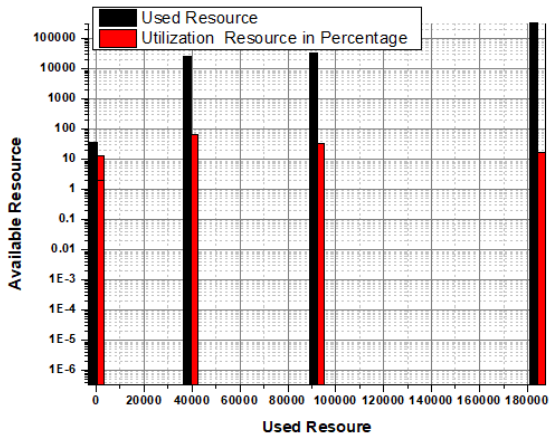

Figure 4. Graphical representation of LDPC implementation resource utilization

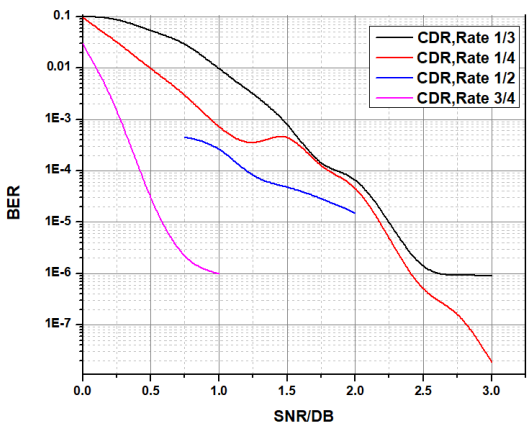

Figure 5. LDPC code performance analysis with various CDR code rates

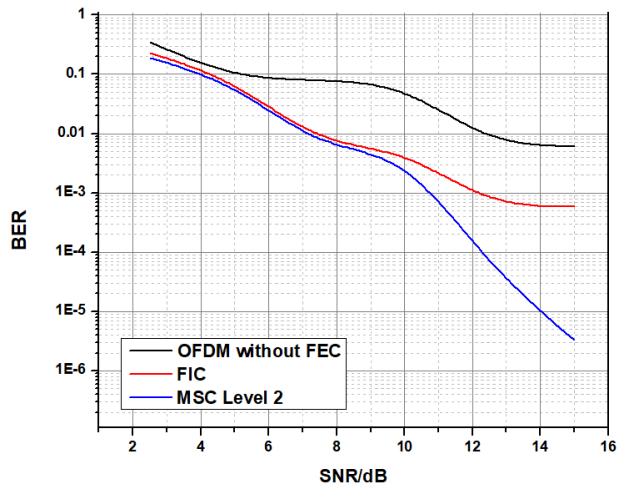

Figure 6. LDPC code performance analysis for DAB using standard channels

3. FIELD PROGRAMMABLE GATE ARRAY BASED LDPC ENCODER TECHNIQUES

In the applications of Deep-Space (AR4JA) and Near-Earth (C2) communications, the Consultative Committee for Space Data Systems (CCSDS) uses the Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) codes. In order to obtain the high throughput, the existing architecture is not efficient. Therefore, encoder architectures with CCSDS are recommended with suitable standards. In the prior art, several architectures have many numbers of registers and logical resources. In this paper, we propose an architecture which reduces resource utilization. A grouping has been used in encoding algorithm to extract the common subexpressions. To reduce logical resources, two-layer architecture is used to integrate similar kind of circuit structures [21-26]. A pre-processing method is used to handle special size of the generator's matrix. Additionally, the control unit is replaced with configuration registers. The proposed architecture is implemented using only 1658 LUTs and 1038 FFs, verified on FPGA and a throughput of 4.69 Gbps is achieved. This architecture comparison shows that, it provides multi-Gbps throughput and lower resource utilization as compared to existing architectures.

3.1 FPGA based quasi-cyclic low density parity checks encoder

In this paper, we propose 12 quasi-cyclic low density parity checks with two-step encoding as per the standards of IEEE 802.11n/ac/ax. In this method it includes all codes of the particular set instead of separately targeting each code. Multiplication is performed by inverse matrices in the proposed algorithm. This encoding method will greatly reduce the complexity of the multiplications. For any other type of supported codes, the encoding process will take single or many clock cycle which allows the full-parallel architecture implementation. XOR-gate trees are used in proposed VLSI encoding architecture [27-29]. The proposed method uses the common sub-expression sharing techniques (CSST) to extract common subexpressions (CSs) with features and structure of the used matrices. In this paper the original matrices common features and corresponding inverses helps to identify expressions result. Here the specific codes that deals with

innovative subexpression extraction procedures are explained as a set. The proposed encoder technique operates at 1 GHz frequency and consumes 125 to 107 K-Gates and integrated using 90- and 45-nm technologies. This encoder achieves the throughput up to 1.62 Tbps.

In this work, On Field-Programmable Gate Array (FPGA), we have implemented a rate-adaptable (RA) prefix-free code distribution matching (PCDM) encoder. A wide range of information rates from 1.6 to 4.8 bit/symbol with fine granularity of 0.2 bit/symbol in probabilistic constellation shaping (PCS) systems, is supported in RA-PCDM encoder Implementation. RA-PCDM Implementation has the shaping performance of 0.55 db of the theoretical limit [30-35]. In a universal architecture for all PCDM codebooks, sliding window processor is used in demonstrating parallel encoding of RA-PCDM. RA-PCDM encoding and decoding is almost the same in terms of procedure and complexity. It is shown that less hardware area is used in RA-PCDM when compared with low-density parity-check (LDPC) codes based traditional rate adaptation scheme, while offering finer rate granularity and shaping gain. To achieve channel capacity, RA -PCDM is a practical PCS technology that enables high-throughput optical communications than RA-LDPC at a lower cost [36, 37].

3.2 LDPC encoding preprocessing frameworks

The authors [38] have described a flexible hardware encoder which can be used for regular and irregular parity check codes having low density. In comparison to the turbo codes, the LDPC codes have higher performance and lower complexity in decoding. However, the drawback of this code is complexity in encoding. The authors have presented hardware LDPC encoder by incorporating methods used by the Richardson and Urbanke [39-42]. The complexity of the designed encoder is in linear nature, flexible in design operation and supports H matrices as shown in Figure 7. An implementation on FPGA Virtex-II XC2V4000-6 shows that it occupies the resource space of only 4%. The frequency of the operation is 143 MHz and produces the throughput in terms of code words of 45 million with latency equal to 0.18 ms. Improvement in performance is achieved by working on the parallelism feature. On the same chip several instances of encoder are mapped concurrently by encoding the multiple message blocks. In the same device if encoder is implemented with sixteen instances and 82 MHz frequency, then device is capable of producing code word of 410 million per second and operates 80 times faster in comparison to Intel Pentium-lV 2.4 GHz PC [43, 44].

The LDPC codes perform well in comparison to Turbo codes, having low complexity and are similar in design. The authors have considered the encoding problems of the LDPC codes. The problem of encoding for codes specified by sparse parity-check matrices has been considered [45, 46]. The authors have demonstrated the method of design efficient encoders by exploring the sparseness of parity check matrix. Also authors have proven that dissociative coefficient can be reduced to a very low value to maintain and coding quotes even of the practical length 100000. The optimized codes have actually admitted the real linear time encoding. Table 2 shows the comparison between various processor instruction execution speeds with respect to time. Figure 8 shows the graphical analysis of various processor instruction execution speed with respect to time.

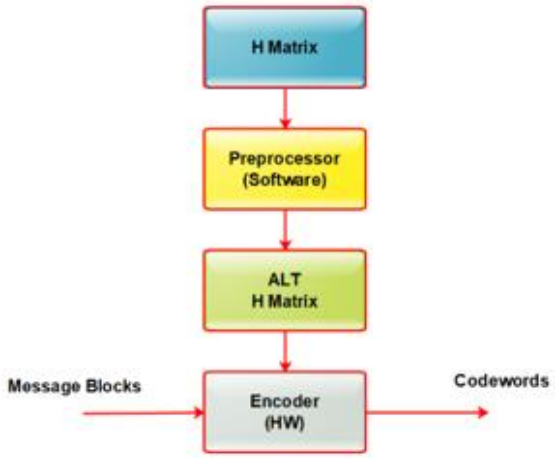

Figure 7. LDPC encoder pre-processing framework

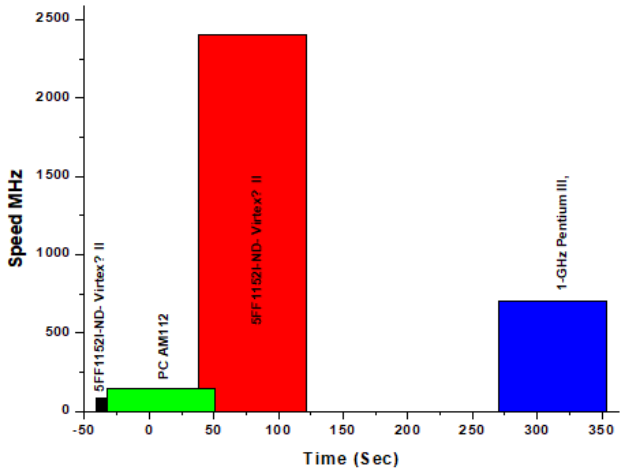

Figure 8. Graphical analysis of various processor instruction execution speeds with respect to time

Table 2. Various processor instruction execution speed with respect to time

Processor	Time (Sec)	Speed (MHz)
Field Programmable Gate Array-Virtex®-2, 16 encoder instances.	1	82
PC AM112 (Intel Pentium 4 2.66 GB).	80	2400
Field Programmable Gate Array-Virtex®-2, Encoder.	9	143
Hard drive20 GB, RAM256 MB, 1-GHz Pentium III	312	700

DVB-S2 standard LDPC encoder architecture has been studied [47]. The 360 bit wise parallel operation is the basis of proposed LDPC encoding architecture. To improve the speed two types of index addresses are used. This designed LDPC encoder is implemented on FPGA and throughput found to be 10GBPS at 100 MHz clock frequency.

The high speed parallel 360 bit wise processing is performed by using Eq. (1).

$$B_{i,j} = B_{i,j} \oplus B_{i-1,j} \quad (i = 1,2,3 \ldots., p-1, j = 0,1,2 \ldots.,359) \tag{1}$$

where, 'B' presents Bit parity in memory, 'i' descries the row wise location in memory matrix, 'q' is the first column out of

359 columns in the memory matrix and 'j' descries the row wise location in memory matrix.

4. VARIOUS LDPC ALGORITHMS AND ITS ARCHITECTURES

The authors [48] have presented a new LDPC encoder for CMMB and it has been designed based on the RU method. In this method, backtracking algorithm have been used to improve the efficiency. This process significantly minimizes complexity of encoding and calculation. The LDPC encoder implemented for CMMB has an increased rate of encoding.

4.1 Hardware and software framework for LDPC Encoders

Figure 9 shows the basic framework of the proposed encoder. There are two steps in the proposed work, pre-Hardware encoding and processing [49, 50]. The method of optimized LU decomposition has been used to pre-process the original parity check matrix H, which generates the necessary matrices used by the hardware encoder. For the pre-processing stage, software platform has been used once for the given H matrix. Similarly to encode the message blocks software implementation has been used.

The authors [51] have presented low density parity check code based encoder architecture for DMB-TH based on Application Specific Instruction Set Processor (ASIP). Analysis of the encoding algorithm has been carried out and the ASIP encoder has been optimized. Extraction of the special instruction sets is done according to the optimised algorithm. High throughput is obtained in the ASIP architecture with the use of main processor and co-processor working. Simple programs can change the code rates to 0.4, 0.6 and 0.8 in ASIP encoder and thus it is flexible. Keeping the maximum frequency of 117MHz, based on XC2V6000, throughput of the encoder can deliver 232Mbps, 206Mbps and 187Mbps for 0.8, 0.6 and 0.4 code rates, respectively. Figure 10 shows the connection of the main processor to the co-processor. The coprocessor is the subordinate processor which performs tasks under the control of main processor [52-55].

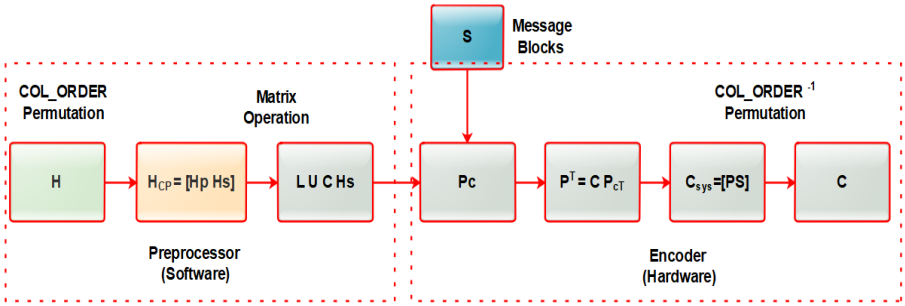

Figure 9. Hardware and software framework of LDPC encoder

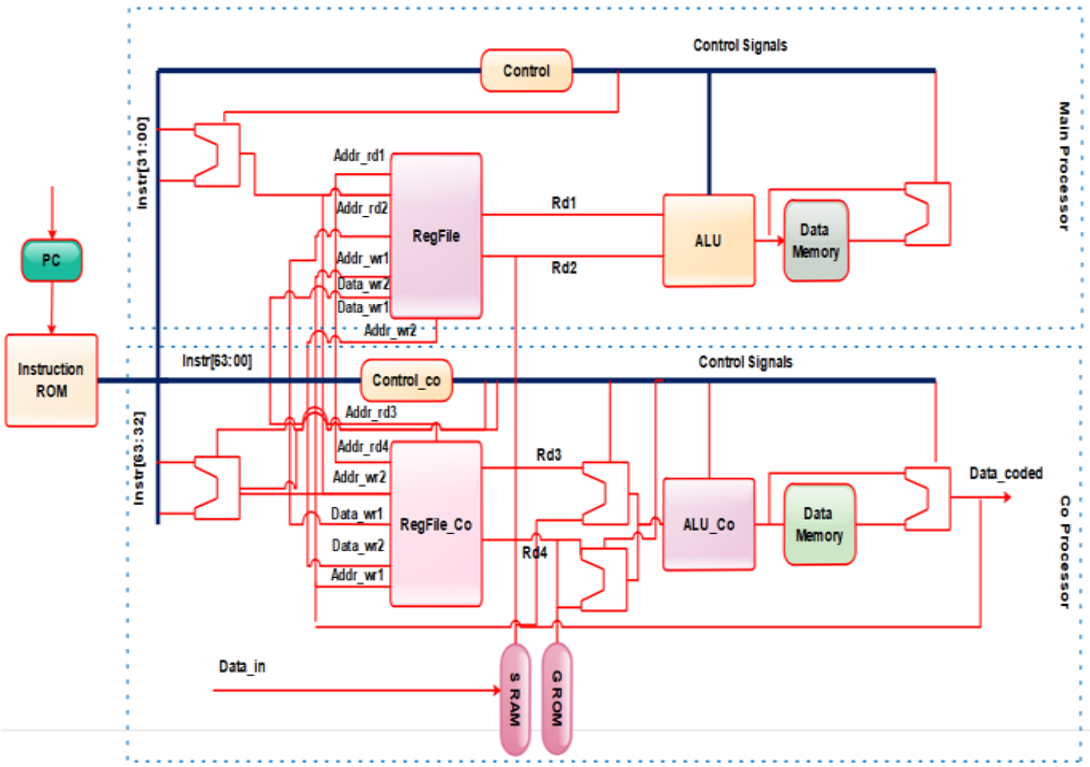

Figure 10. The LDPC encoder architecture

The quasi-cyclic matrix is given in Eq. (2).

$$H = \begin{bmatrix} H_{1,1} & H_{1,2}O_{1,3} \dots\dots\dots\dots\dots & H_{1,n} \\ H_{2,1} & H_{2,2}O_{2,3} \dots\dots\dots\dots\dots & H_{2,n} \\ & & \vdots \\ H_{m,1} & H_{m,2}\,O_{m,3} \dots\dots\dots\dots\dots & H_{m,n} \end{bmatrix} \quad (2)$$

where, H describes the quasi-cyclic matrix, i indicate numbers rows in a matrix, j indicates numbers of columns in matrix is $H_{i,j}$ represents 127 * 127 matrix, $O_{i,j}$ represents the 127 * 127 all zero matrix.

4.2 Low complexity LDPC encoder for CMMB

The authors [56] have presented real time LDPC encoder with low complexity for CMMB. This encoder supports a code rate of 1/2 and 3/4. Also to store data the sparse matrices are used in the memory organization. The entire design has been routed and synthesized using Altera Stratix 2. The rate of encoding is 32.44 Mbps with maximum frequency of 200 MHz for 1/2 code rate and 67.16 Mbps for 3/4 code rate. The arbitrary H Matrix LDPC code can be supported by the fully parameterized LDPC encoder with necessary initialized data of memory block.

The encoded LDPC codes obtained by CMMB are systematic. The parity and information bits can be rearranged as given in Eq. (3).

$$C_{Col\_order(i)} = \begin{cases} P_{bit_i} & 0 \le i \le 9215 - K \\ S_{bit_{i+k-9216}} & 9216 - K \le i \le 9215 \end{cases} \quad (3)$$

Table 3. Application of LDPC in various fields

Sl. No.	Authors Name	Year	Merits	Limitations
1	Liao et al. [57]	2021	• A flexible high speed with maximum throughput LDPC for 5G communication using single GPU processor is proposed. • The proposed LDPC encoder has a high throughput of 38-62 GPS with respect to ½ to 8/9 response rate of single GPU.	• It is very difficult to operate efficiently in confined area. • Proposed LDPC encoder has performed more parallel operation using single GPU processor hence its consists more jitters and hazards in output signal it requires more filter to rectify the noise.
2	Choudhary and Janyani [58]	2021	• The author's presents two modified frame structure for OFDM optical fiber communication using LDPC code. • It is capable to carry the high bandwidth signal over a 50KM length at 10Gbps in single-mode fiber. • It enhances the OFDM signal error correction and detection rate by using phase conjunction subcarrier coding (PCSC). • LDPC codes have improved performance and low complexity of decoding in comparison to Turbo codes.	• When a 64-bit data packet communicates over single-mode fiber, it requires more subcarrier for long-distance communication process. Hence the model required for this process is more complex and expensive.
3	Nidagundi and Patil [59]	2016	• The resources utilization of ASIC FPGA analyzed in terms of number LUTs, logic blocks and bonded IOB. • It is observed that the RU method performs encoding operation with a propagation delay of less than 1.256 nanoseconds in comparison with the general method of LDPC encoder. • The paper proposes lower triangular approach and straight forward method encoding schemes for the LDPC codes and compared the methods for area utilization on ASIC platform.	• Comparison of ALT and Modified ALT methods is not done.
4	Johnson and Gaur [60]	2016	• The method reduces the conventional complexity. • The LDPC codes prove to be more efficient because of the BER performance • The method has FPGA implementation on Spartan 3E board and analysis has been done based on device utilization by the straight forward method in comparison to lower triangular modification method.	• The delay limitation has not been focused in the lower triangular method. • Power utilization has not been focused in both the methods.
5	Kakde and Khobragade [61]	2016	• This work aims to develop the VLSI architecture with flexible manner by effectively utilizing available resources. • A low complexity LDPC designed using architecture of systolic high throughput and message-passing algorithm. • The complete design is simulated and verified using Xilinx ISE 13.1 EDA tool.	• The device utilization reduces in ASIC, FPGA due to implementation of pipelining.
6	Dutta and Pramanik [62]	2015	• The work focuses on different levels of obstructions in the design of the decoding • In this paper, proposed an algorithm to form matrix of LDPC rectangular sparse into triangle square upper part and rectangular part of the H matrix. • The proposed algorithm has better BER performance.	• The hardware implementation has not been carried out. • The performance analysis has not been carried out between modified ALT and systematic ALT methods.

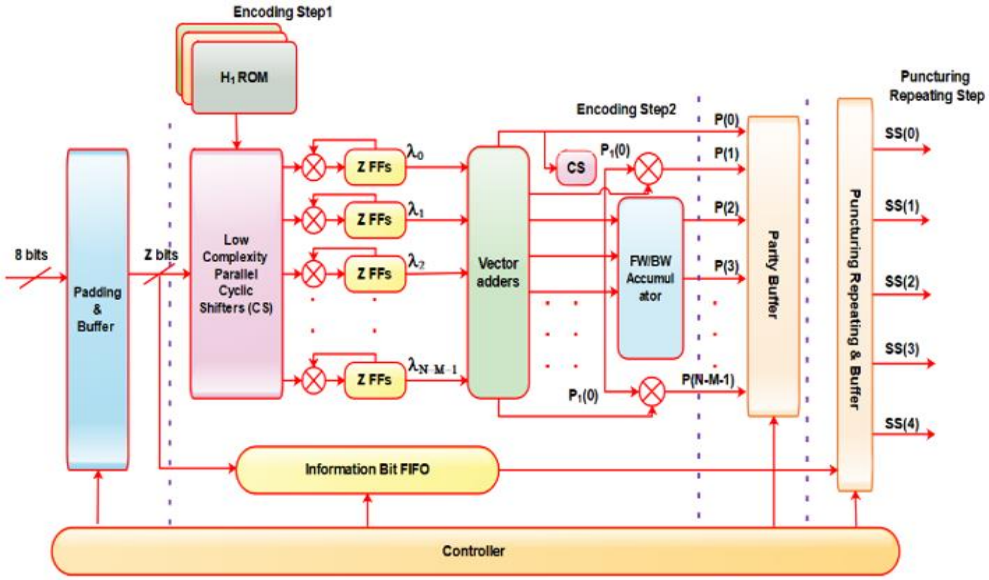

Figure 11. Compatible and low complexity Cyclic Shifters using LPDC

Information bit vector to be encoded is S-bits and the parity code vector is P-bits correspondingly. Where C represents the encoder codes efficiency, Col_order(i) is describing the bit mapping code words as per CMMB standards and K indicates LDPC information code length (4608 bits for ½ rate and 6912 for ¾ code rate). The Table 3 shows the various protocols and application of LDPC encodes. It also identified the merits and limitations of LDPC encoder's methods.

The authors [63] designed IEEE 802.11n/ac standards based architecture encoder for a Quasi cyclic low density parity check code. To achieve the high throughput and low complexity, the encoding process is designed based on the parallel processing. Low complexity cyclic shifters are used in the encoder architecture to reduce the hardware overhead. The encoder throughput is increased by performing forward and backward accumulation in one clock cycle. Implementation of the proposed encoder is done on a 130nm CMOS technology.

The proposed encoder core has a gate count of 96K. Figure 11 shows the proposed compatible and low complexity CS. Many steps are there in barrel shifter based proposed CS and supports Z in different sizes for cyclic shift by incorporating the multiplexors.

4.3 LDPC encoder algorithm's response on different code rate

A quasi-cyclic LDPC encoder structure is implemented on FPGA with pipeline architecture [64]. The experiment has been conducted on FPGA board ZYNQ-7 ZC706 with length of block range from 576 to 2304 with a code rate of 5/6. It is implemented by using Verilog HDL and results were analysed using Simulink. The implemented method is designed in such a way that supports different code lengths and code rates. A standard of IEEE 802.16e is followed for the base matrix and base parameters. The encoder throughput, logic elements and clock speed have been identified for different code lengths. The obtained results show that for IEEE 802.16e codes it gives speed up to maximum of 16 GBPS. The authors have presented higher efficiency and low complexity LDPC encoder.

Based on the Urbanke and Richardson work, classic method is used to design this encoder by incorporating a novel dynamic algorithm. This method uses the greedy algorithm with sparse matrix of LDPC codes for approximate triangulation. The encoding complexity has been effectively reduced for LDPC code in CMMB. The LDPC encoder is implemented on Altera Stratix 2 with code rate of 1/2 with 34Mbps encoding rate and 3/4 code rate with 69Mbps encoding rate.

The authors have the generalized LDPC (G-LDPC) and photograph based LDPC, design procedure is simple and has highly structured encoders and decoders. A computer based search is the basis for photograph based codes. In this work authors have used the photographs to design ensemble code word weight for finite length LDPC and generalized LDPC (G-LDPC). Also they consider the asymptotic case in this work. By observing the results of asymptotic case, minimum distance typical relative value grows linearly or not is verified. The code word weight enumerator technique is adopted to obtain the G-LDPC and LDPC codes. The linear growth for relatively smallest value is determined for trapping set size, pseudo weight and smallest stopping set size. From the results it is found that G-LDPC codes in trapping set enumerators is the solution for complex problem.

5. CONCLUSION

This work encapsulates a brief survey on LDPC code. The process of decoding implementation should not be so tedious compared with the encoding process. The mathematical operations performed on generator matrix and the parity check matrix is the complex part. The implementation in terms of the structures and the regularity of the LDPC codes is simplified. To achieve better error performance, the code detects the bits and handles all the errors and the Shannon limit could be attained. The SNR (signal to noise ratio) should be a high value to have a reliable communication by reducing noise to the minimum possible value. The SNR is improved in LDPC codes, but the geometry based design of LDPC codes has low SNR when compared with turbo structured LDPC codes.

Pipelined structure ASIC implementation has proved to consume less space and less delay in comparison with the non-pipelined structure. The performance in terms of bit error rate

is improved in modified ALT technique when compared with lower triangular systematic approximate method. The LDPC general encoder method has more propagation delay than 1.26ns of RU encoding method. The main drawback of the LDPC codes is its high encoding complexity. LDPC codes supports semi parallel architecture to provide parallelism.

Future Scope: LDPC code techniques will be enhanced to operate in 5G and 6G communication encrypted and decrypted operation by adopting reconfigurable parallel switching operations.

Limitation: The LDPC code techniques generate jitter, attenuation and hazards when it is operated in high speed parallel communication system

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