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Real-time Simulations on Ultracapacitor based UPQC for the Power Quality Improvement in the Microgrid

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ABSTRACT

Penetration of renewable energy systems (RES) into microgrid (MG) increases rapidly due to the intensified energy demands by the distribution level consumers. To meet this demand, consumers are erecting small scale distribution renewable energy generating systems (DREGS) which mostly constitutes of solar photovoltaic systems. Injecting power from the DREGS to the MG will rise potential problems like real and reactive power distortions, sag/swells which affect the power quality of the system. Voltage sags and swells are normally caused by MG intermittencies which occur at the high power and low energy situations. In order to maintain the power quality of the MG during intermittencies, an ultracapacitor (UC) is integrated along with a unified power quality conditioner (UPQC) with the DREGS is proposed in this paper. Basically, an ultracapacitor is a high power and low energy density device that will compensate the MG intermittencies. This proposed system deals with the control and design aspects of the ultracapacitor, a bidirectional converter for charging and discharging of UC, and a UPQC. The UPQC will act as a dynamic voltage restorer (DVR) for the MG side and an active power filter (APF) for the load side. The proposed system is designed and modelled using Matlab/Simulink platform and the results were analyzed.

1. INTRODUCTION

Day to day power intake to the low voltage distribution grid or MG from all power generating sources was increasing and the fact that due to the modernization of all the industrial and home applications which are now majorly operated on electricity. All industrial loads which exist on the SPV linked MG's will face power quality issues which causes system irregularities and stability problems [1]. DREGS export the excess power to the MG to satisfy the required demand. All DREGS come under non-conventional energy sources, out of which the SPV system is the major source. Due to this reason research mainly essences on SPV systems in recent years, and its design and modelling concepts were focused [2], [3] and some of the downsides of SPV are addressed to extract peak power from the system. For that MPPT algorithms are used for better yielding of output power [4], [5], [6].

However, the MG's linked with the SPV systems generates power quality issues into MG due to the irregularities in neutral currents, unbalanced load currents, harmonics, and uneven sharing of real and reactive powers [7]. In weak MG's due to the feed-in fluctuating SPV power into the MG will cause the voltage uncertainty problems like sags and swells [8], [9]. These voltage uncertainties will cause failures in power electronics systems due to false tripping of power electronic switches [10]. Power quality issues at the grid and consumer loads are serious issues at present-day MG's. To overcome these power quality issues some of the suitable solutions are using a UPQC with the SPV interfaced grid linked inverter [11]. The main objective of designing a UPQC is to enhance the power quality in the MG's by nullifying the harmonic currents caused by the sags, swells, and unbalanced loads.

A solar-powered versatile three-phase system is designed to recompense the load harmonics currents is discussed in [12]. A real power filtering mechanism in a single-phase solar-powered system is discussed in [13]. Mostly, single-phase and three-phase systems use shunt real power filter to work as a non-sinusoidal current source as discussed in [14], [15]. Series real power filters working as a non-sinusoidal voltage source which is tied between the MG and load can regulate the load unbalance voltages, reactive power of the load, and harmonic currents are discussed in [16]. It is well known that non-sinusoidal references are complicated to be analyzed using PWM converters, they require a further struggle to achieve decent real power filter performance, regarding this a dual compensation technique is employed in UPQC applications as discussed in [17].

Recent advancements in the power systems cause the penetration of DREGS like solar, wind, and plugin electric vehicles will give rise to power quality problems in the MG's. Energy accumulating devices like the battery, UC, fuel cells, etc., installed with DREGS will be a possible solution for the power quality problems and decreases the uncertainties to maintain the reliable operation of the system [18]. In the upcoming years, integration of energy accumulating devices is crucial and is commercially implementing on a large scale for many applications [19]. In many DREGS, battery storage systems were integrated with the MG with different control techniques to mitigate the instabilities in the system [20],[21]. All the power quality problems due to intermittencies can be

restored by using real power support as well as reactive power support from the energy accumulating devices. Out of all the available energy accumulating devices UCs is having the support for real power support for the MGs as well as reactive power support for the typical power distortion instances like voltage sags and swells [22].

This article addresses the power quality problems due to intermittencies in the DREGS tied MGs using UC based UPQC. The novelty of this paper is to introduce the UC with the UPQC device for the real power and reactive power assist to the MG and also presents the mathematical modelling of UC. Rather than the conventional battery-based DREGS tied low voltage MG's, the proposed system selects a UC due to its higher charge/discharge cycles and more economical. The major advantage of the proposed topology is having an average current mode (ACM) control coordinated with a central level integrated controller (CLIC) for BDC, which will operate the BDC in a stable operating region. The rest of the paper organizes as follows, section 2 deals with the proposed system design of UC and bi-directional DC-DC converter (BDC), section 3 deals with the control strategy for three-phase inverters of UPQC, a BDC, and a CLIC, section 4 presents the simulation outcomes of the proposed system and section 5 concludes the paper.

2. SYSTEM DESCRIPTION

In this section, basic design concepts of UC and a BDC are discussed, and the proposed system block diagram is presented in Figure 1 and it shows that DREGS connected with the load and is controlled by a UPQC device. The UC is connected to the dc-link of the UPQC through a BDC as shown in Figure 1.

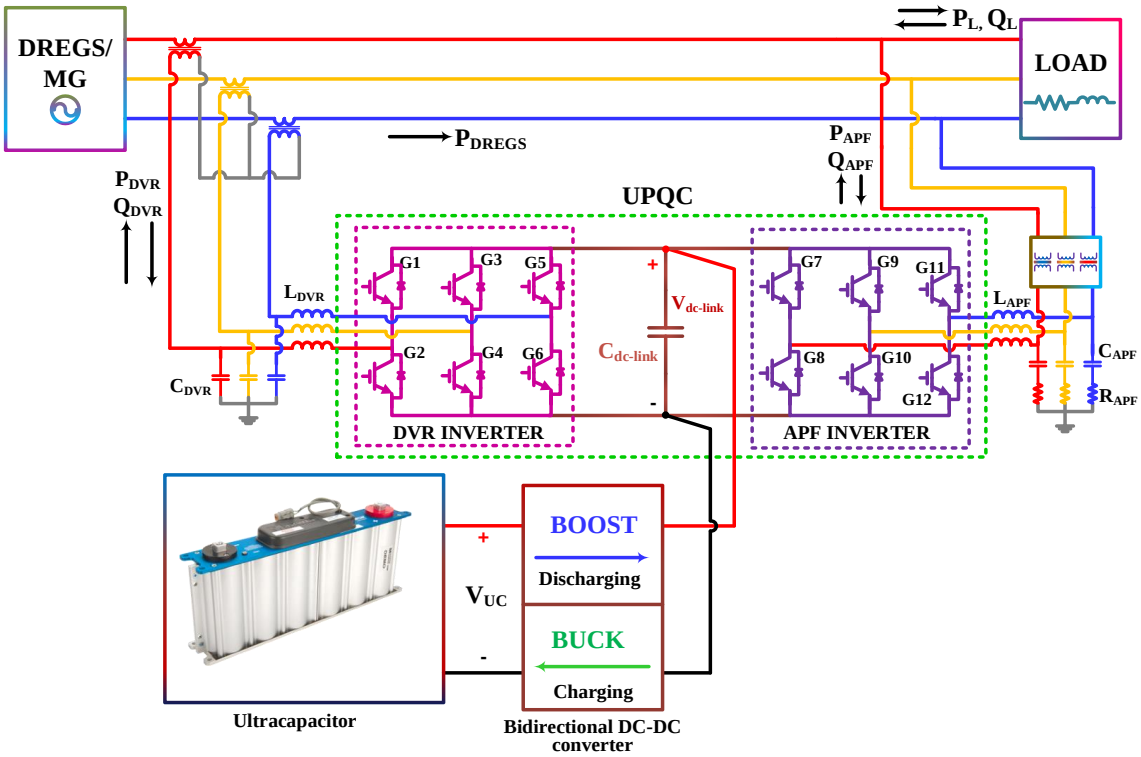


Figure 1. Block diagram of the proposed system with UC based UPQC.

2.1 Design and Modelling of Ultracapacitor

An ultracapacitor, also termed as an electrochemical capacitor or a supercapacitor, is an electrical energy storage device that is rapidly growing in popularity. The architecture and mechanism of operation are somewhere between a typical capacitor and a battery, which opens some exciting and useful applications. The equivalent circuit model of UC is shown in Figure 2, which constitutes of two resistors and a capacitor. The resistor which is parallel to the capacitor is called the equivalent parallel resistor (R_p), and the resistance which is series with the parallel combination of R_p and capacitor is called equivalent series resistor (R_s). R_p signifies the charging and discharging states of the UC and the R_s signifies the internal losses while the UC is in discharging mode.

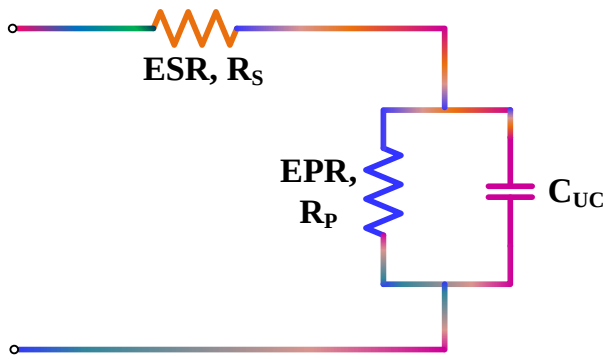


Figure 2. Equivalent circuit of UC.

The key constraint that controls the value of UC capacitance is the value of the preferred standby time of the converter [23].

The energy stored in a UC depends on the variations in the voltage across its terminals and the capacitance of it, which can be given by eq. (1).

$$E_{UC} = \frac{1}{2} C_{UC} \left(V_{i-UC}^2 - V_{f-UC}^2 \right) \quad (1)$$

where,

E_{UC} = Total capacity of energy that can be accumulated in the UC (W-sec)
$V_{i\text{-}UC}$ = Voltage before discharging (V)
$V_{f\text{-}UC}$ = Voltage after complete discharging (V)
C_{UC} = UC capacitance (F)

The value of C_{UC} can be calculated using eq. (2) [23] as follows

$$C_{UC} = I_{UC-avg} \times \left(\frac{1}{\Delta V} \right) \times \Delta t \quad (2)$$

Usually, UC is discharged up to half of its rated capacity, at half of its rated capacity 1/3rd capacity of energy accumulated in the UC is discharged as stated in [23]. Beyond half of its rated capacity, it is not cost-effective to discharge the UC and its needs converter should be overrated. To avoid these drawbacks, while discharging it is better to choose the low voltage limit ($V_{UC\text{-}low}$) as half of its rated voltage limit ($V_{UC\text{-}rated}$) as given by eq. (3) [23].

$$V_{UC-low} = \frac{V_{UC-rated}}{2} \quad (3)$$

The average current (I_{avg}) can be calculated using the following equations as stated in [23].

$$I_{max} = \frac{P_{out}}{V_{UC-low}} = 2 \times \frac{P_{out}}{V_{UC-rated}} \quad (4)$$

$$I_{min} = \frac{P_{out}}{V_{UC-rated}} \quad (5)$$

From eq. (4) & (6), we can calculate the value of I_{avg} as

$$I_{avg} = \frac{I_{max} + I_{min}}{2} = 3 \times \frac{P_{out}}{V_{UC-rated}} \quad (6)$$

where,

P_{out} = Converter power capacity at discharging
I_{min} =Minimum current of UC
I_{max} = Maximum current of UC

For a chosen value of converter rating, the minimum value of UC capacitance required is calculated as follows

$$C_{UC-min} = \frac{3P_{out}}{V_{UC-rated}^2} \times \Delta t \quad (7)$$

If the V_{UC} is the voltage of a single UC around 2.5 V. For obtaining a higher voltage rating, the number of UCs should be connected in series and the total voltage rating of the series-connected UCs is given by eq. (8) and for obtaining the higher current rating, the number of UCs should be connected in parallel (p). For n and p connected UCs, the minimum value of capacitance ($C_{UC\text{-}min}$) for a single UC is given by eq. (9).

$$V_{UC-series} = n \times V_{UC} \quad (8)$$

$$C_{UC-min} = \frac{n \times C_{UC}}{p} \quad (9)$$

where,

n = number of series connected UCs
$V_{UC\text{-}series}$ = Voltage across series connected UCs
p = number of parallel connected UCs

2.2 Design of Bidirectional DC-DC converter

A Bidirectional DC-DC converter (BDC) is a buck-boost converter and it should be operated in three modes of operation. A BDC acts as an interface between the UC and the DC link to maintain the constant voltage at the DC link point even though the voltage of UC gets varied at the discharging mode. An UC based BDC is shown in Figure 3, in mode I the UC will be in discharging mode by providing the real and reactive power support as well as the voltage recovery during voltage sags. In mode II of BDC operation, the UC will be charged by taking the power from the DREGS/Grid by compensating for the intermittencies in the line. In mode III of operation, BDC will be in PWM blocking state where both switches are in the blocked state.

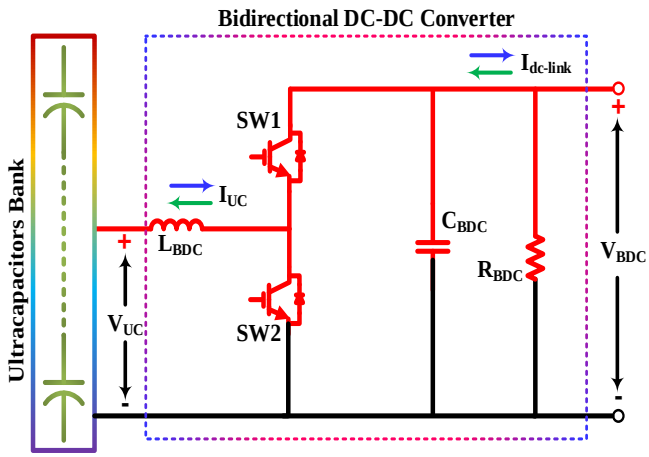


Figure 3. Ultracapacitors bank with bidirectional DC-DC converter.

3. CONTROL STRATEGY FOR THE PROPOSED SYSTEM

3.1 Control strategy for UPQC

The complete control strategy for UPQC is based on the controlling methods of DVR and APF inverters as shown in Figure 4. Two back-to-back three-phase inverters are connected through a dc-link capacitor in a UPQC topology as shown in Figure 1. One of the inverters acts as a series DVR which is connected between the DREGS and the dc-link capacitor and the other one is a shunt-connected APF inverter which is connected between the load and the dc-link capacitor. A BDC is connected to the dc-link capacitor to charge/discharge the UC storage of the proposed system. For DVR control, a PLL is used to estimate the value of angle θ, and the control method is known as the in-phase compensation method. The value of θ determines the voltages V_{RY}, V_{YB}, V_{BR}, and these line-line voltages are transformed into the d-q components and the line to neutral voltages V_{RN}, V_{YN}, V_{BN} can be approximated by using equation (10) as discussed in [24].

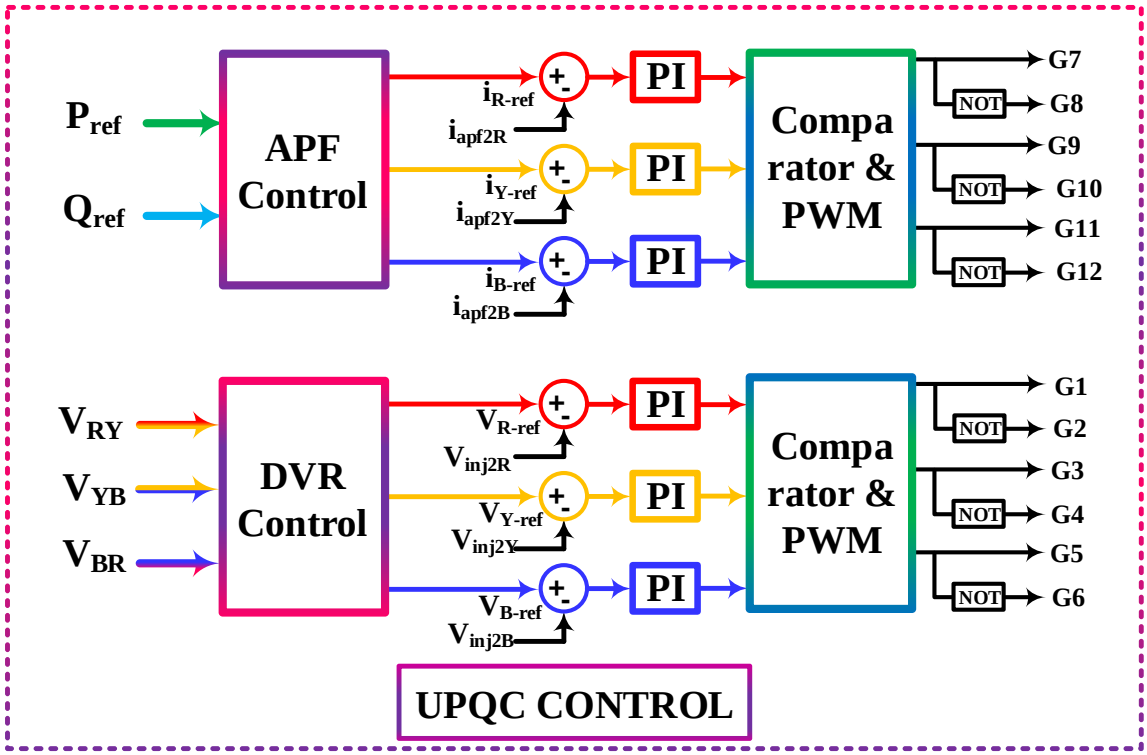


Figure 4. Control strategy for UPQC.

$$\begin{bmatrix} V_{RN} \\ V_{YN} \\ V_{BN} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\left(\theta-\frac{\pi}{6}\right) & \sin\left(\theta-\frac{\pi}{6}\right) \\ -\sin\left(\theta-\frac{\pi}{6}\right) & \cos\left(\theta-\frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} \frac{V_d}{\sqrt{3}} \\ \frac{V_q}{\sqrt{3}} \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} V_{R-ref} \\ V_{Y-ref} \\ V_{B-ref} \end{bmatrix} = m \times \begin{bmatrix} \left(\sin\theta - \frac{V_{RN}}{V_s}\right) \\ \left(\sin\left(\theta-\frac{2\pi}{3}\right) - \frac{V_{YN}}{V_s}\right) \\ \left(\sin\left(\theta+\frac{2\pi}{3}\right) - \frac{V_{BN}}{V_s}\right) \end{bmatrix} \quad (11)$$

These voltages are standardized using line to neutral voltage of 120 V_{rms} as a reference and equated with the actual system voltages V_s to identify the V_{ref}. The real and reactive power supplied by DVR is obtained using equation (12) as follows,

$$\left.\begin{aligned} P_{DVR} &= 3\times V_{inj2R(rms)} \times I_{LR(rms)} \times c\,os\,\phi \\ Q_{DVR} &= 3\times V_{inj2R(rms)} \times I_{LR(rms)} \times \sin\phi \end{aligned}\right\} \quad (12)$$

where,

V_d = voltage at direct axis component
V_q = voltage at quadrature axis component
P_{DVR} = real power of DVR
Q_{DVR} = reactive power of DVR
$V_{R\text{-}Ref}$, $V_{Y\text{-}Ref}$, $V_{B\text{-}Ref}$ = Injected voltage references
V_s = actual system voltage
m = modulation index which is taken as 0.45
$V_{inj2R(rms)}$ = rms values of injected voltage
I_{LR} = Load current
ϕ = phase difference

The shunt/APF inverter is based on the d-q current compensation method(i_d-i_q), in which i_q is used to control the real power and i_d is used to control the reactive power. The d-

q domain reference currents of APF inverter are calculated using equation (13), where $V_{q\text{-}s}$ is the system voltage in q-axis and the current references are calculated using (14) as follows

$$\left.\begin{aligned} P_{APF} &= -\frac{3}{2}\times v_{q-s}\times i_{ref-q} \\ Q_{APF} &= -\frac{3}{2}\times v_{q-s}\times i_{ref-d} \end{aligned}\right\rangle \quad (13)$$

$$\begin{bmatrix} i_{R-ref} \\ i_{Y-ref} \\ i_{B-ref} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{d-ref} \\ i_{q-ref} \end{bmatrix} \quad (14)$$

3.2 Control strategy for BDC

The voltage regulation of a BDC is done by using the ACM which is widely used in BDC controlling strategies [25], and a more stable operation is achieved to control the BDC for charging and discharging purposes of UC. The UC based APF has discharged the energy when the voltage reference V_{ref} value is greater than the $V_{out\text{-}BDC}$ value, which operates the BDC in boost mode by making the $I_{uc\text{-}ref}$ current flow positive, and for the buck mode of operation, V_{ref} value is lesser than the $V_{out\text{-}BDC}$ value thereby making the $I_{uc\text{-}ref}$ current flow negative. The ACM control and the CLIC are shown in Figure 5.

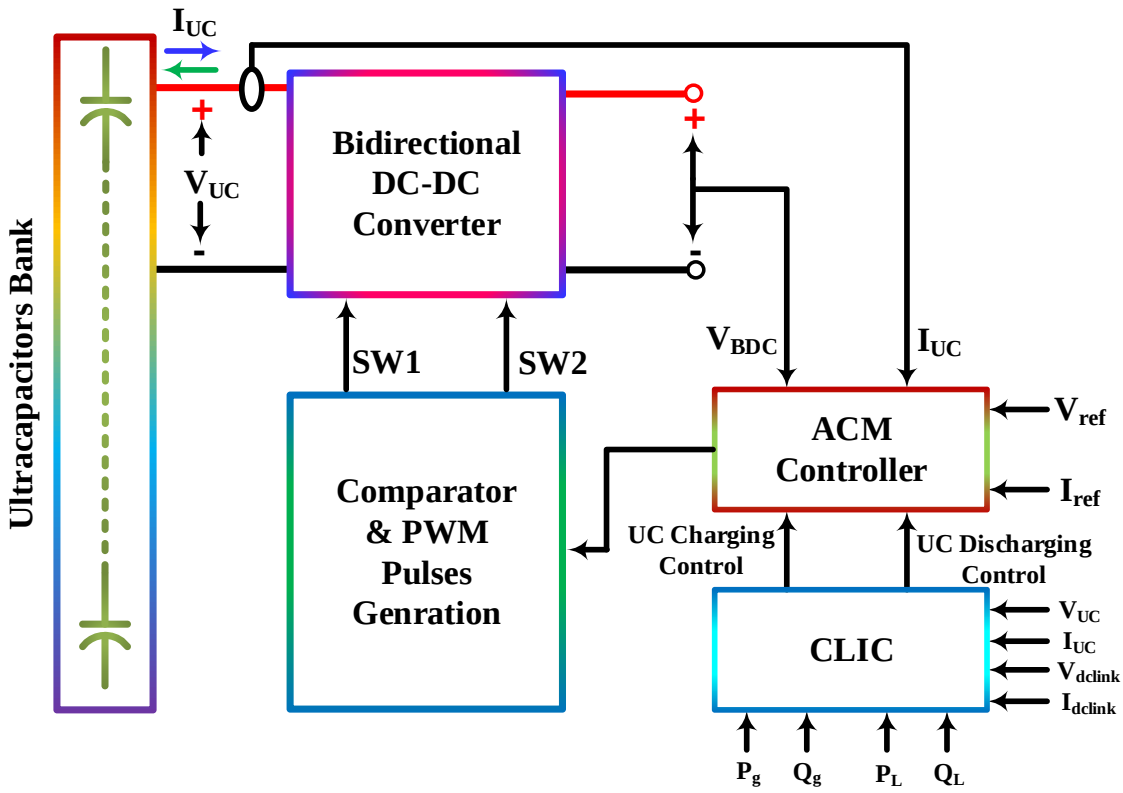


Figure 5. Control strategy for BDC along with the CLIC.

3.3 Central Level Integrated Controller

The CLIC controls the BDC and the UPQC circuit based on the circuit parameters like real and reactive powers of the grid (P_g, Q_g), load (P_L, Q_L), voltage and current of UC (V_{UC}, I_{UC}) and dc-link ($V_{dc\text{-}link}$, $I_{dc\text{-}link}$) as shown in Figure 5. This CLIC will operate in 5 states based on the above parametric inputs. In state I, CLIC will operate as a real power assist state and in state II it will operate as a DREGS intermittency smoothing state. In the state I and state II of operation the real power values P_L, P_g is used to set the P_{ref} value to control the UC-BDC system for supplying real power to the grid, and the P_{ref} will decide that whether the system should be operated in grid assist mode or UC charge mode. In state III, CLIC will operate in a reactive power assist state, in this state UC-BDC system will supply the reactive power to the grid, and the BDC losses will be supplied by the grid. In state III the reactive power values Q_L, Q_g is used to set the Q_{ref} value to control the UC-BDC system for supplying reactive power to the grid, and the Q_{ref} will operate the BDC to maintain a constant dc-link voltage.

In state IV, the CLIC will set the BDC to operates in boost mode to discharge the UC to compensate for the sag/swell instabilities for a short duration. Whenever there are short-term disturbances exist on the line, the energy stored in the UC should be supplied for a short duration to overcome these types of disturbances in the system. At the time of swell, the BDC should absorb the additional real power caused by the swell to stabilize the system, and at the time of sag, it should supply the real power to meet the requirement of the system. In state IV, the CLIC will set the BDC to operates in buck mode to

charge the UC, when its state of charge comes below half of its total capacity.

4. SIMULATION OUTCOMES

The simulation circuit of the proposed system is shown in Figure 6, and the simulation parameters are shown in Table. 1. The proposed system is designed and developed in Matlab / Simulink platform.

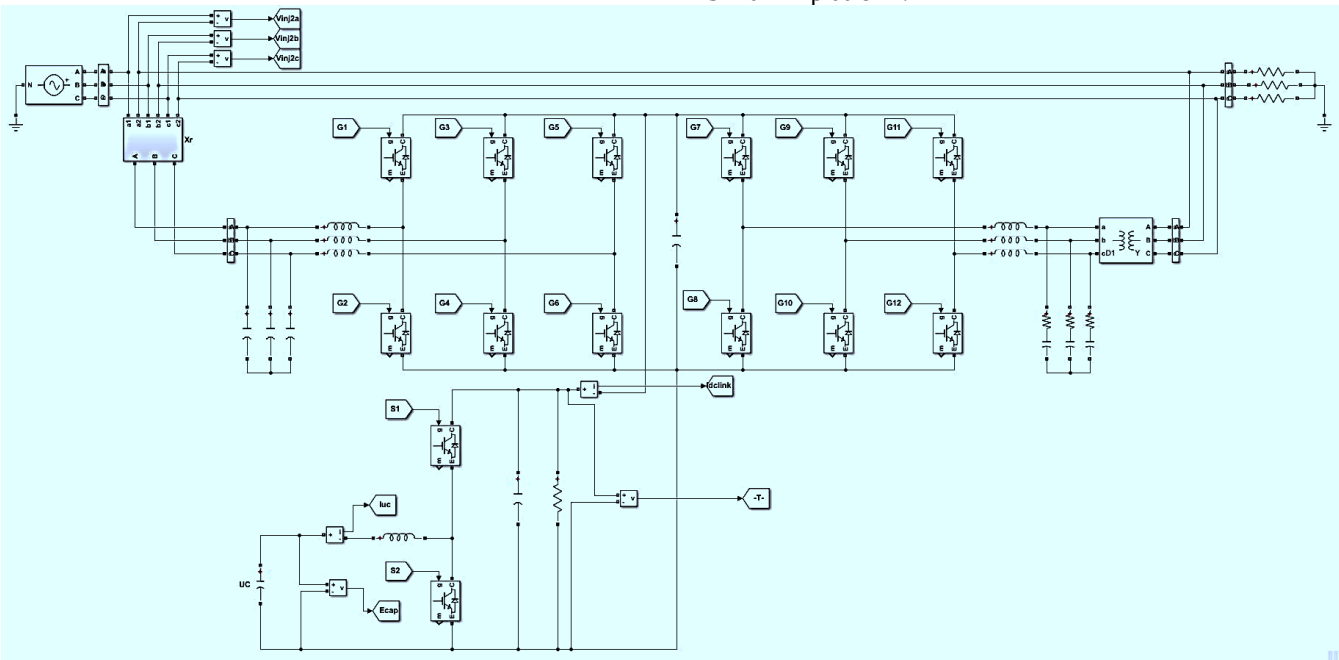
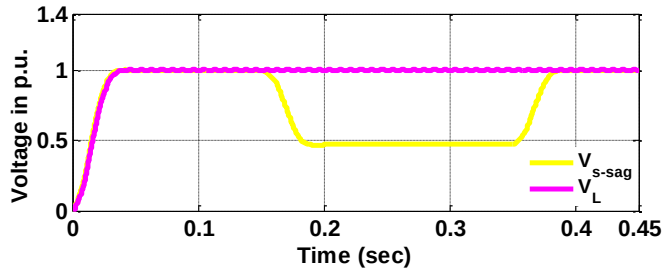


Figure 6. Simulation circuit of the proposed system.

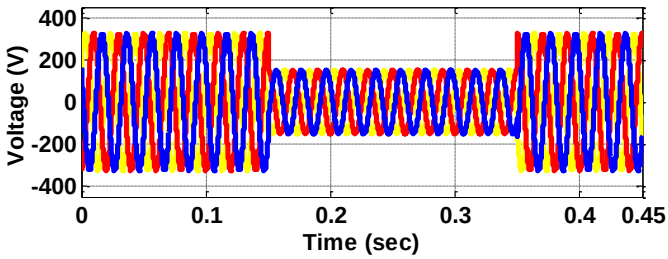
Table 1. Simulation parameters of the proposed system.

Sl. No	Parameter	Value
1	DREGS/Grid Voltage, V_g	208 V
2	Capacitance of UC, C_{UC}	60 F
3	Input inductance of BDC, L_{BDC}	160 µF
4	Output capacitance of BDC, C_{BDC}	45 µF
5	Output resistance of BDC, R_{out}	215 Ω
6	DC link capacitance, $C_{dc\text{-}link}$	3600 µF
7	DVR series inductance, L_{DVR}	1.5 mH
8	APF series inductance, L_{APF}	1.5 mH
9	DVR shunt capacitance, C_{DVR}	100 µF
10	APF shunt capacitance, C_{APF}	100 µF
11	Frequency	50 Hz

For the case I, the proposed system response is obtained in per unit values as shown in Figure 7(a), and for obtaining the three-phase system response the sag voltage of source in rms ($V_{s\text{-}sag}$) is induced in the system from time, t = 0.15 sec to 0.35 sec and the extent of the sag is taken up to 0.47 p.u. During sag, the load voltage (V_L) will be remained constant at around 0.99 p.u. with the help of UPQC. The line-to-line source voltages (V_{SRY}, V_{SYB}, V_{SBR}) of DREGS/grid is shown in Figure 7(b) and is having a voltage dip from 0.15 sec to 0.35 sec. This voltage dip is compensated by using a UPQC device with the help of UC-BDC, the injected voltages (V_{inj2R}, V_{inj2Y}, V_{inj2B}) is shown in Figure 7(c). During $V_{s\text{-}sag}$, the additional voltage required by the load is supplied by the UPQC to keep the line-to-line Load voltages (V_{LRY}, V_{LYB}, V_{LBR}) as constant as shown in Figure 7(d).



(a)



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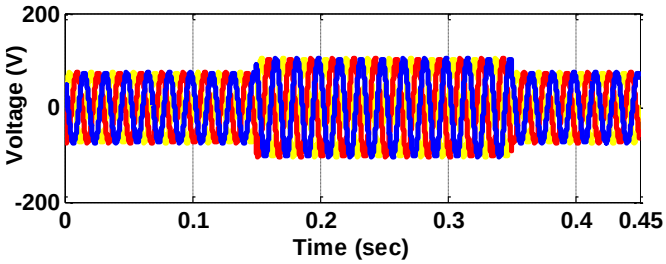

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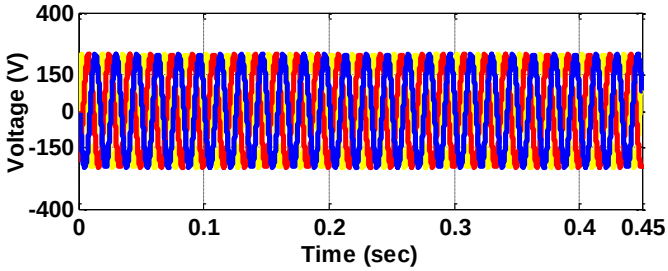
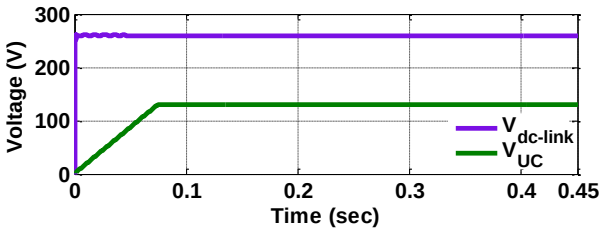


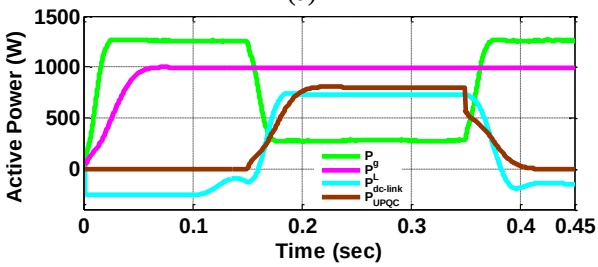
(d)

Figure 7. Voltage sag condition is taken from 0.15 sec to 0.35 sec (a) $V_{s\text{-}sag}$ and V_L in p.u. (b) the line to line source voltages (c) injected voltages of UPQC (d) line to line load voltages.

During voltage sag, Figure 8(a) presents the voltage of a BDC, Figure 8(b) and Figure 8(c) presents the real and reactive powers of the DREGS/grid, load, and UPQC. From Figure 8, during voltage sag, the real power deficit from the DREGS/grid is compensated by the UPQC device, which is the same as the input power of the inverter which was taken from UC storage. It is also identified that during sag the reactive power from DREGS/grid is reduced and it is compensated using reactive power supplied by the UPQC. The proposed system's real and reactive power support is simulated using Figure 8. During the time, t = 0 to 0.225 sec, the system operates in reactive power assist mode using reactive power from the UPQC which is shown in Figure 8(c), from 0.225 sec to 0.45 sec, the system operates in real power assist mode. The voltages of UC and the dc-link side are shown in Figure 8(a) and the real and reactive powers of the proposed system are shown in Figure 8(b) and Figure 8(c).



(a)



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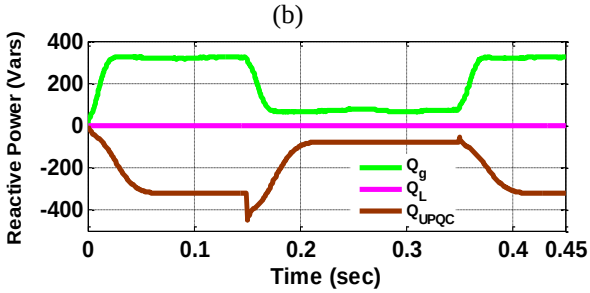
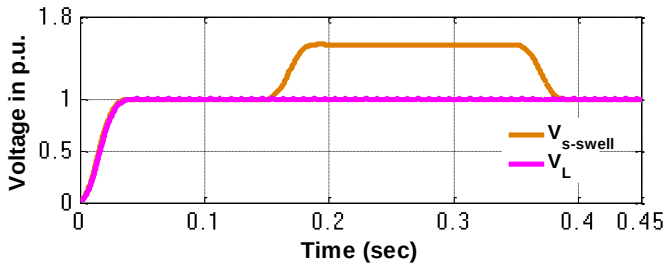


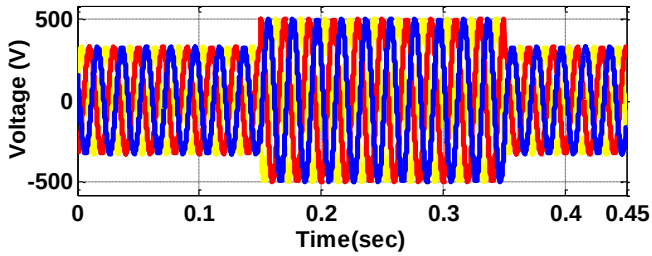
(c)

Figure 8. Sag condition. (a) Voltages of BDC and UC. (b) Real and Reactive powers of the proposed system using UPQC.

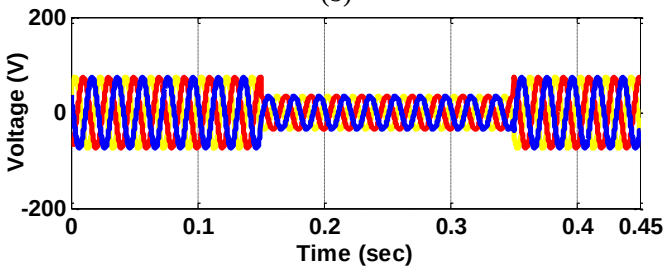
For case II, the proposed system response is obtained in per unit values as shown in Figure 9(a), and for obtaining the three-phase system response the swell voltage of source in rms ($V_{s\text{-}swell}$) is induced in the system from time, t = 0.15 sec to 0.35 sec and the extent of the sag is taken up to 0.53 p.u. During sag, the load voltage (V_L) will be remained constant at around 0.99 p.u. with the help of UPQC. The line-to-line source voltages (V_{SRY}, V_{SYB}, V_{SBR}) of DREGS/grid is shown in Figure 9(b) and is having voltage dip from 0.15 sec to 0.35 sec. This voltage dip is compensated by using a UPQC device with the help of UC-BDC, the injected voltages (V_{inj2R}, V_{inj2Y}, V_{inj2B}) is shown in Figure 9(c). During $V_{s\text{-}sag}$, the additional voltage required by the load is supplied by the UPQC to keep the line-to-line Load voltages (V_{LRY}, V_{LYB}, V_{LBR}) as constant as shown in Figure 9(d).



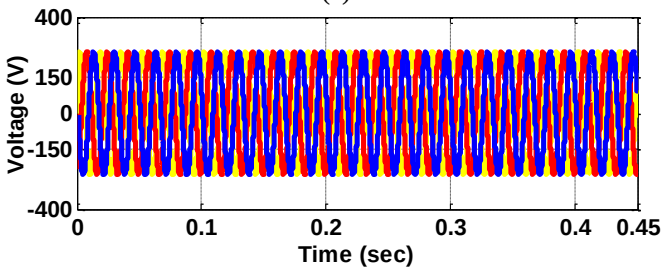
(a)



(b)



(c)



(d)

Figure 9. Voltage swell condition is taken from 0.15 sec to 0.35 sec. (a) $V_{s\text{-}swell}$ and V_L in p.u. (b) the line to line source voltages (c) injected voltages of UPQC (d) line to line load voltages.

During voltage swell, Figure 10(a) presents the voltage of a BDC, Figure 10(b) and Figure 10(c) presents the real and reactive powers of the DREGS/grid, load, and UPQC. From Figure 10, during voltage swell the surplus real power from the DREGS/grid is taken by the UPQC device, to charge the UC storage. The proposed system's real and reactive power are shown in Figure 10. The voltages of UC and the dc-link side are shown in Figure 10(a) and the real and reactive powers of the proposed system are shown in Figure 10(b) and Figure 10(c).

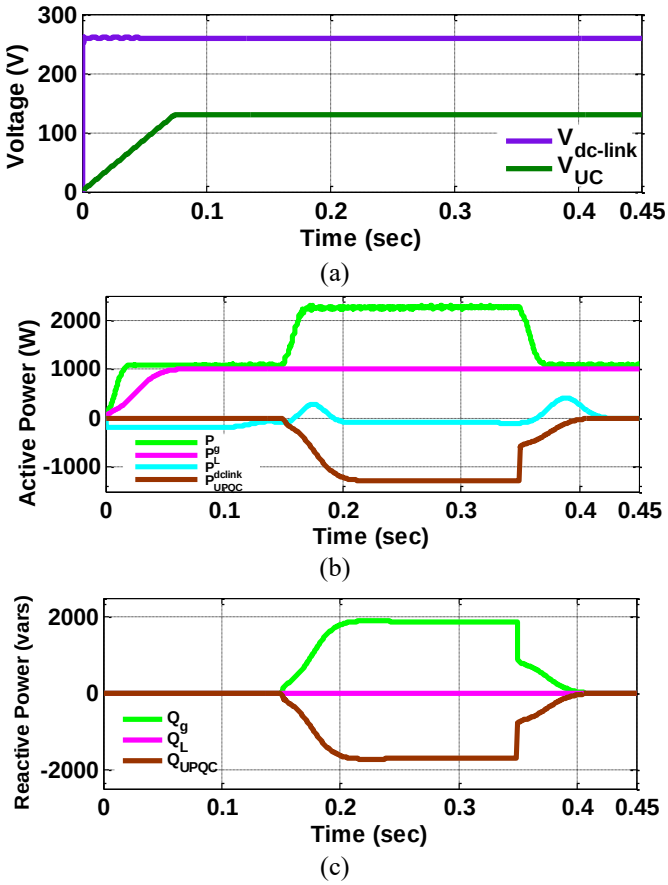


Figure 10. Swell condition. (a) Voltages of BDC and UC. (b) Real and Reactive powers of the proposed system using UPQC.

5. CONCLUSION

In this article, the proposed system uses an ultracapacitor based BDC converter and UPQC between the DREGS and loads to improve the power quality in the MG system. The voltage sag and swell will be compensated using the DVR portion of the UPQC. The real and reactive power assist will be provided by the APF portion of the UPQC to overcome the intermittencies caused by the disturbances. A CLIC integrated ACM control is employed to regulate the BDC converter to maintain the constant dc-link voltage. The DVR inverter employs an in-phase compensation control technique and the APF uses a current control d-q technique to control the proposed system are discussed. From the simulation results, it is clear that the proposed system performs well to compensate for the short-term disturbances in the Microgrids.

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