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Steady State Behavior of a Single-Switch Non-isolated DC-DC SEPIC Converter Topology with Improved Static Voltage Gain

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ABSTRACT

This paper presents the analysis of steady state behavior of a single switch non-isolated Single Ended Primary Inductance Converter (SEPIC) topology for achieving high DC voltage gain using diode-capacitor voltage multiplier. A voltage boosting module consisting of inductor and capacitor in addition with two diodes is introduced in the conventional SEPIC configuration in order to derive the DC-DC conversion technology proposed in this work. The voltage gain of the converter is extended using a diode-capacitor voltage multiplier cell. The converter suggested in this work has a single controlled switch. Hence, the conduction losses and the control complexity of the switch are very much reduced. The open loop configuration of the proposed non-isolated converter is described under continuous inductor current mode. The voltage boosting capability of the presented converter is compared with that of the existing modified SEPIC structure. The presented positive output converter topology has low switch voltage-current stress compared to the existing modified SEPIC topology given in the literature. The inductor and capacitor components of the suggested converter are so chosen that the DC output voltage and current waveforms show very low percentage of ripples. A DC voltage level of 24 V is given as input to the proposed converter. The DC voltage obtained across the load terminals is around 370 V which is achievable with low duty ratio (= 0.7) of the active switch. The voltage conversion ratio is very much influenced by the variation of the duty cycle of the power switch. In this work, the converter topology is presented and its various modes of operation are explained with equivalent circuits. The PSIM software platform is effectively and efficiently utilized to validate the performance of the converter. The obtained results convey that the proposed DC-DC conversion technology with extended voltage gain has the capability to maintain the steady-state output voltage and current profiles with almost negligible amount of ripples owing to the use of suitably designed non-dissipative elements in LC filter.

1. INTRODUCTION

During the past few years, both the population and industrial growth lead to increased electrical energy demand all over the world. The bulk amount of electrical energy can be generated using conventional sources (fossil fuels) such as coal, petroleum, and natural gas. But the method of generating electrical energy using non-renewable energy sources leads to pollution of surrounding environment due to carbon emissions from the electrical energy consumption and increased cost of the overall system. Moreover, the fossil fuels are depleting day by day. To protect the environment and reduce the global surface temperature, it is necessary to develop renewable form of energy sources. In the 1970s, the researchers began to concentrate on clean and sustainable energy sources such as photovoltaic (PV) panels, fuel cells, and wind power system [1, 2]. Among the various renewable energy sources available, solar resources have certain advantages such as reliability, environmental-friendly, low maintenance, and low operational cost. The DC output voltage generated by the solar cells is dependent on the weather conditions, and is of low value (around 15V – 40V) and is variable with respect to sunlight intensity [3, 4].

The low level of DC output voltage generated by PV panels should be converted to the high level of DC voltage in order to connect these PV panels to the grid or to the local consumers. Hence, it is required to have a power electronic interface between PV system and DC grid system [5]. This interface can be a step-up DC-DC power electronic converter with extremely low duty ratio, which should be capable to produce high DC voltage from the low DC voltage generated by the PV panels.

There are many isolated and non-isolated DC-DC boost power electronic converter topologies in literature to achieve high DC output voltage [6-19]. The high voltage gain can be obtained using traditional single-switch DC-DC boost converter with increased value of duty cycle nearer to unity [20, 21]. But the duty cycle nearer to unity will increase the conduction and switching losses which might result in lower efficiency. There is another way of increasing the output voltage by connecting multiple boost converters in series. However, this scheme will increase the cost of the converter due to too many numbers of components. The isolated topologies use a high frequency transformer for isolating the DC input port and the DC output port. However, these isolated configurations can achieve high step-up voltage conversion

ratio proportional to the size of the transformer. But the demerits of using transformer-based topologies are that (i). the leakage inductance of the transformer can cause voltage spikes on the active switches and high power dissipation, and (ii). electromagnetic interference (EMI) problems. Due to these limitations, the isolated topologies have reduced overall converter efficiency.

The high voltage gain can also be realized using coupled-inductor approach [22, 23]. But, in this method, the leakage inductance of the inductor causes high voltage spikes across the controlled power switches. An active clamp circuit can be used to resolve this issue [24]. However, the transformer-less DC-DC converters can be implemented using switched-inductor and switched-capacitor approaches to achieve high DC output voltage with minimum value of duty ratio of the switches [25, 26]. These approaches also suffer from the drawbacks such as complexity, a greater number of components, increased input ripple current level, and poor voltage regulation. Moreover, high charging currents will flow through the main active switch thereby causing high conduction losses in the case of switched-capacitor structure. The voltage-lift structure based DC-DC converter used to obtain high voltage gain also suffers from the increased conduction losses due to high charging currents [27-29]. The above drawbacks are eliminated in interleaved boost topology [30]. This topology can give high voltage conversion ratio when increased number of switches is employed in the circuit [31].

Because of higher efficiency and simple structure, non-isolated converter topologies are preferred. There are certain non-isolated single-switch DC-DC converter topologies such as Cuk, Zeta, conventional SEPIC, and modified SEPIC configurations for obtaining high static voltage gain [32, 33]. The modified SEPIC structure can give almost twice the static voltage gain as that produced by the conventional boost conversion technology [34]. The voltage gain of the modified SEPIC topology can be extended using voltage multiplier cell (Diode-Capacitor cell) technique [35]. This voltage multiplier based boost converters can be realized without any additional active switch. Moreover, the original configuration of the converter need not be modified because of the addition of Diode-Capacitor cell in the circuit [36]. Many Diode-Capacitor cells can be added to extend the static gain of the converter. It is possible to step-up the DC output voltage level to higher value without using any magnetic elements in the cell.

The work proposed in this paper explains the continuous inductor current mode operation of a non-isolated single-switch positive output step-up DC-DC conversion technology. The proposed topology is derived from the conventional SEPIC structure in order to achieve high DC voltage gain. The high gain is obtained from the proposed configuration without using high duty ratio of the main switch. The switch is subjected to low voltage-current stress. Further, the DC output voltage level can be extended using diode-capacitor cell based voltage expander. The addition of diode-capacitor cell modifies the open-loop voltage gain of the converter in such a way that the DC output voltage of the converter with voltage expander is almost twice that of the converter [33] without voltage expander.

The remaining sections are planned as follows: Section 2 gives the detailed analysis of modes of operation followed by the steady state behavior of the proposed non-isolated step-up DC-DC conversion topology. The validation of the proposed converter configuration through PSIM simulation is presented

in Section 3. Section 4 concludes the summary of the proposed research work.

2. ANALYSIS OF CIRCUIT CONFIGURATION AND STEADY-STATE BEHAVIOR OF THE PROPOSED DC-DC CONVERSION SCHEME
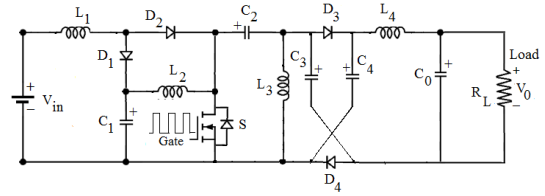

Figure 1. Circuit configuration of the proposed single-switch controlled non-isolated positive output DC-DC boost converter
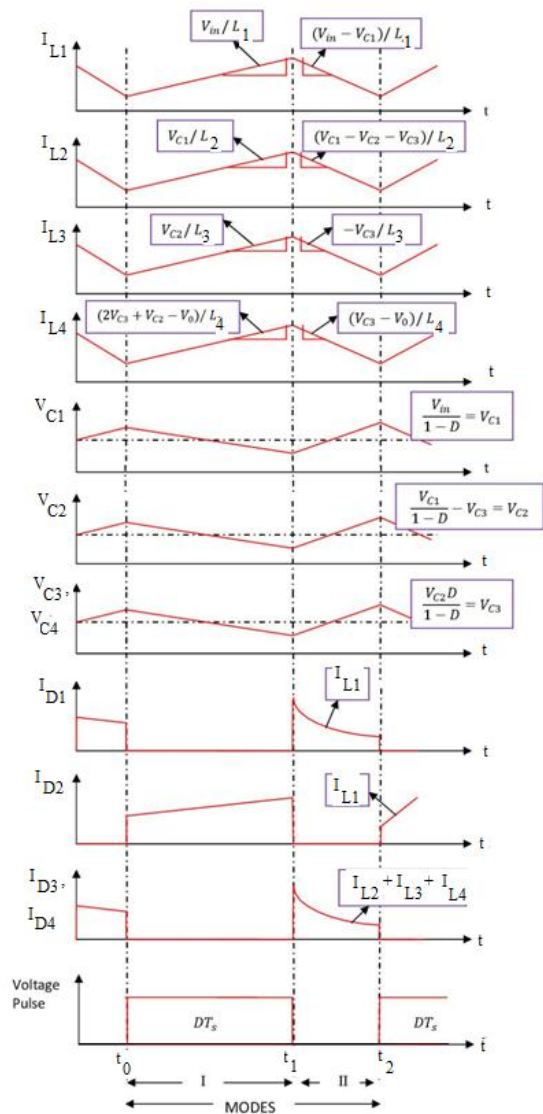

Figure 2. Typical steady-state waveforms of the suggested converter during continuous inductor current mode

The topology of a single-switch non-isolated positive output boost converter capable of producing high DC output voltage is shown in Figure 1. The proposed topology is the extension of the converter configuration given in ref. [33] with voltage

expander cell included. An input DC voltage of 24 V is given to the circuit. The DC output voltage appears across a load resistor R_L. The proposed extended converter configuration employs three identical inductors L_1, L_2 and L_3 with each of 1 mH inductance. There are two sets of identical capacitors: one set having C_1 and C_2 with each of 100 µF capacitance, another set having C_3 and C_4 with each of 10 µF capacitance. The large values of capacitances are chosen to achieve constant voltage. The power circuit employs four ideal diodes namely D_1, D_2, D_3 and D_4. The module formed by two diodes D_3 and D_4 and two capacitors D_3 and D_4 is called Diode-Capacitor voltage expander cell. The voltage gain of the converter proposed in [33] is extended using the Diode-Capacitor voltage multiplier module. The LC filter section consists of inductor L_4 and capacitor C_0. The filter components (L_4=1 mH and C_0=300 mF) are selected in such a way that the ripples are reduced in the output voltage and current. The ideal active high power semiconductor switch S is triggered into conduction by a proper gate pulse. All the inductors, capacitors, and diodes are controlled by the single switch S in the power circuit. In this work, the switching frequency (f_s) of the switch is chosen as 50 kHz. The typical steady-state waveforms of the suggested converter configuration operating under continuous inductor current mode are presented in Figure 2. The circuit operation and the steady-state behavior of the converter under continuous inductor current mode are explained as shown in Figure 1 above.

2.1 Circuit operation of the converter during Mode-I

The high power semiconductor switch S of the converter under continuous inductor current conduction mode is switched on during the time interval t_0-t_1. This mode of operation of the converter is represented in Figure 3. The diode D_2 gets forward-biased. The diodes D_1, D_3 and D_4 get reverse-biased. The inductor L_1 is magnetized with current flow path: V_{in}-V_{L1}-D_2-S-V_{in}. The inductor L_2 gets magnetized from the capacitor C_1 with current flow path: V_{C1}-V_{L2}-S-V_{C1}. The inductor L_3 gets magnetized from the capacitor C_2 with current flow path: V_{C2}-S-V_{L3}-V_{C2}. The inductor L_4 gets magnetized from the capacitor C_4 with current flow path: V_{C4}-V_{L3}-V_0-V_{C3}-V_{C4}. The load resistor R_L receives the energy from the capacitor C_0. The following equations are obtained during Mode-I operation:

$$\begin{cases} V_{in} = V_{L1}; V_{C1} = V_{L2}; V_{C2} = V_{L3}; \\ 2V_{C3} + V_{C2} - V_0 = V_{L4}; V_{C4} = V_{C3} \end{cases} \tag{1}$$

where, V_{L1}, V_{L2}, V_{L3} and V_{L4} represent the voltages across the inductors L_1, L_2, L_3 and L_4 respectively; V_{C1}, V_{C2}, V_{C3} and V_{C4} represent the voltages across the inductors C_1, C_2, C_3 and C_4 respectively.
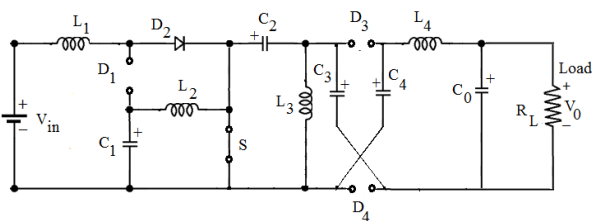
2.2 Circuit operation of the converter during Mode-II

The active switch S of the converter under continuous inductor current conduction mode is turned-off during the time interval t_1-t_2. This mode of operation of the converter is represented in Figure 4. The diode D_2 gets biased in the reverse direction. The diodes D_1, D_3 and D_4 get forward biased. The inductor L_1 gets demagnetized through the path: V_{in}-V_{L1}-D_1-V_{C1}-V_{in}. The inductor L_2 gets demagnetized through the path: V_{C1}-V_{L2}-V_{C2}-D_3-V_{C4}-V_{C1}. The inductor L_3 gets demagnetized through the path: V_{L3}-V_{C3}-D_4-V_{L3}. The inductor L_4 gets demagnetized through the path: V_{C4}-V_{L4}-V_0-D_4-V_{C4}. The voltages across the inductors are written as Eq. (2):

$$\begin{cases} V_{in} - V_{C1} = V_{L1}; V_{C1} - V_{C2} - V_{C4} = V_{L2} \\ -V_{C3} = V_{L3}; V_{C3} - V_0 = V_{L4}; V_{C4} = V_{C3} \end{cases} \tag{2}$$

By applying the volt-second balance principle for the inductors L_1, L_2, L_3 and L_4, the following Eqns. (3), (4), (5), and (6) can be obtained:

$$V_{C1} = \frac{V_{in}}{(1-D)} \tag{3}$$

$$\frac{V_{C1}}{(1-D)} = V_{C2} + V_{C3} \tag{4}$$

$$DV_{C2} = (1-D)V_{C3} \tag{5}$$

$$(1+D)V_{C3} + DV_{C2} = V_0 \tag{6}$$

where, D represents the duty ratio of the switch S.
By rearranging the Eqns. (3), (4), (5) and (6), the following voltage gain Eq. (7) is derived:

$$\text{Voltage Gain} = \frac{V_0}{V_{in}} = \frac{2D}{(1-D)^2} \tag{7}$$

The above Eq. (7) can be used to calculate output voltages (V_0) for various input voltages (V_{in}) and duty ratios (D). The following Table 1 depicts the values of output voltages for various values of input voltages and duty ratios. For comparison of the analytical results, the input voltage range is considered as varying from 12 V to 48 V due to the fact that the DC voltage delivered by the input renewable energy source may be in the range from 12 V – 40 V approximately. In this work, the upper limit for the duty ratio (D) of the switch is chosen as 0.7 as D value above 0.7 leads to very high output voltages for the increased input voltages.
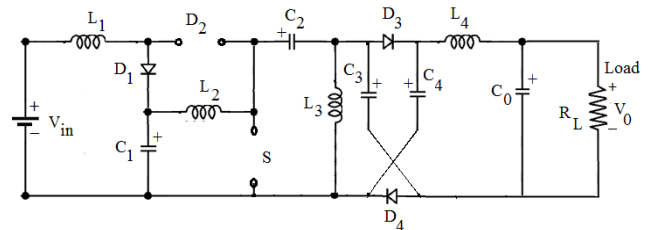

Figure 3. Circuit representation of the converter during Mode-I operation

Figure 4. Circuit representation of the converter during Mode-II operation

Table 1. Analytical results of the proposed converter

Input voltage (V_{in}) V	Output voltage (V_0) V				
	D = 0.4	D = 0.5	D = 0.6	D = 0.7	D = 0.8
12	26.67	48	90	186.72	480
24	53.33	96	180	373.44	960
36	80.00	144	270	560.16	1440
48	106.67	192	360	746.88	1920

3. PSIM SIMULATION MODEL OF THE CONVERTER AND THE RESULTS

Initially, the PSIM model of the non-isolated positive output DC-DC boost converter is developed without Diode-Capacitor (D-C) voltage multiplier cell as shown in Figure 5 and the converter operating under continuous inductor current mode is simulated in PSIM environment at a switching frequency of 50 kHz for the switch with duty ratio D = 0.7. The values of circuit components used for simulation are shown in Figure 5 itself. An input DC voltage of 24 V is given to the circuit as shown in Figure 9. The output DC voltage obtained is around 186 V and the output DC current is around 0.5 A for the converter without diode-capacitor cell. The waveforms of output voltage and output current are shown in Figure 6. Next, the PSIM model of the proposed converter is developed with a Diode-Capacitor voltage expander cell and an additional inductor L_4 as shown in Figure 7. The parameters of the proposed converter are tuned in such a way that a high level of DC output voltage around 370 V is obtained across the load. Table 2 lists the values of parameters used for simulation of the suggested converter. The gate pulse given to the active switch S is indicated in Figure 8. The duty ratio 'D' of the switch is varied from 0.5 to 0.9 to validate the performance of the converter. However, at duty ratio D = 0.6 itself, high static voltage gain is obtained. The waveforms of DC input voltage, DC output voltage and DC output current are indicated in Figure 9, Figure 10, and Figure 11 respectively. The output DC voltage obtained is around 373 V and the output DC current is around 1 A for the proposed converter with diode-capacitor cell. The waveforms of voltages appearing across the four inductors are shown in Figure 12, Figure 13, Figure 14, and Figure 15 respectively. Figure 16 shows the current flow through the inductor L_1. The remaining three inductors carry almost the same current as that of inductor L_1. The charging and discharging voltage characteristics of the capacitors C_1, C_2, C_3 and C_4 are depicted in Figure 17, Figure 18, Figure 19, and Figure 20 respectively. The charging and discharging current waveforms of the four capacitors is shown in Figure 21. The voltage-current stress waveforms of the diodes D_1, D_2, D_3 and D_4 are depicted in Figure 22, Figure 23, Figure 24, Figure 25, and Figure 26 respectively. The voltage – current stresses across the active switch S are indicated in Figure 27 and Figure 28 respectively.
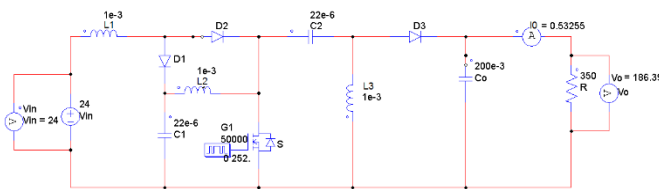

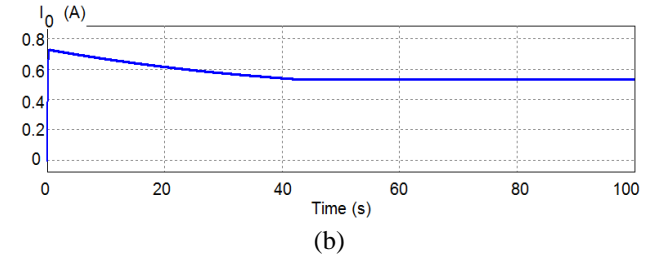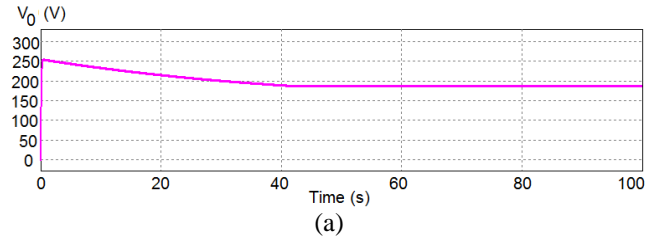**Figure 5.** PSIM model of the non-isolated DC-DC boost converter without Diode-Capacitor cell

Figure 6. (a) Waveforms of Output voltage (V_0), and (b) Output current (I_0) of the converter without Diode-Capacitor cell
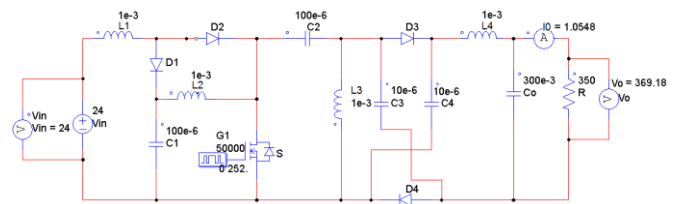

Figure 7. PSIM model of the proposed non-isolated DC-DC boost converter with Diode-Capacitor cell

Table 2. Simulation parameters of the proposed converter

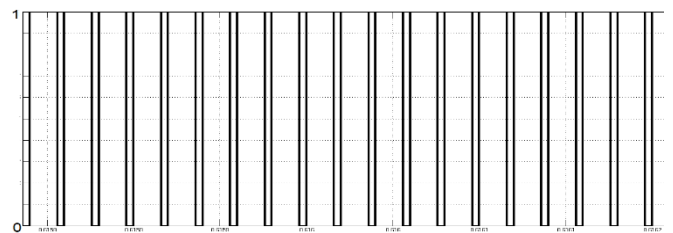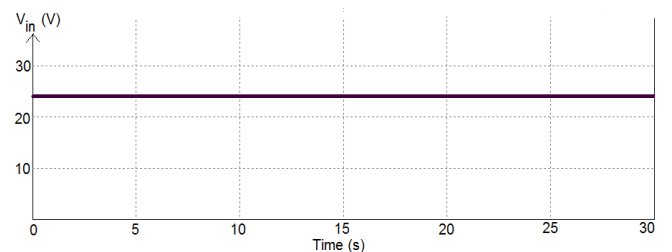| Parameters	Symbols	Values
Input voltage	V_{in}	24 V (DC)
Output voltage	V_0	370 V (DC)
Inductors	L_1, L_2, L_3, L_4	1 mH (each)
Capacitors	C_1, C_2	100 µF (each)
Capacitors	C_3, C_4	10 µF (each)
Output capacitor	C_0	300 mF
Switching frequency	F_s	50 kHz
Load resistance	R_L	350 Ω
Output current	I_0	1 A
Duty ratio of the switch S	D	0.7

Figure 8. Gating pulse to the switch S

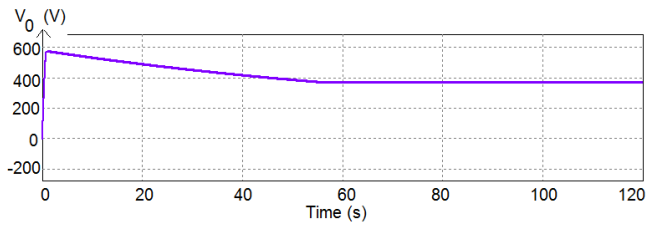**Figure 9.** Input voltage
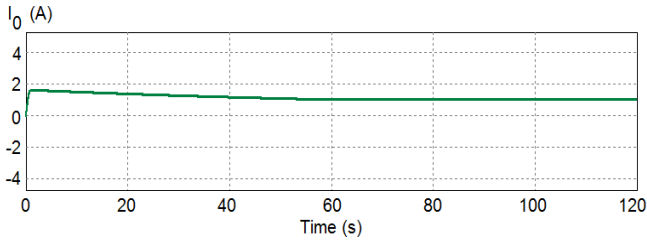
Figure 10. Output voltage (V_0)

Figure 11. Output current (I_0)
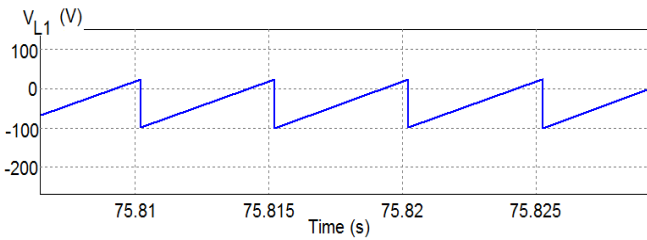

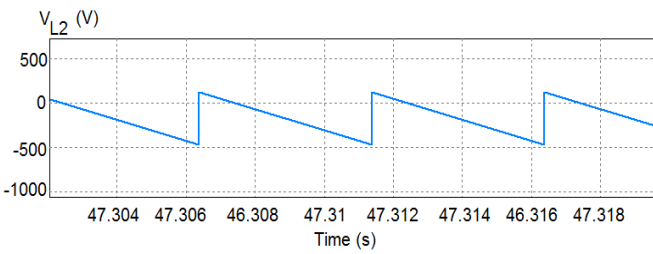**Figure 12.** Voltage across the inductor L_1

Figure 13. Voltage across the inductor L_2
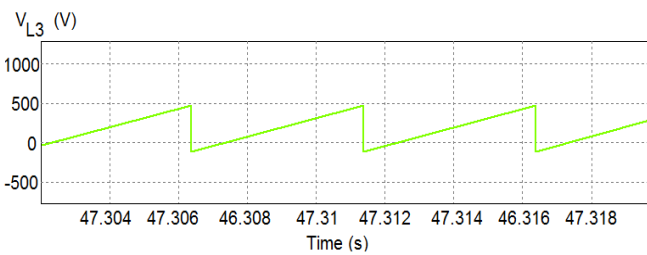

Figure 14. Voltage across the inductor L_3
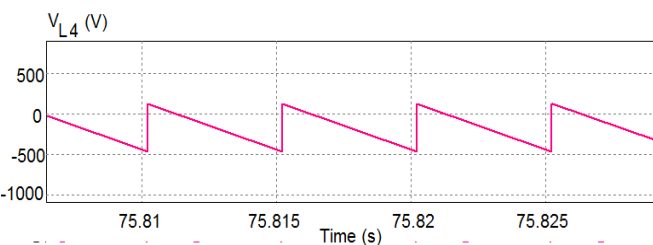

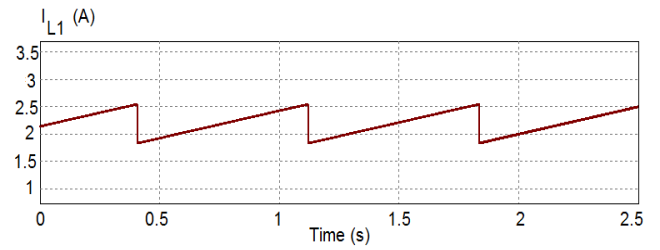**Figure 15.** Voltage across the inductor L_4

Figure 16. Current through the inductor L_1
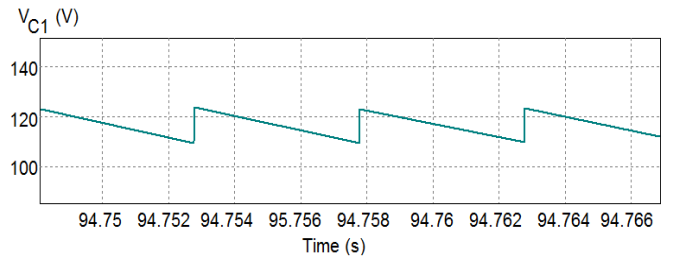

Figure 17. Voltage across the capacitor C_1
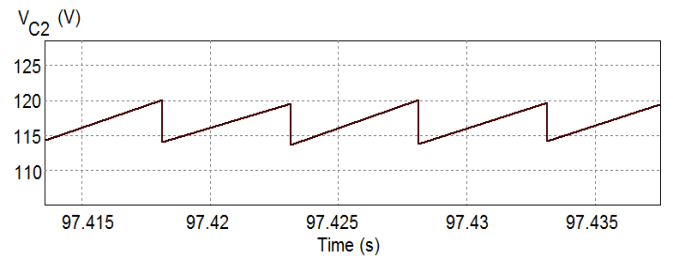

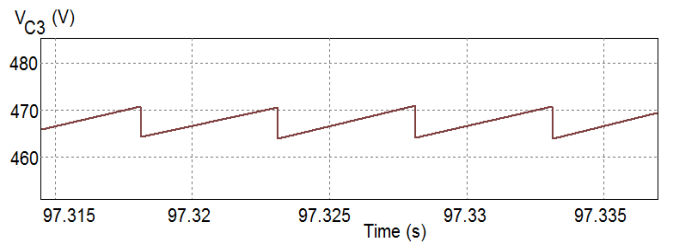**Figure 18.** Voltage across the capacitor C_2

Figure 19. Voltage across the capacitor C_3
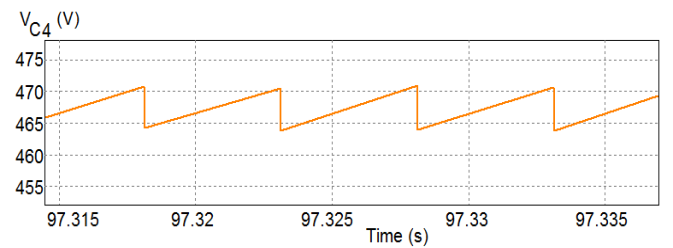

Figure 20. Voltage across the capacitor C_4
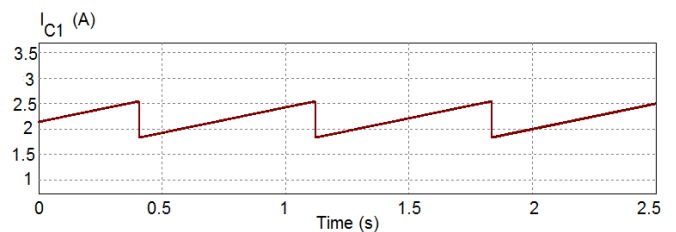

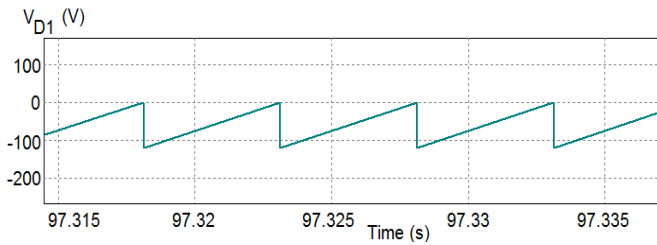**Figure 21.** Current through the capacitor C_1

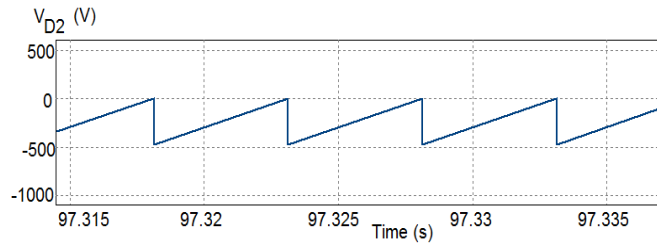**Figure 22.** Voltage across the Diode D_1

Figure 23. Voltage across the Diode D_2
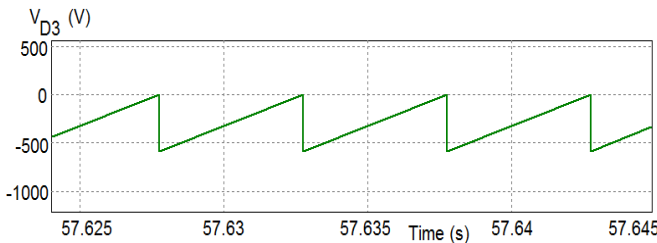

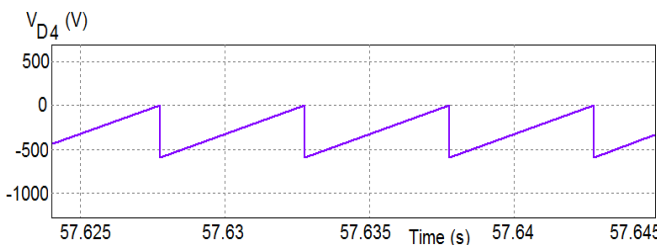**Figure 24.** Voltage across the Diode D_3

Figure 25. Voltage across the Diode D_4
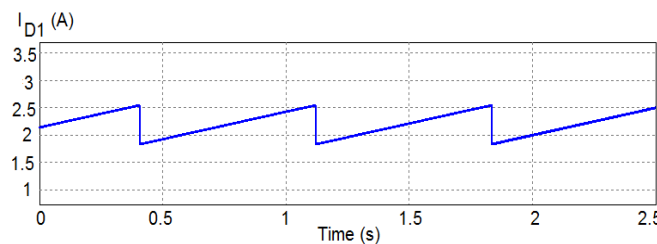

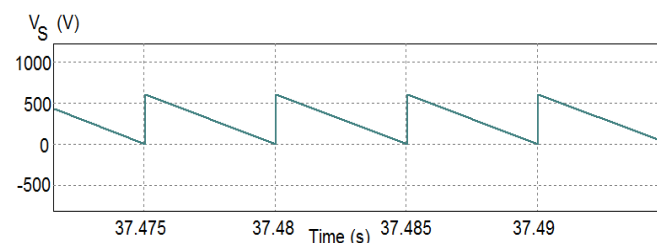**Figure 26.** Current through the Diodes

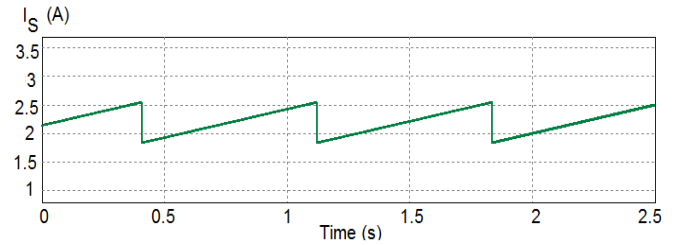**Figure 27.** Voltage across the Switch S

Figure 28. Current through the Switch S

4. CONCLUSIONS

In this paper, the continuous inductor current mode analysis in terms of modes of operation and steady-state behavior of a non-isolated high step-up positive output DC-DC conversion scheme is presented in open-loop configuration with and without diode-capacitor voltage expander module. The PSIM simulation tool has been employed to validate the performance of the proposed converter topology. The results of simulation shown for duty ratio D = 0.7 demonstrate that the suggested converter configuration has the ability to realize a high level of DC output voltage which is almost fifteen times the DC input voltage. The improved DC output voltage profile is mainly due to the presence of diode-capacitor voltage multiplier cell. The waveforms of output voltage and output current are shown to have fewer amounts of ripples due to the proper selection of filter components. The static voltage gain of the converter has been derived in open-loop mode. The gain derived is twice that of the converter proposed in [33]. The well-suited area of applications of the proposed converter is for high voltage renewable energy systems. The voltage and current waveforms of non-dissipative elements, diodes, and active switch are also analyzed for performance validation of the converter. The converter configuration suggested in this work employs a single MOSFET switch which is subjected to lower amounts of voltage and current stresses. In future work, the zero-voltage-switching concept may be employed for the switch in view of reduction of switching loss so that the converter efficiency may be improved.

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NOMENCLATURE

D	Duty ratio of the active switch
L_1, L_2, L_3, L_4	Inductances of inductors, mH
C_1, C_2, C_3, C_4	Capcitances of capacitors, μF
C_0	Filter capacitance, mF
V_{in}	Input DC voltage, V
V_0	Output DC voltage, V

Subscripts

in	input
o	output
L	load