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Contribution of Multilevel Inverters in Improving Electrical Energy Quality: Study and Analysis

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ABSTRACT

The work proposed in this paper concerns the study of harmonic pollution generated by static converters, particularly inverters, which largely contributes to the degradation of the supplied electrical energy quality. So, we studied in first the EMC of the conventional two-level inverter to highlight the harmful pollution of this kind of converter. We then looked at multi-level inverters to characterize their degree of pollution according to their number of levels in order to propose practical solutions for industrial applications. Thus, we considered three structures of multi-level inverters namely: a diode clamped inverter, a flying capacitor clamped inverter and a cascaded h-bridge inverter. At the end of this study, we retain that these three structures make it possible to obtain a waveform of the output voltage close to the sinusoidal form. The results of simulation obtained and compared to the STD international standard templates, also allowed us to conclude that among the three structures studied the cascaded h-bridge inverter is the most interesting from the electrical energy quality point of view. In addition, this converter has the advantage of owning a reduced number of switches which results in a weight and a cost, better than those of the other two studied inverters.

1. INTRODUCTION

In recent years, the evolution of power electronics was very important in a world where energy aspects became an essential issue. Otherwise, applications of power electronics are diverse and span a broad field of electrical engineering ranging from a few watts to several hundred megawatts [1-2]. The static conversion structures that mainly make up the applications of this discipline are becoming more and more powerful requiring an adaptation of technology to this evolution. The latter was allowed thanks to the development of semiconductor components technologies [3-5]. The evolution of voltage and current levels and the improved performance of these components have enabled the use of a more efficient power electronics devices for higher power applications [6]. Nevertheless, the current components performances do not allow to have an optimal conversion of the electrical energy. Indeed, the increase in voltage is often used to improve yields [7]. However, the use of components with high voltage amplitudes does not improve the overall efficiency of the installation; they deteriorate it because these components are generally less efficient than components with lower voltage amplitudes and therefore produce more losses [8].

Otherwise, from the energy quality point of view, electrical disturbance means any deviation of the network voltage from its shape and nominal value. By extension, we can also consider as disturbances the phenomena acting on the current shape because they have a direct influence on the voltage. Disturbances have adverse effects on electrical equipment, which usually manifests by warm-ups, causing the functioning degradation that could lead to a total destruction of these equipments [9-12]. To deal with this situation, traditional and modern solutions have been proposed. However, traditional solutions, based on passive circuits calculated in accordance with the harmonic's rows to filter, involve a larger space and the presence of the resonance phenomenon associated to these circuits. In addition, the passive filters cannot adapt to the network evolution, the polluting load and therefore constitute medium efficiency solutions. Advances in the field of power electronics have favored the implementation of static converters which constitute the modern solutions. Indeed, the latter are less cumbersome and do not cause any resonance phenomenon with the electrical network elements and show great flexibility in view of power network and pollutant load evolution [13, 14].

These converters absorb non-sinusoidal currents, so they behave like generators of harmonic currents. In this case the fundamental of the current is not in phase with the voltage, we have a reactive power consumption, that is, the power consumed is greater than the real active power. To reduce or eliminate these disturbances and thus improve the distributed electrical energy quality, several solutions exist. Among these solutions, we can quote the modification of the polluting static converter in terms of topology and/or control in order to intervene directly at the disturbances source [15]. In this objective, new structures of static converters have been developed. These structures are called multilevel converters because they have more than two voltage levels output.

2. INTEREST AND CONCEPT OF MULTILEVEL INVERTERS

An inverter is referred to as multilevel when it generates an output cut-out voltage composed of at least three levels. This type of converter has essentially two advantages. Firstly, multilevel structures allow the limitation of voltage constraints suffered by power switches: each power switch, when in the off state, supports a much lower fraction of the full DC bus voltage than the number of levels is high. On the other hand, the output voltage delivered by multilevel inverters have interesting spectral qualities [16, 17].

Otherwise, these inverters include a set of power switches and voltage sources. Through appropriate connection and control, they can generate a multi-step voltage wave shape with variable and controllable frequency, phase and amplitude.

The multilevel inverter output waveform is synthesized by controlling power switches [18]. Figure 1 helps to understand how these converters work [16, 18]. The action of power switches is represented by an ideal multi-position switch. A two levels inverter generates an output voltage with two values (2 levels), while the three levels converter generates three voltages (3 levels), and so on. The two-level converters can generate a voltage waveform of variable frequency and amplitude by adjusting a time average of the two voltage levels, which is usually performed with pulse width modulation techniques (PWM) [18, 19]. Multilevel inverters have voltage level as another degree of control freedom to generate the output signal to improve the output signal quality. In general, these converters can be seen as voltage synthesizers, in which the output voltage is synthesized from several discrete voltage levels [20, 21].

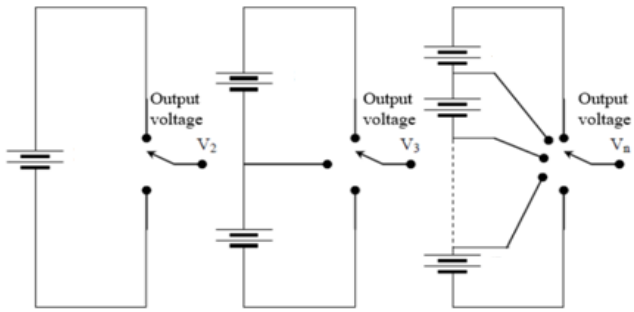

Figure 1. Multilevel converters [20]

3. INVERTERS TOPOLOGIES

3.1 Topology of a conventional three-phase two-level inverter

We can realize a three-phase two-level inverter by grouping, in parallel, three single-phase inverters (half bridge) and control the switches of each to obtain at the output three-phases shifted by 120°. In fact, by grouping three single-phase half-bridges, a three-phase bridge inverter with six switches is obtained, as shown in Figure 2. In the latter, switches on the same arm of the inverter must be complementary so that the DC input voltage is never short-circuited and the currents circuits ia, ib and ic are never open [22]. So that switches can impose the output voltages, whatever the load currents, they must be bidirectional in current. Each of them consists of a controlled opening and a closing power semiconductor and an antiparallel mounted diode. These switches can be chosen according to the power to be controlled [21, 22].

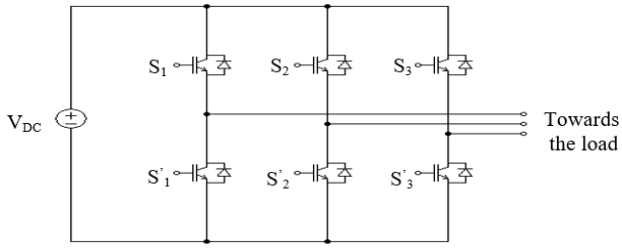

Figure 2. Structure of a conventional three-phase voltage inverter

3.2 Multilevel inverter topologies

Currently, with the emergence of new power electronics components, research activities focus on the analysis and development of multilevel inverter structures, for implementation within higher performance or more powerful applications [18, 23]. These areas of activity require the use of high voltages; consequently, the idea of using components with having high voltage calibers is not done without counterparty. Indeed, increasing the voltage withstand of the components generates a significant deterioration of the static and dynamic characteristics. So, these components are less efficient than those with low voltage calibers. To solve this problem and use more efficient components, new structures have been developed [3, 23]. These structures are called multilevel inverters because they have more than two output voltage levels. These converters consist in putting in series the power switches in order to increase the switched voltage and to distribute the voltage stress on different switches. They also allow the use of low caliber components which are therefore less expensive and more efficient [3, 23]. The advantage of these structures lies in their ability to improve the waveforms and the harmonic spectra of the output quantities.

Two categories of multilevel inverters are currently listed. The first category groups the main inverters into three groups [3, 13, 14, 19, 23-25]:

(1) Neutral point clamped multilevel inverter (NPC).
(2) Flying capacitor multilevel inverter (FC).
(3) Cascaded H-bridge multilevel inverter (CHB).

The second category of multilevel inverters includes the hybrid assemblies of inverters of the first category [3, 13, 14, 19, 23-25].

3.2.1 Neutral point clamped multilevel inverter (NPC)

The fast evolution of manufacturing techniques for semiconductor devices and the orientation of the designers towards hybrid component technology, such as IGBT, allowed the development of new inverter structures. The NPC structure constitutes the first structure of multilevel inverters. This topology had intended to add an intermediate voltage level to the output voltage of a conventional inverter (two levels) in order to reduce harmonics [26, 27].

For the general case, Figure 3 shows the structure of an NPC N levels inverter [26]. The principle of this topology is the creation of N-2 capacitive middle points, by connecting capacitors in series. By connecting each of these points to the output, we obtain N voltage levels. These voltage levels are obtained by controlling the power switches signals [28-31].

Thus, for each output voltage level, there is only one possible configuration for the arm. The disadvantage of this topology lies in the fact that the clamp diodes are exposed to a voltage greater than V_{DC}/N-1. This involves a series of diodes to achieve a high voltage value.

For a N levels inverter, the elements numbers characterizing this topology especially the number of continuous bus capacitors $N_{C_{DC}}$, the main switches number N_S, the main diodes number N_D and the clamping diodes number N_{cD}, are governed by the following relationships [18, 26, 32, 33]:

$$N_{C_{DC}} = N - 1 \quad (1)$$

$$N_S = 2(N-1) \quad (2)$$

$$N_D = 2(N-1) \quad (3)$$

$$N_{cD} = (N-1)(N-2) \quad (4)$$

The voltage across a capacitor threshold is given by the following equation [14, 18]:

$$U_c = V_{DC}/N - 1 \quad (5)$$

With V_{DC}: the total voltage applied to the inverter input.

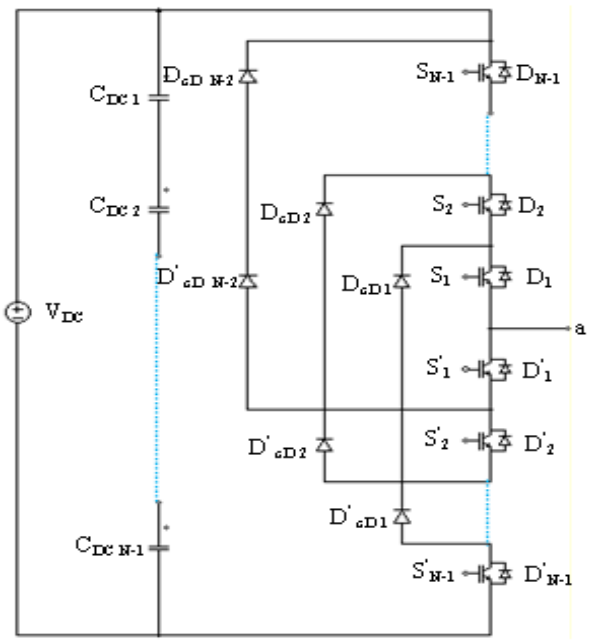

Figure 3. Neutral point clamped multilevel inverter arm

3.2.2 Flying capacitor multilevel inverter

The flying capacitor multilevel inverter or multicell converter is an energy conversion topology which is based on the serialization of controlled power switches. The operating principle of this topology is almost identical to that of the NPC topology. This structure is obtained by connecting loopback capacitor cells (Figure 4). Firstly, it solves the problem of voltage balance, and secondly it reduces the excessive number of diodes. In this topology, the capacitors replace the diodes, hence the name flying capacitor inverter [18, 34-36]. For an inverter with N levels the number of these capacitors is given by the following formula [14, 18, 37]:

$$N_{bc} = N - 2 \quad (6)$$

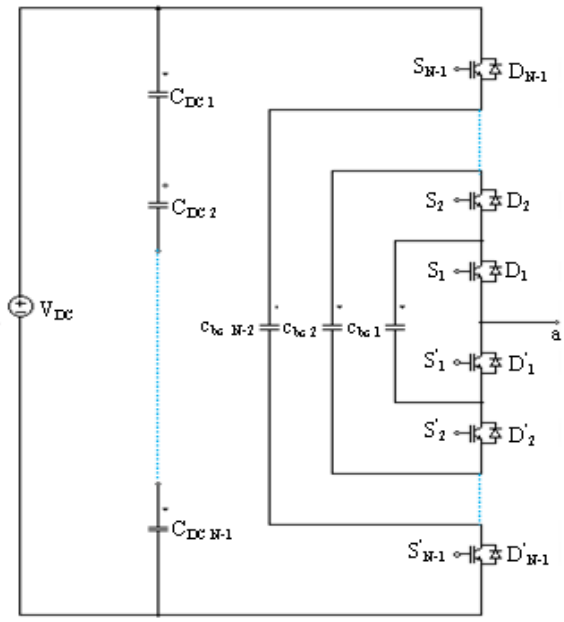

Figure 4. Flying capacitor multilevel inverter arm

3.2.3 Cascaded H-bridge multilevel inverter

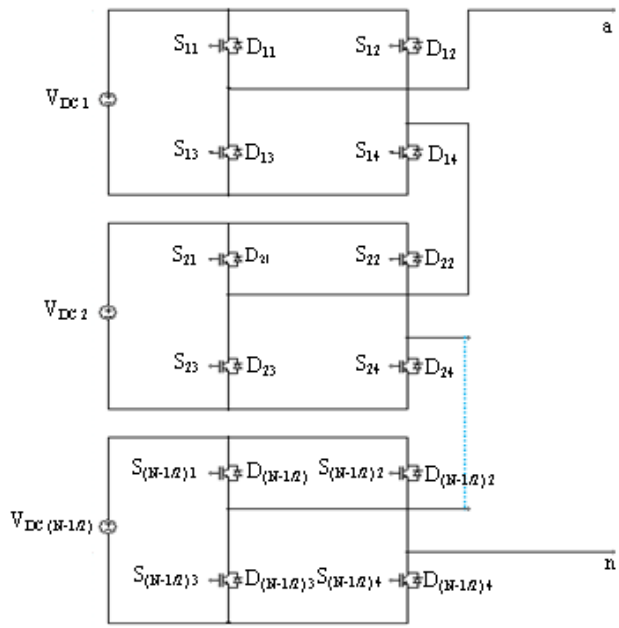

Figure 5. Cascaded H-bridge multilevel inverter arm

The principle of this structure is to connect in series several bridge single-phase inverters (four power switches) with isolated and independent voltage sources. The aim is to obtain a sinusoidal waveform composed of several levels of voltages. Figure 5 shows an inverter arm representative of this topology. Each single-phase inverter is powered by an independent voltage source. At the output of each single-phase inverter, one can have three different voltage levels, $+V_{DC}$, 0, $-V_{DC}$, by connecting the V_{DC} source to the output using different configuration of the power switches [14, 18]. The outputs of these inverters are connected in series so that the output waveform of the arm is equal to the sum each individual inverter voltages [18, 38-40].

$$V_{an} = V_{a1} + V_{a2} + \cdots + V_{a(\frac{N-1}{2})} \quad (7)$$

The number of single-phase bridges for each arm is given by the following formula [18, 39, 40]:

$$N_B = \frac{N-1}{2} \quad (8)$$

The use of single-phase bridge in series makes it possible the increase of the level voltage number and the converter power. However, the major disadvantage of this topology is the large number of isolated DC voltages required for each bridge. For a three-phase system, the output of the three arms can be connected in either a triangle or a star.

4. INVERTERS COMMAND STRATEGY

Pulse width modulation technique (PWM) is the growth and the fruit of the power electronics development. It is the heart of the static converters control. It is the most used for controlling inverters. It consists of comparing a reference or modulating wave (Vr), generally sinusoidal (the signal to be synthesized) to a generally triangular carrier wave (Vc) [14, 22, 41-43]. The output signal changes state at each intersection of the modulator and the carrier. This technique can be considered as an extension of the cutting control principle in which the pulse duration is no longer regular but chosen in such a way as to eliminate the maximum of harmonics of low ranks which are difficult to filter.

The reference voltages, of the three-phase inverter, allowing generating a balanced three-phase voltage system are defined by the following equation system [22]:

$$\begin{cases} V_{ra} = V_m \sin(wt) \\ V_{rb} = V_m \sin(wt - 2\pi/3) \\ V_{rc} = V_m \sin(wt - 4\pi/3) \end{cases} \quad (9)$$

This technique is characterized by the modulation index (m) and the modulation rate (r). These two parameters are given respectively by the following equations [22]:

$$m = f_c/f_r \quad (10)$$

$$r = A_r/A_c \quad (11)$$

With:
fc: Switching frequency.
fr: Reference frequency.
Ac: Carrier amplitude.
Ar: Amplitude of the reference.

For inverters with a number of N levels greater than two, the classic sinusoidal technique with its unique triangular signal does not allow the generation of all required control signals. The sinusoidal modulation with multiple triangles is indicated to do it. This technique requires (N-1) triangular signals of the same frequency and the same amplitude. The modulation rate corresponding to multilevel inverters is given by the following expression [14, 22, 41]:

$$r = A_r/(N-1)A_c \quad (12)$$

Several variations of this technique can be found in the literature. In our work we used the phase disposition technique (PWM-PD).

5. SIMULATION RESULTS AND DISCUSSION

In order to make a comparison between the conventional three-phase inverter and the multilevel three-phase inverter, we performed several different simulations based on the indirect method (time simulations followed by frequency analyses). The study is based on the plot of the inverter output voltage waveform and also on the calculation of the total harmonic distortion (THD) of the latter. This rate is validated by the IEEE STD 519-2014 standard [44]. The principle of the study is to simulate the conventional inverter and the multilevel inverter with its different topologies by varying the number of levels from 3 to 31. We start our study by the conventional inverter (2 levels), and we are interested afterwards in the study of multilevel inverters of three structures namely: the neutral point clamped multilevel inverter, the flying capacitor multilevel inverter and the cascaded H-bridge multilevel inverter. The models used are illustrated in Figures 3, 4 and 5. The power switches are ideal diodes and IGBT transistors.

The simulation parameters are shown in Table 1 below.

Table 1. Key simulation parameters

Control		load		Source (V_{DC} (V))			
f_m	f_c	R	L	Conventional	Multilevel inverter		
Hz	kHz	Ω	H	inverter	NPC	FC	CHB
50	20	10	0.002	100	100		100/N-1

Figures 6, 8, 10, 12, 14, and 16 show the temporal variations of the inverter output voltage corresponding to the studied configurations. We have also represented respectively in Figures 7, 9, 11, 13, 15 and 17 their frequency spectra.

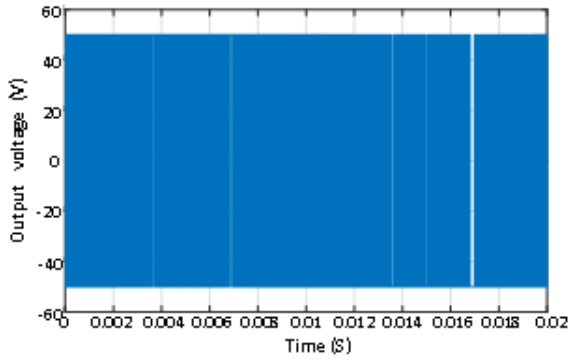

Figure 6. Inverter output voltage waveform for multilevel inverter (two levels)

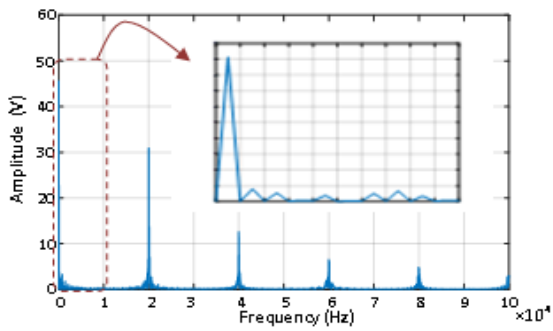

Figure 7. Frequency spectrum of the inverter output voltage for multilevel inverter (two levels)

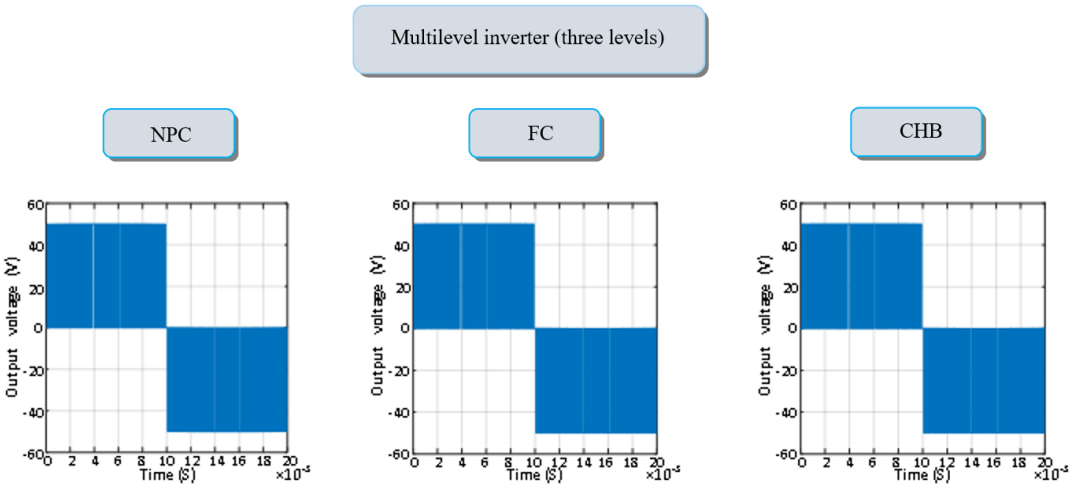

Figure 8. Inverter output voltage waveform for multilevel inverter (three levels)

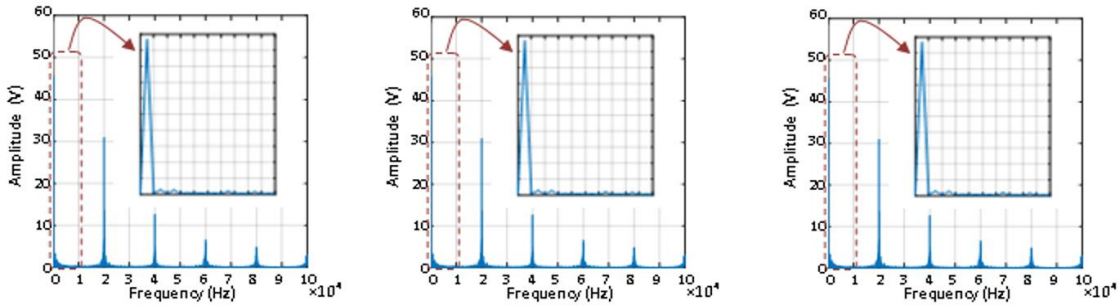

Figure 9. Frequency spectrum of the inverter output voltage for multilevel inverter (three levels)

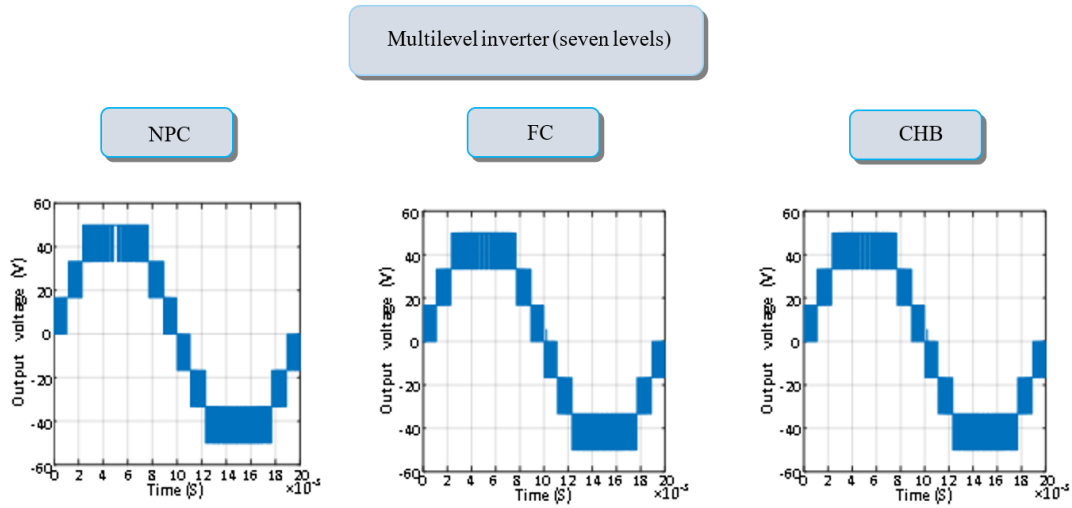

Figure 10. Inverter output voltage waveform for multilevel inverter (seven levels)

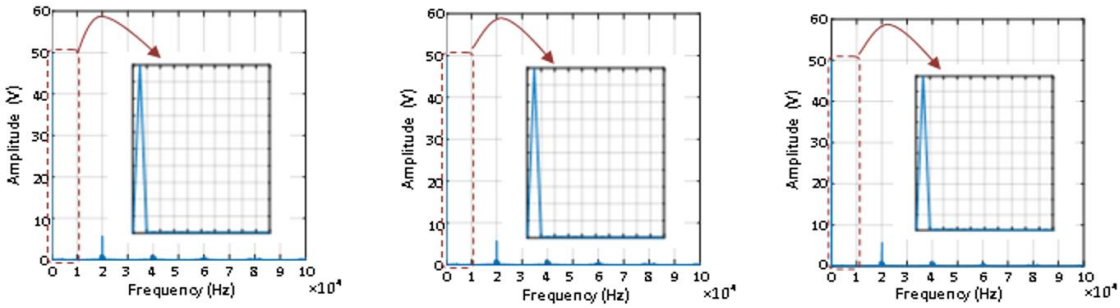

Figure 11. Frequency spectrum of the inverter output voltage for multilevel inverter (seven levels)

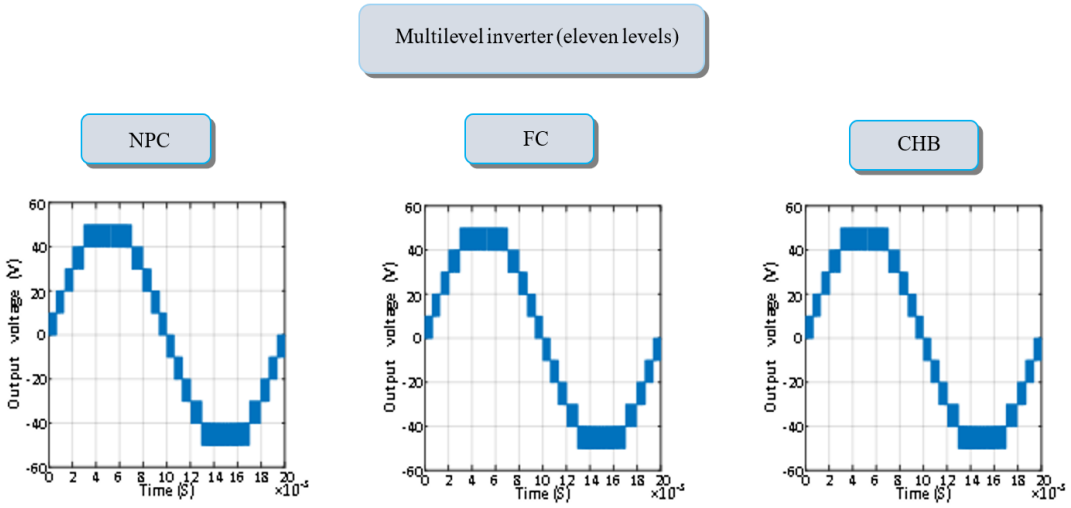

Figure 12. Inverter output voltage waveform for multilevel inverter (elven levels)

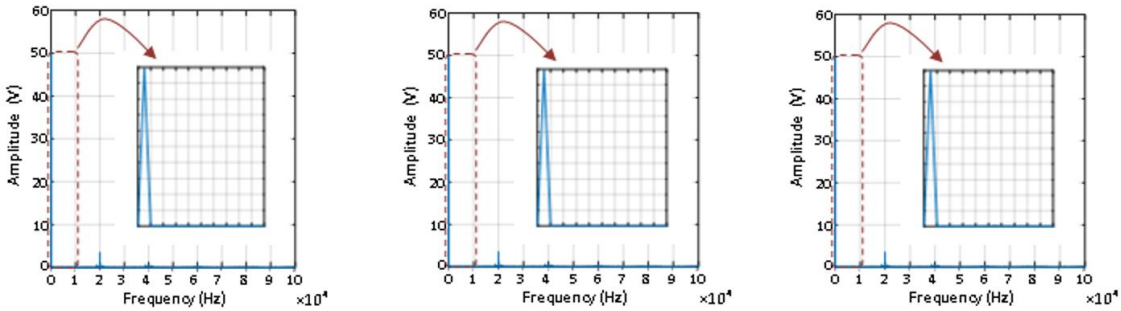

Figure 13. Frequency spectrum of the inverter output voltage for multilevel inverter (elven levels)

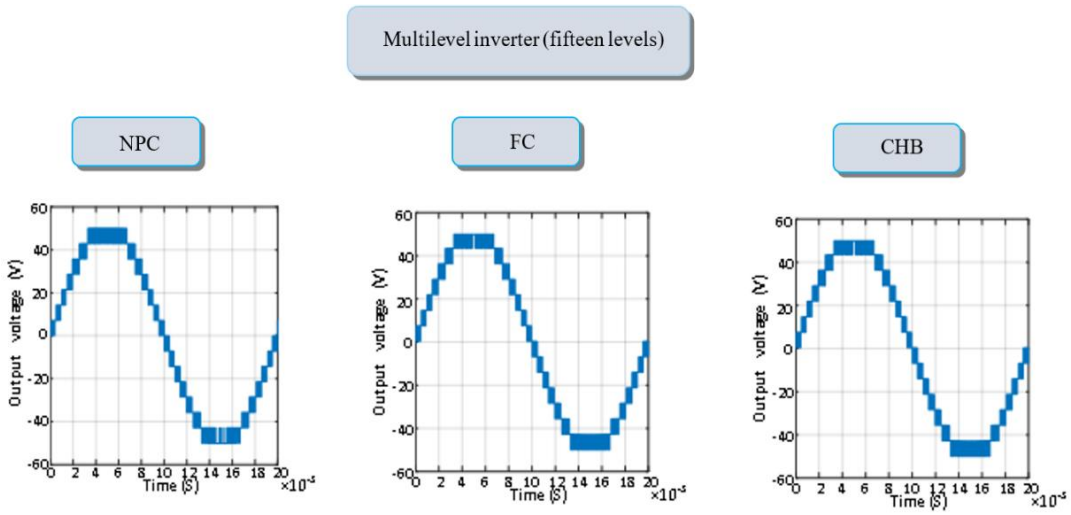

Figure 14. Inverter output voltage waveform for multilevel inverter (fifteen levels)

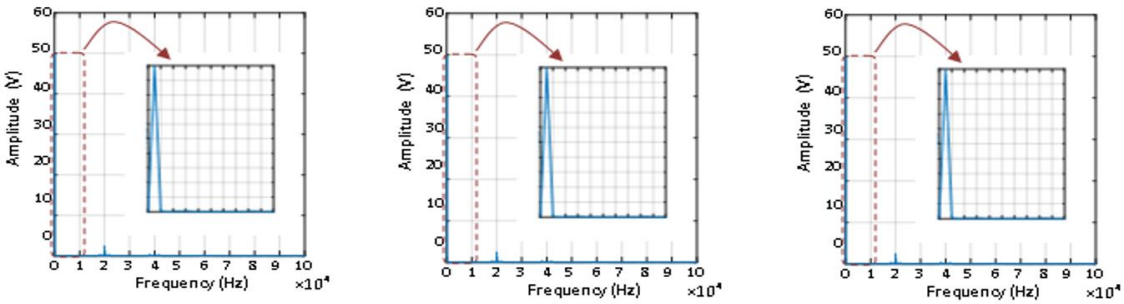

Figure 15. Frequency spectrum of the inverter output voltage for multilevel inverter (fifteen levels)

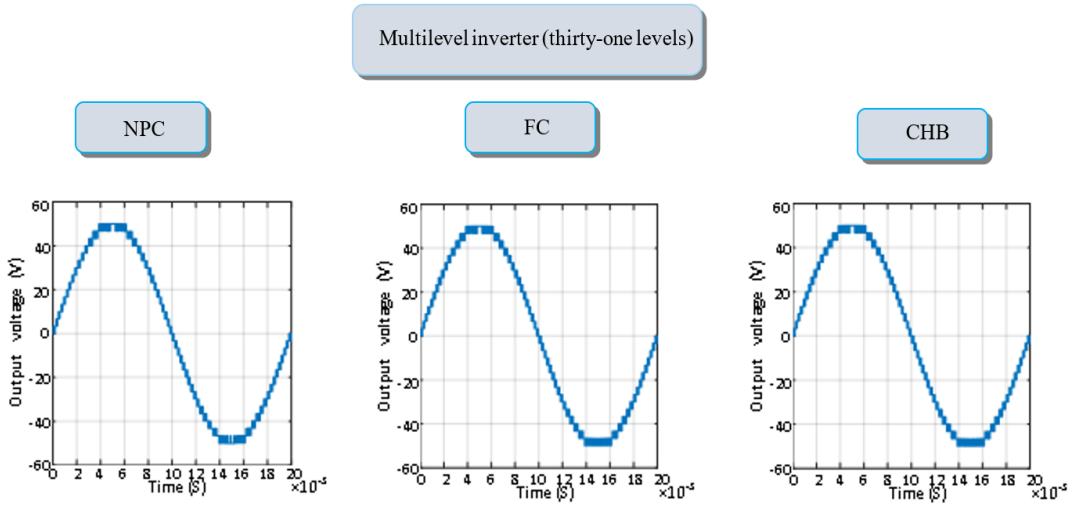

Figure 16. Inverter output voltage waveform for multilevel inverter (thirty-one levels)

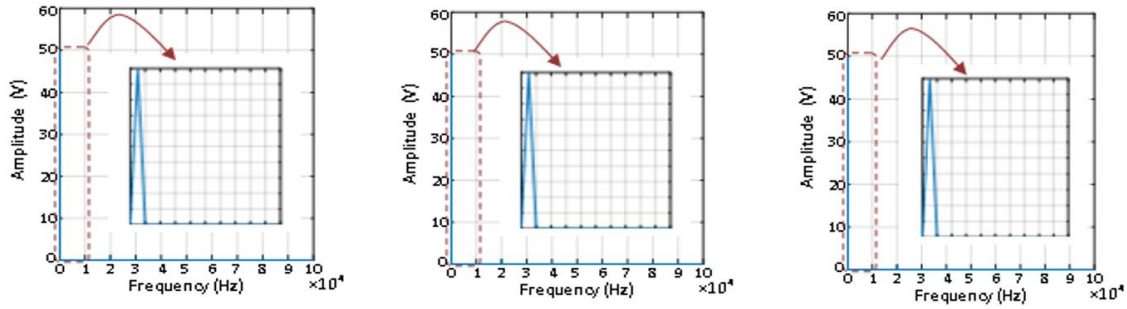

Figure 17. Frequency spectrum of the inverter output voltage for multilevel inverter (thirty-one levels)

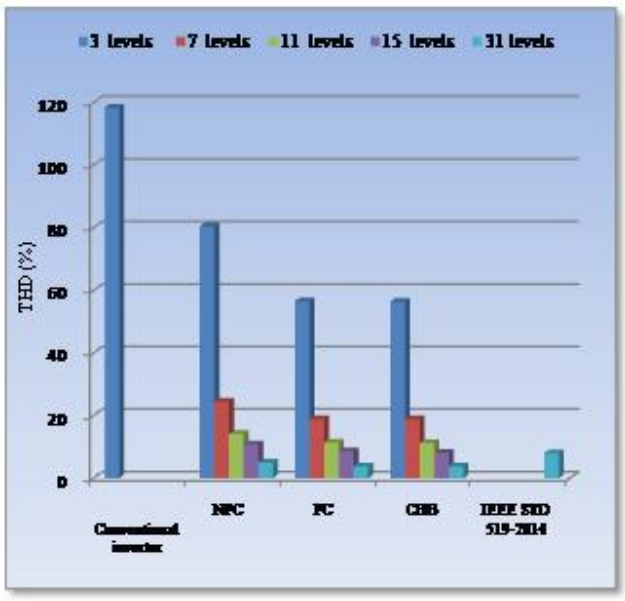

Figure 18. Comparison of voltage THD among various topologies of multilevel inverters and the IEEE STD standard

Analysis of these results shows that the voltage is distorted. This distortion is very important in the case of the conventional inverter (2 levels) and inversely proportional to the levels number (N) in that of multilevel inverters. We can therefore conclude that, the increase in the level's number leads to an improvement in the multilevel inverter output voltage waveform quality which approaches the desired sinusoidal shape. Indeed, the distortion is characterized on the frequency domain by the appearance of harmonic frequencies of odd rank whose amplitude decreases when the level's number increases.

Thus, we have postponed in Figure 18, the total harmonic distortion variation corresponding to the conventional and three multilevel inverters topologies for several levels. We also added in this same figure the template of the IEEE STD 519-2014 in order to know if the standard is met or not.

From these last results, we find that the conventional inverter has a very high total harmonic distortion (THD=118.424%) which greatly exceeds the limit allowed by the considered standard which is equal to 8% which explains the results found in temporal regime.

The results corresponding to the multilevel inverters show a noticeable decrease in the total harmonic distortion compared to the conventional inverter. In addition, we note that the harmonic distortion rate relative to the NPC topology is greater than the harmonic distortion rate relative to the FC and CHB topologies due to the presence of diodes in this topology.

Also, we can see that the increase in the number of levels leads to a reduction of the total harmonic distortion in the case of three multilevel inverter configurations.

Otherwise, we notice that the total harmonic distortion, relative to the three studied structures, exceeds the limit allowed by the IEEE STD 519-2014 for levels 3, 7, 11, 15. By contrast, the found value of the total harmonic distortion corresponding to level 31 does not exceed the limit specified by the IEEE STD 519-2014. At the end of this study, we can say that the cascaded h-bridge multilevel inverter is the most advantageous structure because we get at the output of the

latter a higher quality voltage. Indeed, the later does not require the use of a filter and whose topology comprises a reduced number of power switches and a total absence of capacitors (DC bus and balancing capacitors). Therefore, this reduces the cost, size, losses of the cascaded h-bridge multilevel inverter.

6. CONCLUSIONS

In this paper we studied the EMC of three multilevel converters structures in order to have a good quality of the supplied electrical energy.

The ultimate goal was to identify the least polluting structure that can be used in complex devices such as electric vehicles.

The obtained results, after simulation of the three considered converters, allows us to state that overall the output voltage waveform of the three converters is close to the sinusoidal form. Furthermore, we showed in this work that when the levels number increases the number of harmonics and their amplitudes decrease which results in a decrease in the total harmonic distortion. We have also shown through this study, that in the case of the cascaded h-bridge multilevel inverter the number of required power switches is reduced compared to the case of the neutral point clamped multilevel inverter and that of the flying capacitor multilevel inverter. So, from the EMC point of view (better electrical energy power quality), we recommend the use of the cascaded h-bridge multilevel inverter. However, in the practical choice of the converter it will be necessary to take into account in addition to the EMC aspect the converter cost, its volume and the involved losses.

A compromise will have to be found between these different parameters in order to decide on the final choice of the converter to use in a given application.

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