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A Dual Frequency Compensation Technique to Improve Stability and Transient Response for a Three Stage Low-Drop-Out Linear Regulator

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ABSTRACT

A novel internal compensation technique named dual frequency compensation is proposed to improve the stability and the transient response of the on-chip output capacitor three stage low-drop-out linear voltage regulator (LDO). It exploits a combination of amplification and differentiation to sufficiently separate the dominant pole from the first non-dominant pole so that the latter is located after the unity gain frequency regardless of the load current value. The proposed LDO regulator is analyzed, designed, and simulated in standard 0.18 µm low voltage CMOS technology. The presented LDO regulator delivers a stable voltage of 1.2 V for an input supply voltage range of 1.35-1.85 V with a maximum line deviation of 4.68mV/V and can supply up to 150mA of the load current. The maximum transient variation of the output voltage is 54.5 mV when the load current pulses from 150mA to 0mA during a fall time of 1µs. The proposed LDO regulator has a low figure of merit compared with recent LDO regulators.

1. INTRODUCTION

Many system-on-a-chip (SoC) applications integrate circuit blocks, such as digital, analog and radio-frequency blocks [1-4]. Charge pump regulators are commonly used to generate high voltages for lighting or memory units [5, 6]; switching converters are employed to regulate digital blocks, due to their high power efficiency [7, 8]; and low-drop-out linear voltage regulators are used to provide low noise supply voltage with very low ripple for noise sensitive blocks, such as analog/RF circuits [9, 10]. An example that highlights the present-day importance of voltage regulators and power management blocks can be found in ref. [11], where the power supply requirements for a Code-Division Multiple Access (CDMA) modem of a mobile phone are described. As shown in Figure 1, LDO regulators play a very important role in the integrated power management unit in modern portable electronic devices [11], they scales down the supply voltage to provide for many various other blocks.

An important issue in LDO voltage regulator design is stability, which has a direct impact on the transient response of this system. In addition, the downscaling of the supply voltage and the decrease of the intrinsic gain of the MOS transistor for nanometric CMOS technologies [12, 13] requires the use of multiple stages in the implementation of the LDO regulator, this degrades the close-loop response by the presence of multiple poles, hence the need to develop a robust compensation method. Compensation can be external or internal. Generally, external compensation is achieved with a high value capacitor in the order of µF [14]. As for internal compensation, Miller compensation is one of the most widely used techniques [10], but other techniques and approaches can be found in literature [15-28].

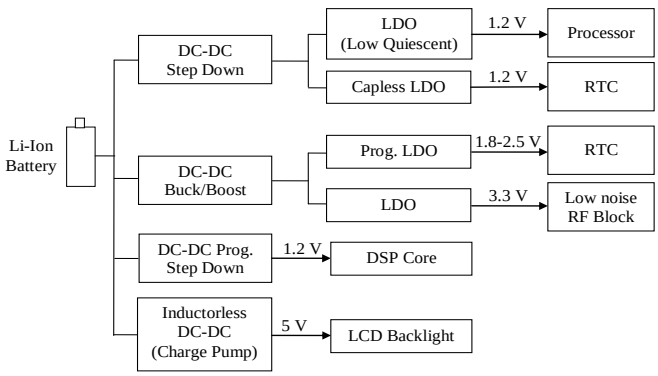


Figure 1. Power management unit in modern portable devices [11]

In this work a novel frequency compensation technique is proposed to achieve the stability for wide range of the load current for the LDO regulator and also enhance his transient response. In section 2, a literature review of stability enhancement is summarized. In section 3, the proposed LDO regulator circuit is given and detailed analysis is performed. In section 4, the simulation results are given to show the performance of the proposed LDO regulator in terms of stability, transient response and others parameters accompanied by a comparison with previous related works. Finally, in section 5, the simulation results are given to show the performance of the proposed LDO regulator in terms of

stability, transient response and others parameters accompanied by a comparison with previous related works.

2. LITERATURE REVIEW OF LDO STABILITY ENHANCEMENT

Many solutions have been proposed in the literature to improve the stability of LDO regulators with small current load values. One of the earliest proposals [15] uses a compensation block to control the damping factor [16]. This improves the stability of the system and increases the bandwidth. A variant of this work can be found in [17], where a block is introduced to control the quality factor of the pair of non-dominant complex poles. To save power, the active load of the differential pair of the error amplifier is reused as a current buffer. An additional branch is included to introduce a zero in the negative real half-plane with the twofold objective of improving the stability and increasing the maximum current at the gate of pass transistor. Unfortunately, every stage of the control circuit is loaded by compensating capacitors, which causes a decrease in the Slew-Rate (SR) of the LDO regulator. Capacitive multipliers were also used in [18-22]. As an example, in [18], a differentiator, formed by a capacitor and a current buffer, is introduced. This buffer serves a double purpose. First of all, it introduces a fast path between the output of the LDO regulator and the gate of pass transistor. Second, the buffer helps to separate the poles, since the capacitor appears at the gate of pass transistor multiplied by the gain of the current buffer. It is worth noting that the use of a current buffer is compatible with other compensation techniques. As an example, in [22], a current buffer is used as part of a classical Reverse Nested Miller Compensation (RNMC). In [23], adaptive power transistors technique is proposed to allow the LDO regulator to transform itself between two stage and three stage cascaded topologies with respective power transistor, depending on the load current condition. This later technique achieves high stability and good transient response. Most of these techniques and approaches suffer from the instability problem at very low load current, while several applications need the LDO regulator to hold the output and provide good performance under a no-load current condition such as CMOS RAM keep-alive applications.

To overcome the limitations of the classical internal compensation, an alternative topology called Flipped Voltage Follower (FVF) has been proposed [24]. This method has been well analyzed, developed and applied to the LDO regulator [25], it is characterized by a local feedback which makes it possible to achieve a low output impedance, and consequently to improve the SR at the gate of pass transistor, which improves the transient response as well as the stability, but because of the low value of the static gain generated by this method [25], the performance of the line and load regulations remains limited which degrades the transient response. To improve the performance of stability and regulation, several LDO regulators have been proposed, such as the one that uses the Cascode Flipped Voltage Follower [26], the multiple-loop LDO regulator based on the flipped voltage follower [27] and the LDO regulator with mixed internal compensation which marries the Miller compensation and the flipped voltage follower [28].

3. PROPOSED LDO REGULATOR

3.1 Main blocks of proposed LDO regulator

The diagram block of proposed LDO regulator is shown in Figure 2, while Figure 3 gives transistor implementation of proposed error amplifier (EA). For error amplifier design, a single-ended two-stage error amplifier with fully differential input is chosen [29], it consists of M_1-M_6 transistors, bias current $I_{B,EA}$ and common feedback resistor R_{CM}. A fully-differential PMOS M_1 input stage is used to achieve high power supply noise rejection. The third stage is composed by the PMOS pass transistor M_P to achieve low dropout voltage [10]. The feedback network is composed by the resistors R_{FB1} and R_{FB2}. R_L is the load resistor which models the low voltage system-on-chip powered by the LDO regulator output. The load capacitor C_L is integrated on chip, which is essential to improve the transient response. V_I is the power supply input voltage, V_{REF} is the reference voltage provided by another sub-circuit, $V_{G,P}$ represent the voltage at the gate of pass transistor M_P. V_O is the output voltage of LDO regulator. The compensation network will be clarified later in this section.

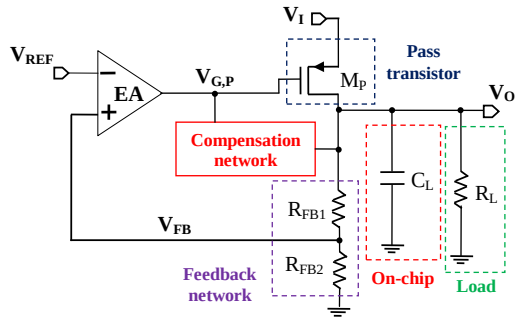


Figure 2. Block diagram of the proposed LDO regulator

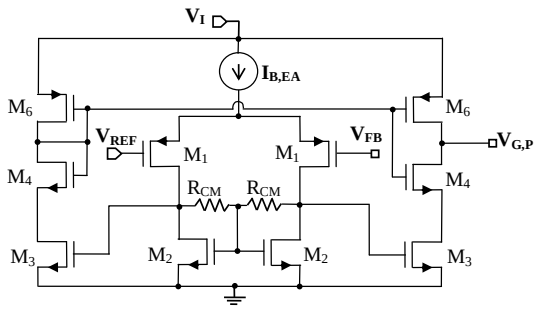


Figure 3. Proposed error amplifier (EA)

3.2 Stability analysis

3.2.1 Uncompensated frequency response

To determine the uncompensated open-loop transfer function, of the proposed LDO regulator system, defined by Eq. (1), a small signal model is established and it is represented in Figure 4. By applying the Kirchhoff current laws, we obtain the transfer function $H_{ol,u}(s)$ given by Eq. (2). Where, $H_{0,u}$ is the DC gain given by Eq. (3), where β is the feedback factor expressed by Eq. (4). g_{m1} is the transconductance of the EA first stage which is equal to that of transistor M_1 and $R_{O1,EA}$ represents the output resistance of the EA first stage expressed by Eq. (5), where r_{o1} and r_{o2} represent the small output resistances of transistors M_1 and M_2, respectively. g_{m3} and $g_{m,P}$

represent the transconductance of EA second stage, which is equal to that of transistor M_3, and the transconductance of pass transistor M_P, respectively. r_{o6} is the small signal output resistance of EA second stage which is equal to small signal output resistance of transistor M_6. R_O is the output resistance of LDO regulator given by Eq. (6), where $r_{o,P}$ is the output resistance of M_P. Note that s denotes the complex variable of Laplace.

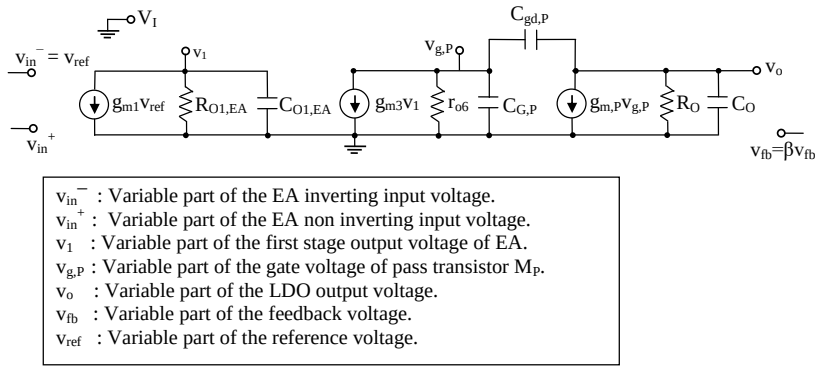


Figure 4. Small signal model of the proposed uncompensated LDO

$$H_{ol,u}(s)=\frac{v_{fb}}{v_{ref}} \tag{1}$$

$$H_{ol,u}(s)=\frac{H_{0,u}(1+\frac{s}{z_{RHP}})}{(1-\frac{s}{p_d})(1-\frac{s}{p_{nd}})(1-\frac{s}{p_3})} \tag{2}$$

$$H_{0,u}=-\beta g_{m1}g_{m3}g_{m,P}R_{O1,EA}r_{o6}R_O \tag{3}$$

$$\beta=\frac{R_{FB2}}{R_{FB1}+R_{FB2}} \tag{4}$$

$$R_{O1,EA}=r_{o1}//r_{o2}//R_{CMFB} \tag{5}$$

$$R_O=r_{o,P}//(R_{FB1}+R_{FB2})//R_L \tag{6}$$

The transfer function contains a right half-plane (RHP) zero z_{RHP} given by Eq. (7), where $C_{gd,P}$ is the parasitic drain-to-source capacitance. The frequency location of z_{RHP} changes with load current I_L (or value of R_L), because $g_{m,P}$ and $C_{gd,P}$ change with I_L and this is due to the fact that M_p changes the region of operation according to the variation range of I_L [9].

$$z_{RHP}=\frac{g_{m,P}}{C_{gd,P}} \tag{7}$$

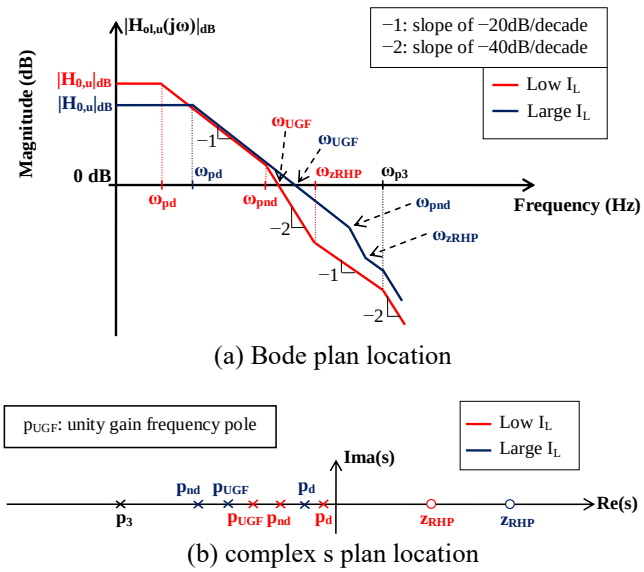
According to Eq. (2), the transfer function contains three left half-plane (LHP) poles p_d, p_{nd} and p_3, where their locations change relatively with the load current. The dominant pole p_d is located at the gate node of M_P ($v_{g,P}$ voltage in Figure 4) due to the large value of $C_{G,P}$ and r_{o6}, where $C_{G,P}$ represents the total capacitance connected between the M_P gate and the small signal ground. The non-dominant pole p_{nd} is located at the output node (v_o voltage in Figure 4). The third pole p_3 represents the high frequency pole and it's located at the first stage output node of EA (v_1 voltage in Figure 4). This last pole is independent of the load current and therefore does not affect the stability. For the proposed LDO regulator design, M_P operates in sub-threshold region when the load current is at its minimum value $I_{L,min}$, while it operates in the saturation region at the maximum value $I_{L,max}$ of load current. In this case the approximate expressions of these three poles are given by:

$$p_d\approx-\frac{1}{r_{o6}(g_{m,P}R_OC_{gd,P}+C_{G,P})+R_OC_O} \tag{8}$$

$$p_{nd}\approx-\frac{r_{o6}(g_{m,P}R_OC_{gd,P}+C_{G,P})+R_OC_O}{R_{o6}R_O(C_{gd,P}+C_{G,P})C_O} \tag{9}$$

$$p_3\approx-\frac{1}{R_{O1,EA}C_{O1,EA}} \tag{10}$$

where, $C_{G,P}=C_{O2,EA}+C_{gd,P}$ and $C_O=C_L+C_{db,P}$. $C_{O1,EA}$ and $C_{O2,EA}$ represent the output capacitances of EA first stage and EA second stage, respectively. $C_{gd,P}$, $C_{gs,P}$ and $C_{db,P}$ represent the parasitic capacitances gate-to-drain, gate-to-source and drain-to-bulk of the pass transistor M_P.



(a) Bode plan location

(b) complex s plan location

Figure 5. Pole-zero location with load current variation

Figure 5 shows the dependence of zeros and poles location on the load current I_L in the Bode plan and in the complex s

plane, respectively. The frequency location is presented in term of angular frequency ω, where $\omega_{zRHP}=z_{RHP}$, $\omega_{pd}=-\omega_{pd}$, $\omega_{pnd}=-p_{nd}$ and $\omega_3=-p_3$. For low I_L, the RHP zero is located in the middle frequencies, which introduces a phase shift of −90°, this pushes the non-dominant pole towards the low frequencies, before the unity gain angular frequency ω_{UGF}. Therefore the magnitude curve in the Bode diagram intersects the frequency axis by a slope of −40 dB/decade and consequently the LDO regulator is unstable. For a case of the large load current, the RHP zero is pushed in the high frequencies, the non-dominant pole is located after the unity gain frequency, so the phase margin is positive but insufficient (less than 45°) to stabilize closed loop response of the LDO regulator system.

It is clear that to stabilize the LDO regulator, it is necessary to separate the dominant and non-dominant poles while keeping a phase margin greater than 45 degree for the entire load current range required by the specifications and keeping higher the unity gain frequency to have a fast transient response, this is achieved by adding a LHP zeros well placed with respect to the non-dominant pole and unity gain frequency locations.

3.2.2 Compensated frequency response

To stabilize the proposed three stage LDO regulator, a dual compensation circuit has been inserted between the LDO output and the pass transistor gate. The compensation network is given by Figure 6. It is composed of two differentiator-current amplifier blocks, (C_{C1}, R_{C1}, M_7, M_8) and (C_{C2}, R_{C2}, M_9, M_{10}), whose role is to separate the dominant pole from the first non-dominant pole and to create LHP zeros to increase the phase margin. The proposed compensation block has no effect on the elimination of the RHP zero. The compensation circuit requires a symmetrical bias current $I_{B,C}$. The cascode trasistors M_{7c}, M_{8c} and M_{13c} help to minimize the effect of channel length modulation to improve matching performance.

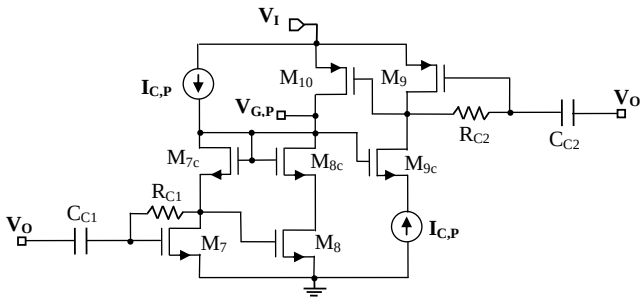


Figure 6. Transistor MOS implementation of proposed frequency compensation circuit

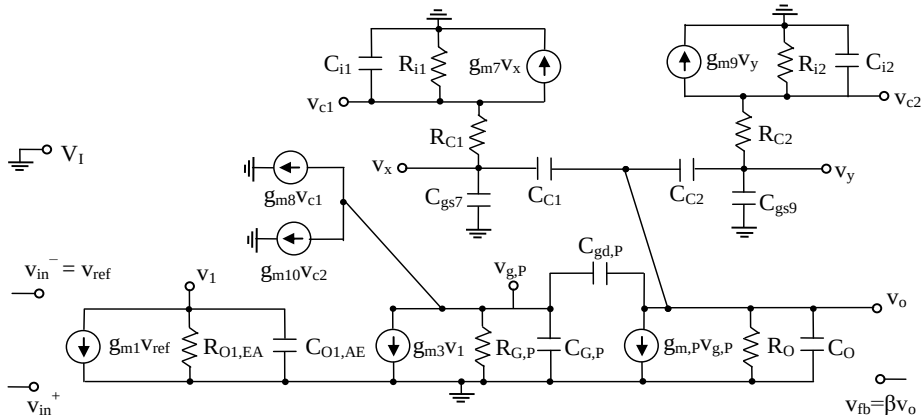


Figure 7. Small signal model of LDO regulator with proposed compensation circuit

To determine the open loop transfer function $H_{ol,c}(s)$ of the compensated system, the small-signal equivalent model was made as shown in Figure 7. By application of Kirchhoff's current law and after some mathematical manipulations and some justified simplifications, we find that $H_{ol,c}(s)$ can be expressed as:

$$H_{ol,c}(s) \approx \frac{H_{0,c}\cdot(1+\frac{s}{z_{RHP}})(1-\frac{s}{z_1})(1-\frac{s}{z_2})}{(1-\frac{s}{p_d})(1+\frac{a_2}{a_1}s+\frac{a_3}{a_1}s^2)(1+\frac{a_4}{a_3}s)(1-\frac{s}{p_5})} \quad (11)$$

where,

$$H_{0,c} = -\beta g_{m1} g_{m3} g_{m,P} R_{O1,EA} R_{G,P} R_O \quad (12)$$

$$R_{G,P} = r_{o6} // r_{o10} // (g_{m8} r_{o8}^2) \quad (13)$$

$$z_1 \approx -\frac{1}{R_C C_C} \quad (14)$$

$$z_2 \approx -\frac{4}{R_C C_C} \quad (15)$$

$$p_d \approx -\frac{4}{R_{G,P} g_{m,P} R_O [(g_{m10}+g_{m8}) R_C C_C + C_{gd,P}]} \quad (16)$$

$$a_1 \approx \frac{R_{G,P} g_{m,P} R_O [(g_{m10}+g_{m8}) R_C C_C + C_{gd,P}]}{4} \quad (17)$$

$$a_2 \approx \frac{R_C^2 C_C^2}{4} + R_{G,P} C_{G,P} R_O (C_O + C_{C,tot} + C_{gd,P}) + \frac{R_C C_C}{2}[R_{G,P} C_{G,P} + R_O (C_O + C_{C,tot} + C_{gd,P})] \quad (18)$$

$$a_3 \approx \frac{R_C^2 C_C^2}{4}[R_{G,P}C_{G,P} + R_O(C_O + C_{C,tot} + C_{gd,P})] + R_{G,P}C_{G,P}R_O(C_O + C_{C,tot} + C_{gd,P})\frac{R_C C_C}{2} \quad (19)$$

$$a_4 \approx \frac{R_C^2 C_C^2}{4}\left(\frac{C_{i1}}{g_{m7}} + \frac{C_{i2}}{g_{m9}}\right)R_{G,P}C_{G,P} + \frac{R_C^2 C_C^2}{4}\left(\frac{C_{i1}}{g_{m7}} + \frac{C_{i2}}{g_{m9}}\right)R_O(C_O + C_{C,tot} + C_{gd,P})] + \frac{R_C^2 C_C^2}{4}R_{G,P}C_{G,P}R_O(C_O + C_{C,tot} + C_{gd,P}) \quad (20)$$

$$p_5 \approx -\frac{1}{R_{O1,EA}C_{O1,EA}} \quad (21)$$

$H_{0,c}$ represents the DC gain of compensated LDO whose value is very close to the value of $H_{0,u}$ previously expressed by Eq. (3). $R_{G,P}$ is the total equivalent resistance connected between the gate node of M_p and ground. It also includes the output resistances of the two current amplifiers of the compensation circuit as shown by its expression given by Eq. (13). In the term a_1, gm_8 and gm_{10} represent the transconductances of the amplifying transistors M_8 and M_{10} of the compensation circuit, respectively. In the term a_4, g_{m7} and C_{i1} represent the transconductance of M_7 and the equivalent input capacitor of differentiator-current amplifier (C_{C1}, R_{C1}, M_7, M_8) in compensation circuit. Likewise, g_{m9} and C_{i2} represent the transconductance of M_9 and the equivalent input capacitor of differentiator-current amplifier (C_{C2}, R_{C2}, M_9, M_{10}).

The dominant pole p_d is located at the gate of M_P. z_1 and z_2 are the LHP zeros created by the compensation circuit, where RC represent the compensation resistance such as $R_{C1}=R_{C2}=RC$ and C_C is the compensation capacitance such as $C_{C1}=C_{C2}=C_C$. The analysis shows that the non-dominant pole corresponds to two complex conjugate poles which are the roots of the polynomial equation presented in the denominator of Eq. (11). The two complex conjugate poles p_2 and p_3 are given by Eq. (22), where ω_0 is the corner angular frequency given by Eq. (23) and ζ represents the damping factor expressed by Eq. (24). When I_L continues to increase, the quality factor $Q=1/(2\zeta)$ increases, and the resonance phenomenon appears in the vicinity of the angular frequency ω_0, whose resonant angular frequency, noted ω_r, is expressed by Eq. (25). The fourth pole is given by $p_4=-(a_3/a_4)$, while the fifth pole p_5 is located at the output node of the error amplifier first stage. Note that the factorization of the numerator and the denominator of the transfer function was done by the method of time constants described in [30].

$$p_{2,3} = -\zeta.\omega \pm j\omega_0\sqrt{1-\zeta^2} \quad (22)$$

$$\omega_0 = \sqrt{\frac{a_1}{a_3}} \quad (23)$$

$$\zeta = \frac{a_2\omega_0}{2a_1} \quad (24)$$

$$\omega_r = \omega_0.\sqrt{1-2\zeta^2} \quad (25)$$

As shown in Figure 8, the location of the poles and the RHP zero of the compensated frequency response for proposed LDO changes relatively with load current I_L. Figure 8 shows that the transfer function corresponding to the frequency response of the proposed compensated LDO also contains two other LHP poles p_6 and p_7 and two other LHP zeros z_3 and z_4. In the case of the low load current, zero z_3 cancels pole p_6 and zero z_4 cancels pole p_7. Furthermore, the stability analysis shows that for certain low values of I_L, the two complex conjugate poles move towards the right half-plane. Not shown in this paper, Cardan's method [31], allows to solve a cubic equation whose solutions give the poles $p_{2,i}$ and $p_{3,i}$ represented in Figure 8. To avoid this potential instability, the gate width Wp of the pass transistor Mp must meet the condition given by constraint (26), where $C_O=C_L+C_{db,P}$ and $C_{C,tot}=2C_C$. $C_{gs,ov}$ and $C_{gd,ov}$ represent the overloop capacitance gate-to-source and gate-to-drain of M_P, respectively [29].

$$W_P \geq \frac{C_O + C_{C,tot}}{20C_{gs,ov} - C_{gd,ov}} \quad (26)$$

For the process used in the proposed design, $C_{gd,ov}=C_{gs,ov}=330$ pF/m. Generally $C_L=100$ pF and therefore we can neglect $C_{db,P}$ in front of C_L, hence $C_O \approx C_L$. If we choose $C_C=1$ pF, we find $W_P \geq 16586{,}9$ µm. In conventional LDO design, the minimum value of W_P is given by Eq. (27) [10], where $I_{L,max}$ is the maximum output current supplied by an LDO regulator to the load, V_{DO} is the maximum dropout voltage and K_p' represents a process transconductance parameter of PMOS transistor which is equal in technology used to 96.6 µA/V^2. For our design specifications, $V_{DO,max}=150$ mV and $I_{L,max}=150$ mA. If the M_P gate length L_P is set to its minimum value of 0.18-µm, $W_{P,min}=12422{,}36$ µm. We observe that the minimum value of W_P given by Eq. (26) in proposed design, is greater than that given by Eq. (27) in conventional design. Thus, there is a compromise between the layout area occupied by M_P and the stability of the proposed LDO regulator system.

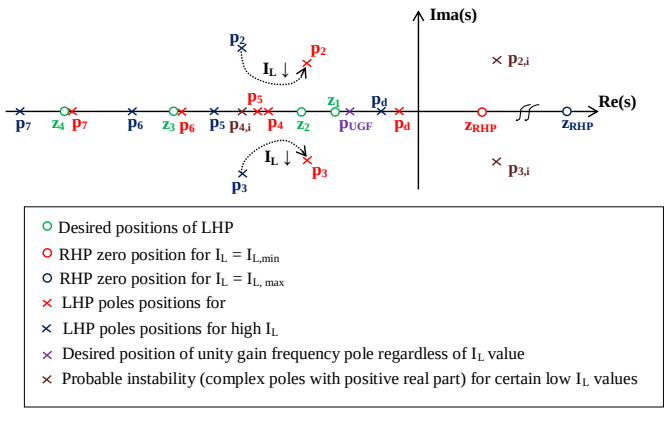


Figure 8. Pole-zero location in complex s plane for the proposed compensated LDO regulator

$$\left(\frac{W_P}{L_P}\right)_{min} = \frac{I_{L,max}}{K_p' V_{DO}^2} \quad (27)$$

To show the robustness of the proposed compensation circuit, we evaluated the phase margin PM for all required values of the load current. The phase margin of the proposed LDO system is given by:

$$PM \approx 90° - \tan^{-1}(\frac{\omega_{UGF}}{\omega_{z_{RHP}}}) + \tan^{-1}(\frac{\omega_{UGF}}{\omega_{z_1}}) + \tan^{-1}(\frac{\omega_{UGF}}{\omega_{z_2}}) - \tan^{-1}(\frac{\omega_{UGF}}{\omega_{pd}}) - \tan^{-1} Q(\frac{\omega_{UGF}}{\omega_0} - \frac{\omega_0}{\omega_{UGF}}) - \tan^{-1}(\frac{\omega_{UGF}}{\omega_{p4}}) - \tan^{-1}(\frac{\omega_{UGF}}{\omega_{p5}}) \quad (28)$$

To have a sufficient phase margin, it is necessary to place the zero z_1 in the vicinity of the unity gain angular frequency ω_{UGF} and before the resonance angular frequency ω_0 of the two conjugate complex poles, the second zero z_2 is placed in the vicinity of ω_0. If, for example, we choose f_{UGF}=1 MHz and f_{z1}= 1.5f_{UGF}, from Eq. (15), we will have f_{z2}= 6.f_{UGF} and therefore $f_0 \approx f_{z2} \approx 6$ MHz. In this case, and according to Eq. (28), in the worst case where the positive real zero is displaced in the vicinity of the unity gain frequency, the phase margin obtained is equal to 80°. Therefore, the proposed compensation circuit ensures the stability of the LDO regulator for all required values of the load current which represents the desired result.

Finally, the stability condition on the phase margin PM for the proposed LDO regulator system, given by Eq. (29), allows determining the values of R_C and C_C for the desired value of unity gain frequency f_{UGF}.

$$PM \approx 90° + \tan^{-1}(2\pi f_{UGF} R_C C_C) + \tan^{-1}(\frac{\pi f_{UGF} R_C C_C}{2}) \quad (29)$$

3.3 Transient response analysis

Transient response is the dynamic performance of linear regulator [10]. It can be separated into two parts, one is form load variation, named as load transient response, and the other is from line variation, named as line transient response. A typical LDO regulator transient response to load changes is shown in Figure 9.

For an increase of load current by ΔI_L, the LDO output observes an undershoot ΔV_O, for a response time duration of Δt_1. The loop reacts to this load change and the output voltage settles in a time duration defined by reaction time also known settling time Δt_2. Minimizing $\Delta t_1 + \Delta t_2$ is a critical need for digital load applications. The LDO response time Δt_1 depends on undershoot ΔV_O, output capacitance C_O and load current change ΔI_L, and can be expressed as:

$$\Delta t_1 = C_O . \frac{\Delta V_O}{\Delta I_L} \quad (30)$$

The settling time, Δt_2 is determined by the open-loop bandwidth ω_{pd} of the regulation loop and the slew-rate (SR) at the gate of pass transistor MP and can be written as:

$$\Delta t_2 = \frac{2\pi}{\omega_{pd}} + SR \quad (31)$$

with,

$$SR = C_{G,P} . \frac{\Delta V_{G,P}}{I_{SR}} \quad (32)$$

where, $\Delta V_{G,P}$ and I_{SR} represent the voltage change and slewing current at the gate of M_P, and we have $\Delta V_{G,P}$ is proportional to ΔV_O.

The proposed compensation circuit also improves the transient response by increasing the bias current at the gate of the pass transistor M_P via the current amplifier block which amplifies this bias current $I_{B,C}$ during the transient times of the load current, which allows to minimize the slew-rate and consequently to reduce overshoots and undershoots and also to reduce the settling time.

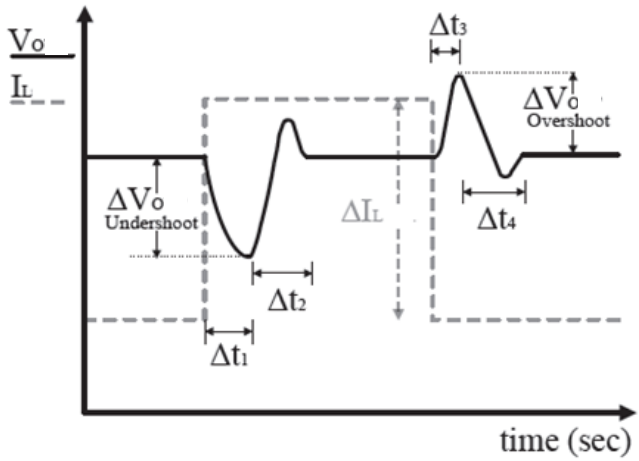


Figure 9. Typical LDO Regulator Load Transient Response

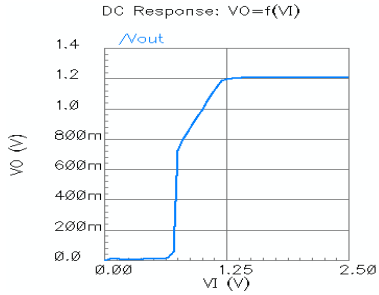
3.4 Voltage reference

The LDO regulator proposed in this work also includes the voltage reference, which plays an important role in the accuracy of the feedback voltage V_{FB}, which is why this voltage reference V_{REF} must have a precise value and independent of the temperature, the supply voltage and the process of the technology used. The voltage reference designed for the LDO regulator was previously realized and published by the same authors [32]. The value of V_{REF} is equal to 0.635 V.

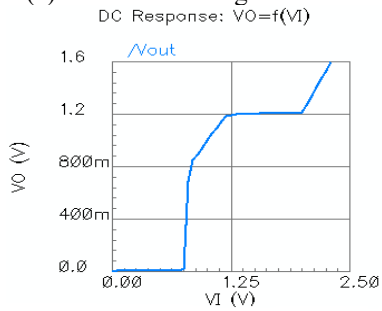
4. SIMULATION RESULTS AND DISCUSSION

The proposed three stage LDO regulator with dual frequency compensation scheme was simulated in standard 0.18 µm CMOS process using Cadence Virtuoso Spectre Simulator.

As shown in Figure 10 in the DC line simulation at maximum load current of 150 mA, the proposed LDO provides a DC output voltage V_O of 1.2 V from a minimum input supply voltage V_I of 1.35 V. The DC line regulation is 4.68mV/V for input supply voltage variation ΔV_I of 0.5 V from 1.35 V to 1.85 V, this operating voltage range is limited by the line regulation of the designed voltage reference [32] as shown in Figure 10 (b).

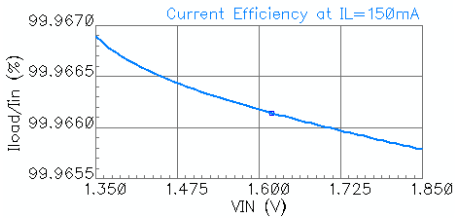


(a) With ideal voltage reference

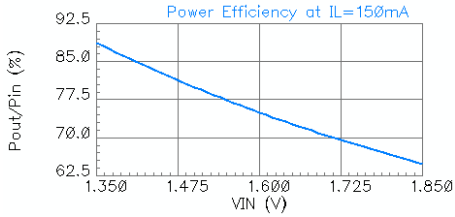


(b) With internal voltage reference

Figure 10. Simulation result of the DC line regulation at maximum load current



(a) Current efficiency

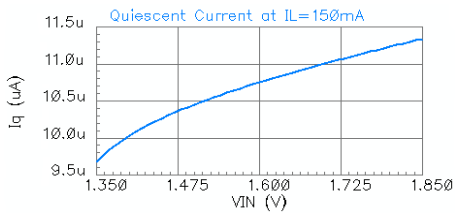


(b) Power efficiency

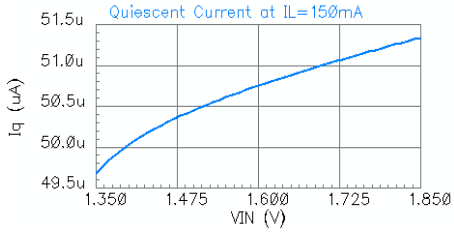
Figure 11. Simulation result of efficiency at maximum load current

As shown in Figure 11 in the DC efficiency simulation, for V_I=1.6, the current efficiency is equal to 99.9662 % while the power efficiency is 75 % at maximum load current of 150 mA, respectively.

Figure 12 gives the simulation result of the quiescent current. The quiescent current consumed by the proposed LDO regulator in full load condition and under the supply input voltage of 1.6 V is 10.75 µA without voltage reference, while this current is 50.75 µA with the internal voltage reference.

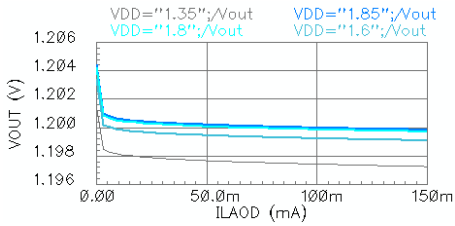


(a) With ideal voltage reference

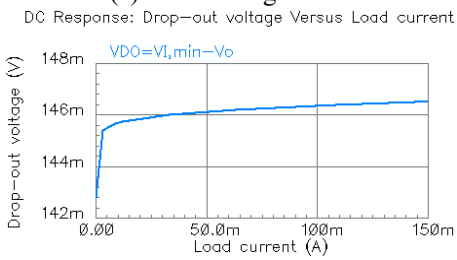


(b) With Internal voltage reference

Figure 12. Simulation result of quiescent current



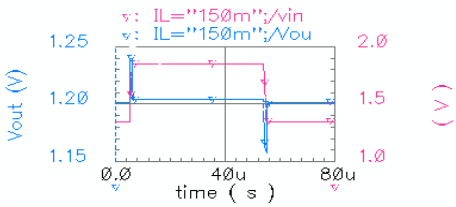
(a) DC load regulation



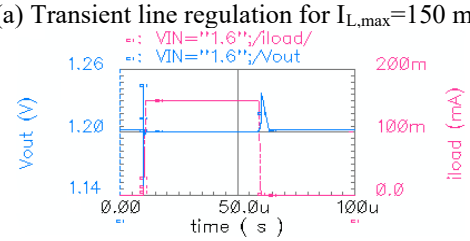
(b) Drop-out voltage

Figure 13. DC load simulation result

As shown in Figure 13 in the DC load simulation, the DC load regulation is equal to 24.2 µV/mA at V_I=1.6 V measured from Figure 13 (a). The proposed LDO regulator has a low value of the drop-out voltage less than 150mV for all required load current range as shown in Figure 13 (b).



(a) Transient line regulation for $I_{L,max}$=150 mA



(b) Transient load regulation for V_I=1.6 V

Figure 14. Transient simulation

Figure 14 presents the transient simulation of the proposed compensated LDO regulator. As shown in Figure 14 (a), for transient line regulation performed at maximum load current $I_{L,max}$ of 150mA, the output voltage V_O presents an overshoot of 19.77 mV when the input supply voltage V_I pulse up from 1.35 V to 1.85 V during 1 µs of rise time, while V_O presents an undershoot of −17.15 mV when V_I pulse down from 1.85 V to 1.35 V during 1 µs of fall time. As shown in Figure 14

(b), for transient load regulation performed at input supply voltage V_I of 1.6 V, V_O presents an overshoot of 44.9 mV and an undershoot of −50.8 mV when load current pulse up from 0mA up to 150mA during 1 µs of rise time, while V_O presents an overshoot of 34.1 mV when load current pulse down from 150mA down to 0mA during 1 µs of fall time.

Figure 15 shows the open loop AC simulation for all required load current range at input supply voltage of 1.6V under C_L=100pF, R_C=100kΩ and C_C=1pF. The proposed LDO is stable for all required current load range. The minimum value of load current I_L for normal operation is 50 µA. The unity gain frequency is practically constant for any value of I_L in the required range and it is close to 1 MHz, which presents a good performance of the proposed compensation circuit. The AC magnitude exhibits a high frequency peak, its location depends on the value of the load current and this due to the presence of two complex conjugate poles as it has been proved in section 3. Table 1 summarizes the AC simulation performance for the proposed LDO regulator at input supply voltage V_I of 1.6 V.

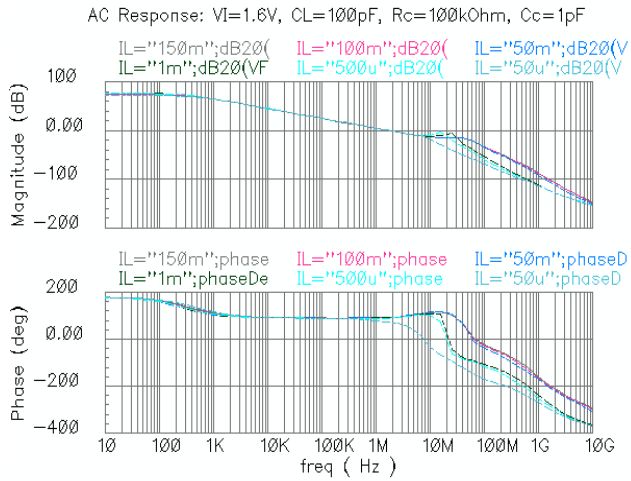


Figure 15. AC open loop simulation for all required load current range

To show the robustness of the proposed dual compensation technique in term of stability with respect to the load current, a comparison with classical compensation methods and others compensation methods cited in this work such as [18] and [21] is performed as shown in Figure 16. The proposed compensation technique ensures stability not only for low values of the load current but also for very low values of the load current, in particular for a zero load current where the phase margin is equal to 45.1° as it is shown in Figure 16 (b). This result is not achieved by the compensation methods proposed in [18, 21]. In addition, the proposed compensation circuit uses a total compensation capacitance $C_{C,tot}$ of 2 pF, while the authors of [18, 21] have used 23 pF and 41 pF respectively to guarantee good stability. The smaller the capacitor to integrate on the chip, the more the layout area is saved.

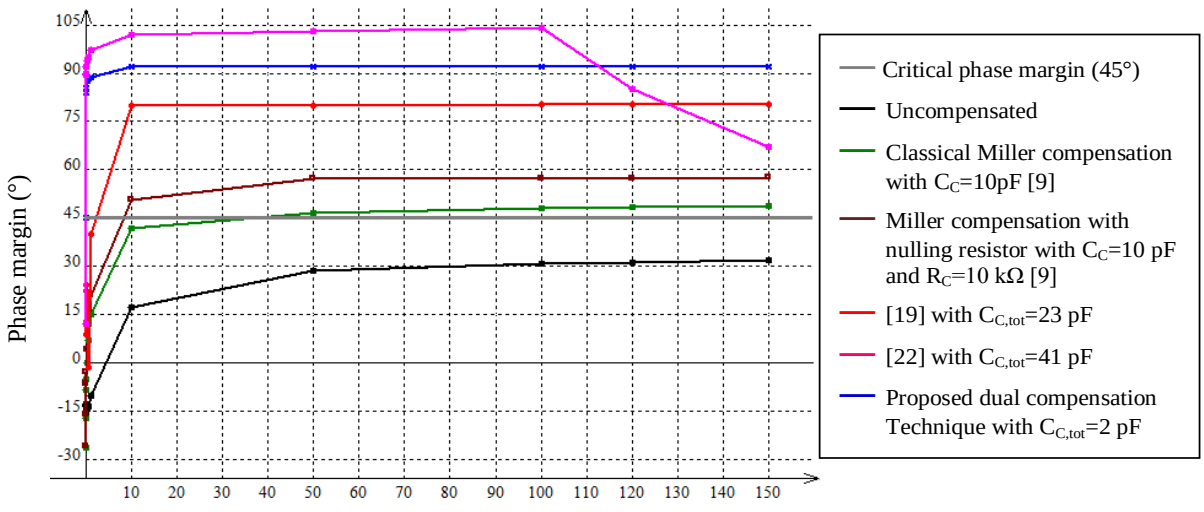
Table 1. AC simulation performance of the proposed LDO regulator at V_I =1.6V

Performance	Mimum load	Full load
DC gain $\|H_{0,c}\|$	72.53 dB	74.05 dB
Bandwidth f_{pd} [1]	268.3 Hz	220.3 Hz
Gain-bandwidth product $\|H_{0,c}\|.f_{pd}$	1.135 MHz	1.110 MHz
Unity gain frequency f_{UGF}	1.139 MHz	1.113 MHz
Phase margin PM [2]	84.06°	92.08°
Resonant frequency f_r [3]	6.309 MHz	39.81 MHz

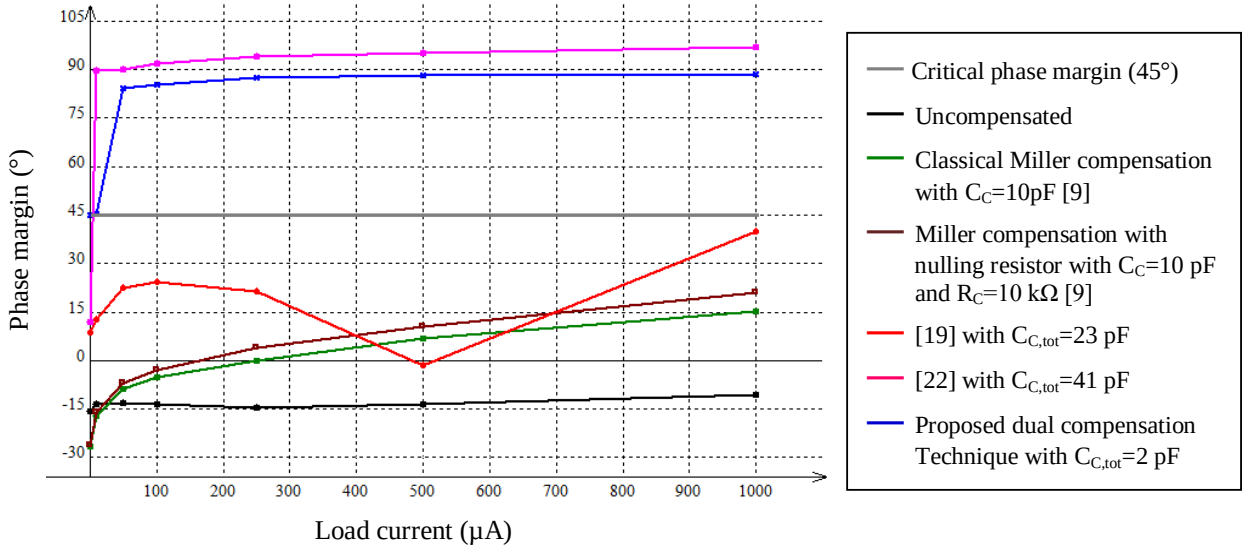
[1] $f_{pd}=2\pi\omega_{pd}$. [2] $PM=180°+Arg[H_{ol,c}(j2\pi f_{UGF})]$. [3] $f_r = f_{pd}=2\pi\omega_r$

Table 2 summarizes performance characteristics of the proposed LDO regulator and comparison with others LDO regulators cited in this work is given. For comparison of the State of the Art, some Figures of Merit (FOMs) is proposed [33]. Note that the smaller the FOM chosen for this work, the better the regulator. The FOM chosen for the comparison is given by Eq. (33), where $|\Delta V_{O,max}|$ is the maximum variation of the output voltage V_O in the line voltage or the load current (maximum overshoot or absolute value of minimum undershoot), I_Q is the quiescent current, C_L is the load capacitance and $I_{L,max}$ is the maximum load current.

$$FOM = \left|\Delta V_{O,\max}\right| \cdot \frac{C_L . I_Q}{I_{L,\max}^2} \tag{33}$$



(a) all load current range



(b) low load current range

Figure 16. Phase margin versus load current for LDO regulator system

Table 2. Performance of proposed LDO regulator and comparison with other LDO regulators cited in this work

Performance	[17]	[25]	[26]	[27]	[18]	[22]	This work
Process (µm)	0.35	0.18	0.35	0.5	0.065	0.18	0.18
Input supply voltage V_I (V)	3.0-4.0	1.1-1.5	1.2-1.5	1.4-4.2	1.2	1.1-1.5	1.35-1.85
Output voltage V_O (V)	2.8	1.0	1.0	1.21	1.0	1.0	1.2
Drop-Out voltage V_{DO} @ $I_{L,max}$ (mV)	200	100	200	200	200	114	146.6
Maximum load current $I_{L,max}$ (mA)	50	50	50	100	100	100	150
Quiescent current I_Q @ $I_{L,max}$ (µA)	65	54	45	45	82.4	20	[5]9.68-11.3 [6]49.68-51.3
Current efficiency η_I @ $I_{L,max}$ (%)	99.935	99.946	99.955	99.955	99.917	[1]N. A.	99.968-99.967
Power efficiency η @ $I_{L,max}$ (%)	[1]N. A.	[1]N. A.	[1]N. A.	[1]N. A.	[1]N. A.	[1]N. A.	88.8-65.5
Minimum on-chip output capacitance C_L (pF)	10^2	10^2	10^3 (Off-chip)	10^5 (Off-chip)	10^2	10^2	10^2
Total compensation capacitance $C_{C,tot}$ (pF)	23	5	41			12	2
Transient Line Regulation (ΔV_O varying V_I)							
Maximum overshoot (mV)	90	[1]N. A.	[1]N. A.	23	8.91	55.66	23.05
Minimum undershoot (mV)	−10	[1]N. A.	[1]N. A.	−12	−10.63	−55.34	−22.49
Transient Load Regulation (ΔV_O varying I_L)							
Maximum overshoot (mV)	80	100	70	47	0	99.52	31.1
Minimum undershoot (mV)	−80	−80	-70	−48	−68.8	-591.1	−54.5
[2] Response time (µs)	15	2	4	5	6	6.3	[3]1,697 [4]1,994
Internal Votlage Reference	No	No	No	No	No	No	Yes
DC Line Regulation @ $I_{L,max}$ (mV/V)	[1]N. A.	[1]N. A.	0.327	[1]N. A.	4.7	[1]N. A.	4.68
DC Load Regulation (µV/mA)	[1]N. A.	[1]N. A.	250	408	300	1	24.7-24.9
FOM (fs)	416	388.8	2520	42750	56.69	118.2	2.345[7]12.03

[1]Not available, [2]Value obtained in load transient regulation, [3]Simulated value obtained at V_I=1.6 V for I_L step-up variation from 150 mA to 0 mA with 1 µs of rise time, [4]Simulated value obtained at V_I=1.6 V for I_L step-down variation from 0 mA to 150 mA with 1 µs of fall time, [5] Values obtained with ideal voltage reference, [6] Values obtained with internal voltage reference, [7] Value obtained with internal voltage reference and calculated by using Eq. (32)

It is difficult to compare LDO regulators because generally each one is intended for a specific application. There are always tradeoffs between different performances such as high stability, fast transient response, low quiescent current which increases battery life and high power supply ripple rejection ratio which is not addressed in the proposed work. To determine the good LDO regulator from the performances inserted in Table 2, we base on the calculated value of the figure of merit FOM which includes the consumption from quiescent current, the capability of the LDO regulator to provide maximum current, the capacitance used to the output which must be as small as possible to save the surface and finally the maximum peak of the output voltage which must be minimized to avoid an abnormal operation of the circuit supplied by the LDO regulator. The proposed LDO regulator is better compared with the LDO regulators cited in the Table 2, because it has the smallest value of FOM which is equal to 2.345 fs with ideal voltage reference, while FOM is equal to 12.03 fs with internal voltage reference.

5. CONCLUSION

In this paper, a novel internally frequency compensation technique called dual frequency compensation is proposed to enhance stability and transient response of the on-chip output capacitor three stage low-dropout linear voltage regulator. The proposed compensation technique guarantees the stability of

the regulator system in a wide range of load current from 0 to 150 mA with small value of compensation capacitance of 2 pF and maximum value of 100 pF of load capacitance. The maximum quiescent current at full load condition of 150 mA is only 51.29 μA when LDO regulator operates with 1.8 V of input supply voltage. Based on the calculated value of the FOM, the proposed LDO regulator exhibits good performance in terms of transient response compared to LDO regulators cited in this paper. The proposed circuit can be used to power a low voltage system on a chip of a smart wearable device. The proposed compensation method in this work degrades the power supply ripple rejection of the LDO regulator due to the decrease in the value of the $R_{G,P}$ resistance. This problem has not been studied in this paper and will be addressed in future work.

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