IIETA International Information and Engineering Technology Association
Advancing the World of Information and Engineering

European Journal of Electrical Engineering
Vol. 23, No. 2, April, 2021, pp. 103-111
Journal homepage: http://iieta.org/journals/ejee

Design of New Duty-Cycle Modulator Structures for Industrials Applications, an Alternative to Pulse-Width Modulation

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https://doi.org/10.18280/ejee.230203

Received: 9 September 2020
Accepted: 14 March 2021

Keywords:
duty-cycle modulation, pulse width modulation, industrials applications

ABSTRACT

In this paper, two new duty-cycle modulator structures are proposed, as a good alternative to existing modulation techniques: the symmetrical linear duty-cycle modulator, and the general linear duty-cycle modulator. The proposed structures consist of two stages with operational amplifiers and theirs period and duty cycle depend on the control voltage. The first stage is a Schmitt trigger comparator which generates the modulated rectangular signal. The other, by integrating the difference between modulated and reference signals, generates a triangular signal is which is sent back to the input of the comparator. To evaluate the performance of the proposed structures, a detailed study of sinusoidal pulse width modulator, non-inverting duty-cycle modulator and they were made. The simulation results computed in MATLAB/Simulink software show that proposed modulator scan operate in low frequency range, maintaining a constant current ripple and an acceptable total harmonic distortion. Their duty-cycles are independent of the values of the passive components used. The experimental tests carried out on symmetrical linear duty-cycle modulator under various reference voltage confirms the robustness of the structure in relation to the values of the components.

1. INTRODUCTION

Modulation is an operation that consists of transposing asignal representing one information into another, without significantly modifying the information it carries. It transforms a modulating or primary signal into a modulated signal. A convention links the characteristics of the modulating signal to those of the modulated signal. Modulation theory has a major research area in signal transmission, signal processing, Analog-to-Digital Conversion (ADC), Digital-to-Analog Conversion (DAC) and control of power electronic converters and continues to attract considerable attention and interest [1]. The switching modulation which includes Sigma-Delta Modulation (SDM) Pulse Width Modulation (PWM) and Duty-Cycle Modulation (DCM) is a type of modulation widely used for industrial applications.

The pioneering complete SDM architecture was invented in 1962 by Janssen and Roermund [2]. The operation of SDM relies on the combination of two signal processing techniques, namely, oversampling and quantization error filtering and feedback, commonly referred as noise shaping [3]. Initially limited to the encoding of low-frequency audio signals and first- or second-order loop filtering, improved architectures and relevant applications of SDM technology have been increasingly developed by many authors, e.g., Goodman in 1969 [4], Jayant in 1976 [5], Hauser in 1991 [6], and Shreier et al. in 2017 [7]. However, the most modern application of SDM technology remain limited to ADC systems [8].

PWM is a modulation technique in which the frequency can be either constant or variable [9]. In constant frequency PWM method, the frequency is constant and the ON time changes according to the modulating signal. It can be produced by comparing a reference signal with a carrier signal [9]. In variable frequency PWM method, the frequency is variable and ON time or OFF time is constant. There are several different PWM techniques, differing in their methods of implementation. The basics PWM topologies including single PWM produced by comparing rectangular reference wave with triangular carrier wave, the multiple PWM and the Sinusoidal PWM (SPWM)using sinusoidal reference wave and triangular carrier wave [10]. There are several advanced PWM topologies depending on the carrier used such as Alternative Phase Opposite Disposition PWM (APOD-PWM), Harmonic-Injection PWM (HI-PWM), Carrier Based Space Vector PWM (CB-SVPWM) and stepped modulation [10, 11]. Although PWM is still widely used in industrial applications [12, 13], it still has some limitations. When PWM is used to control solid state switches, a relatively high frequency carrier is required to reduce current and voltage ripple and THD [14]. This increase in frequency leads to switching losses [15-17] on the one hand, and to thermal stress at the switches on the other hand [14, 18]. Today there are solutions to overcome this undesirable effect, such as the use of newer "big gap" switches, which have lower switching losses than silicon Insulated Gate Bipolar Transistor (IGBT) switches, but at a high cost [14]. Another solution would be to reduce the switching frequency without increasing ripple.

The DCM is a modulation in which an input signal x is transformed into a train of switching wave where duty cycle and period of the modulated signal vary simultaneously according to control signal [8, 19]. Initially invented and patented by Biard in 1962, the realization of classical DCM circuit requires at least two integrated circuits and seven passive elements [20]. A new simplest and higher quality DMC have subsequently been proposed by Mbihi et al. [21]. Initially proposed for instrumentation problems, they are today used in many sectors such as ADC [22, 23], DAC [24], control of electronic power converter [25, 26], digital signal transmission [19], power quality [27] and optical transmission [28]. This structure, although functional and allowing low-frequency operation, has some drawbacks, among which: The non-linearity of the function linking the duty-cycle to the control signal and the dependence of the duty-cycle on the values of the passive components.

In this article, we propose two new duty-cycle modulator structures namely Symmetrical Linear DCM (SLDCM) and General Linear DCM (GLDCM). These structures combining the advantages of PWM and DCM structures, are based on an association between an integrator circuit and a hysteresis comparator.

The remaining part of this paper is organized as follows: A brief description of SPWM and Non-Inverter DCM (NIDCM) is given in section 2. Section 3 is devoted to description and analysis of proposed DCM schemes. Section 4 present the simulation results and experimental validation and finally, section 5 concludes the paper.

2. SPWM AND NIDCM TECHNIQUES

Among the PWM techniques, the SPWM technique is one the most widely used. Nevertheless, in the last decade, the NIDCM gives many good results in several applications. This section describes in detail the SPWM and of NIDCM techniques in terms of relationship between period, duty cycle, reference voltage and all components of the structure.

2.1 Sinusoidal pulse width modulation technique

The scheme of a PWM signal generator is shown in Figure 1. It consists toa triangular signal generator which produces a carrier and an inverting comparator whose output switches as a function of the difference between the carrier and the control signal V_{ref}, where R_1, R_2 and R are resistors and Ca capacitor. The saturation voltages of the amplifiers are $+V_{sat}$ and $-V_{sat}$ while $+V_{CC}$ and $-V_{CC}$ are their supply voltages; V_s is the output of the modulator.

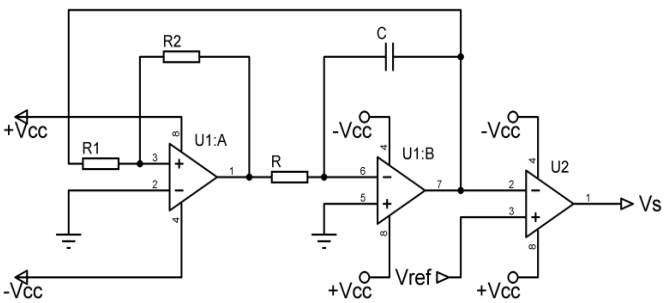


Figure 1. Conventional pulse-width modulator

The period T and duty cycle a (with inverting comparator) of a PWM modulated signal are given by:

$$T = 4RC\frac{R_1}{R_2} \tag{1}$$

$$\alpha = \frac{1}{2}\left(1+\frac{V_{ref}}{V_{sat}}\frac{R_2}{R_1}\right) \tag{2}$$

For V_{ref} =0V, we have $\alpha = \frac{1}{2}$.

The duty-cycle being between 0 and 1, we have:

$$\begin{cases} \alpha = 0 \Rightarrow V_{ref} = -\dfrac{R_1}{R_2}V_{sat} \\ \alpha = 1 \Rightarrow V_{ref} = +\dfrac{R_1}{R_2}V_{sat} \end{cases} \tag{3}$$

so,

$$-\frac{R_1}{R_2}V_{sat} \le V_{ref} \le +\frac{R_1}{R_2}V_{sat} \tag{4}$$

The ratio of the resistors R1 and R2 reduces the resolution of the reference voltage and consequently the resolution of the duty cycle.

2.2 Non-inverter duty-cycle modulation technique

The scheme of the duty-cycle modulator developed by Mbihi et al is shown in Figure 2.

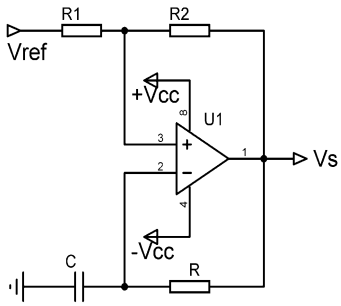


Figure 2. Non-inverter duty-cycle modulator

This modulator has the advantage of being simpler than a PWM modulator. Its period T and duty cycle a are defined by [21]:

$$T = RC\ln\left(\frac{\left(\alpha_2 V_{ref}\right)^2 - \left((\alpha_1+1)V_{sat}\right)^2}{\left(\alpha_2 V_{ref}\right)^2 - \left((\alpha_1-1)V_{sat}\right)^2}\right) \tag{5}$$

$$\alpha = \frac{\ln\left(\dfrac{\alpha_2 V_{ref} - (\alpha_1+1)V_{sat}}{\alpha_2 V_{ref} - (\alpha_1-1)V_{sat}}\right)}{\ln\left(\dfrac{\left(\alpha_2 V_{ref}\right)^2 - \left((\alpha_1+1)V_{sat}\right)^2}{\left(\alpha_2 V_{ref}\right)^2 - \left((\alpha_1-1)V_{sat}\right)^2}\right)} \tag{6}$$

With,

$$\begin{cases} \alpha_1 = \dfrac{R_1}{R_1 + R_2} \\ \alpha_2 = \dfrac{R_2}{R_1 + R_2} \end{cases} \tag{7}$$

There is considerable non-linearity in the expressions of the period and the duty cycle. By linearizing the duty cycle ratio around 0 (V_{ref}=0 and $\alpha = \frac{1}{2}$) we have:

$$\alpha = \frac{1}{2}\left(1 + \frac{V_{ref}}{V_{sat}} \frac{\dfrac{2\alpha_1}{(1+\alpha_1)}}{\ln\left(\dfrac{1+\alpha_1}{1-\alpha_1}\right)}\right) \tag{8}$$

The linearized expression of the duty cycle is only valid for a range of the control voltage V_{ref}[23], which will reduce the resolution of the reference voltage and consequently the resolution of the duty cycle.

The minimum and central period and duty cycle (for V_{ref} =0V) of the Linearized NIDCM (LNIDCM)are given by:

$$\begin{cases} T_0 = 2RC\ln\left(1 + 2\dfrac{R_1}{R_2}\right) \\ \alpha = \dfrac{1}{2} \end{cases} \tag{9}$$

3. DESCRIPTION AND ANALYSIS OF THE PROPOSED STRUCTURES

This section presents the different development leading to the relationships between period, duty cycle, components values and reference voltage for SLDCM and GLDCM.

3.1 Symmetrical Linear Duty-Cycle Modulation (SLDCM)

The SLCDM scheme is shown in Figure 3. It is the result of a modification of the signal generator used in SPWM structure. The hysteresis comparator always generates the modulated signal and the integrator generates, by integrating the difference between modulated and reference signals, a triangular signal that is feedback to the input of the comparator.

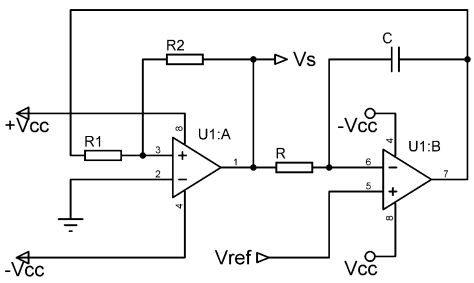


Figure 3. Symmetrical Linear Duty-Cycle Modulation (SLDCM)

This structure is simpler than the conventional pulse width modulator and has only one more component than the non-inverting duty-cycle modulator.

The trigger switching voltages are the solutions of the equation below:

$$v_0 R_2 + V_S R_1 = 0 \tag{10}$$

$$v_0 = -\frac{R_1}{R_2} V_S \tag{11}$$

With v_0 the voltage at the output of the integrator and at the input of the Schmitt trigger.

As $V_S = \pm V_{sat}$, and by calling v_0^+ and v_0^- the switching voltages (respectively positive and negative), we get:

$$\begin{cases} v_0^+ = +\dfrac{R_1}{R_2} V_{sat} \\ v_0^- = -\dfrac{R_1}{R_2} V_{sat} \end{cases} \tag{12}$$

The current in the capacitor C is defined by:

$$i_C = \frac{V_S - V_{ref}}{R} = C\frac{dv_C}{dt} \tag{13}$$

where, v_c is the voltage across the capacitor.

The output voltage v_0 of the integrator is given by:

$$v_0 = V_{ref} - v_C \Leftrightarrow v_C = V_{ref} - v_0 \tag{14}$$

so,

$$\frac{V_S - V_{ref}}{R} = \frac{C}{dt}\left(dV_{ref} - dv_0\right) \tag{15}$$

$$dt = \frac{RC}{V_S - V_{ref}}\left(dV_{ref} - dv_0\right) \tag{16}$$

For a constant value of V_{ref},

$$dV_{ref} = 0 \Rightarrow dt = -\frac{RC}{V_S - V_{ref}} dv_0 \tag{17}$$

Let call t_{ON} and t_{OFF} be the positive and negative pulse width respectively.

During t_{ON}, $V_S = +V_{sat}$ and v_0 goes from v_0^+ to v_0^-; then,

$$t_{ON} = -\frac{RC}{V_{sat} - V_{ref}} \int_{v_0^+}^{v_0^-} dv_0 \tag{18}$$

$$t_{ON} = 2RC\frac{R_1}{R_2}\frac{V_{sat}}{V_{sat} - V_{ref}} \tag{19}$$

During t_{OFF}, $V_S = -V_{sat}$ and v_0 goes from v_0^- to v_0^+; then,

$$t_{OFF} = -\frac{RC}{-V_{sat} - V_{ref}} \int_{v_0^-}^{v_0^+} dv_0 \tag{20}$$

$$t_{OFF} = 2RC \frac{R_1}{R_2} \frac{V_{sat}}{V_{sat} + V_{ref}} \tag{21}$$

The period T of output voltage V_S is given by:

$$T = t_{ON} + t_{OFF} \tag{22}$$

$$T = 4RC \frac{R_1}{R_2} \frac{V_{sat}^2}{V_{sat}^2 - V_{ref}^2} \tag{23}$$

Its duty cycle is equal to:

$$\alpha = \frac{t_{ON}}{T} \tag{24}$$

$$\alpha = \frac{1}{2}\left(1 + \frac{V_{ref}}{V_{sat}}\right) \tag{25}$$

In view to Eq. (25), the duty-cycle ratio of the SLDCM is linear and independent of the values of the passive components. In this configuration, the control voltage can cover the entire range of supply voltages (for $-V_{sat}$ to $+V_{sat}$), so the resolution is maximum.

Its minimum or central period and duty cycle (when V_{ref}=0V) are given by:

$$\left| \begin{array}{l} T_0 = 4RC \dfrac{R_1}{R_2} \\ \alpha = \dfrac{1}{2} \end{array} \right. \tag{26}$$

3.2 General Linear Duty-Cycle Modulation (GLDCM)

By adding a single resistor to the circuit in Figure 3 as shown in Figure 4 below, we can choose to scan the duty cycle for a voltage range defined in [$-V_{sat}$; $+V_{sat}$].

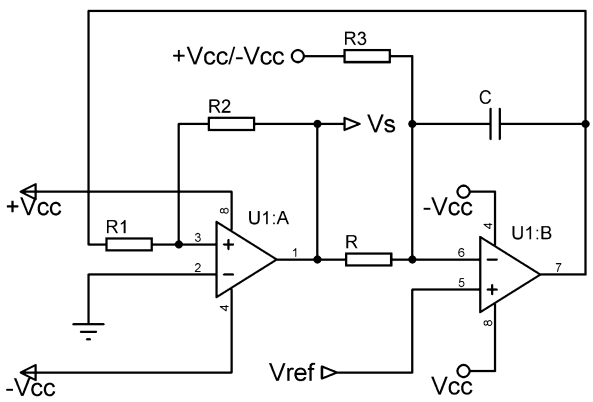


Figure 4. General Linear Duty-Cycle Modulation (GLDCM)

Depending on if we wish to use control voltages in the range $\left[V_{ref\,\min}; +V_{sat}\right]$ or in the range $\left[-V_{sat}; V_{ref\,\max}\right]$, R_3 will be connected to $+V_{sat}$ or $-V_{sat}$ respectively. We have for a constant value of V_{ref}:

$$i_C = \frac{V_S - V_{ref}}{R} + \frac{kV_{sat} - V_{ref}}{R_3} = -C\frac{dv_0}{dt} \tag{27}$$

With k=1 when R_3 is connected to $+V_{sat}$ and k=-1 when R_3 is connected to $-V_{sat}$. Then,

$$dt = -\frac{RR_3C}{R\left(kV_{sat} - V_{ref}\right) + R_3\left(V_S - V_{ref}\right)} dv_0 \tag{28}$$

From the above we have,

$$t_{ON} = 2RC \frac{R_1}{R_2} \frac{R_3 V_{sat}}{\left(R_3 + kR\right)V_{sat} - \left(R_3 + R\right)V_{ref}} \tag{29}$$

$$t_{OFF} = 2RC \frac{R_1}{R_2} \frac{R_3 V_{sat}}{\left(R_3 - kR\right)V_{sat} + \left(R_3 + R\right)V_{ref}} \tag{30}$$

So, the period and duty cycle of general linear duty cycle modulator are:

$$T = 4RC \frac{R_1}{R_2} \frac{R_3^2 V_{sat}^2}{\left(\begin{array}{l} \left(R_3^2 - R^2\right)V_{sat}^2 - \left(R_3 + R\right)^2 V_{ref}^2 \\ +2k\left(R_3 R + R^2\right)V_{sat}V_{ref} \end{array}\right)} \tag{31}$$

And,

$$\alpha = \frac{\left(R_3 - kR\right)V_{sat} + \left(R_3 + R\right)V_{ref}}{2R_3 V_{sat}} \tag{32}$$

This configuration of the linear DCM is more complete than the previous one. Indeed, if we make R_3 tend towards infinity, we find the scheme and equations of the SLDCM modulator.

For $\alpha = \frac{1}{2}$, the minimum or central period T_0 and the corresponding control voltage $V_{ref\,0}$ of GLDCM are given by:

$$\left| \begin{array}{l} T_0 = 4RC \dfrac{R_1}{R_2} \\ V_{ref\,0} = \dfrac{kR}{R + R_3} V_{sat} \end{array} \right. \tag{33}$$

The values $V_{ref\,\min}$ when (k=1) and $V_{ref\,\max}$ when (k=-1) of V_{ref} are obtained for a=0 and a=1 respectively. We have:

$$\left| \begin{array}{l} V_{ref\,\min} = \dfrac{R - R_3}{R + R_3} V_{sat} \\ V_{ref\,\max} = \dfrac{R_3 - R}{R_3 + R} V_{sat} \end{array} \right. \tag{34}$$

In the particular case where R_3=R,

$$\begin{cases} V_{ref\,\min} = V_{ref\,\max} = 0 \\ V_{ref\,0} = \dfrac{k}{2} V_{sat} \\ T = RC \dfrac{R_1}{R_2} \dfrac{V_{sat}^2}{kV_{sat}V_{ref} - V_{ref}^2} \\ T_0 = 4RC \dfrac{R_1}{R_2} \\ \alpha = \dfrac{(1-k)V_{sat} + 2V_{ref}}{2V_{sat}} \end{cases} \quad (35)$$

In this case, we have for k=1:

$$\alpha = \frac{V_{ref}}{V_{sat}} \quad (36)$$

And for k=-1:

$$\alpha = 1 + \frac{V_{ref}}{V_{sat}} \quad (37)$$

4. SIMULATION AND EXPERIMENTAL RESULTS

This section will present the simulations and experimental results based on the equations developed in section 3. Itbegins with a comparison between SPWM, NIDCM and SLDCM. These comparisons were carried out with simulation models in MATLAB/Simulink environment. Next, the experimental tests result of proposed SLDCM structure will be discussed.

4.1 Modulators parameters

Simulations and experimental test were carried out under the specifications found in Table 1 below.

Table 1. Values of the passive components used

Modulators	Passive components			
	R_1	R_2	R	C
SPWM	10kΩ	20kΩ	5.000kΩ	100nF
NIDCM	10kΩ	20kΩ	7.213kΩ	100nF
SLDCM	10kΩ	20kΩ	5.000kΩ	100nF

These values were chosen to have a frequency of 1000 Hz for the SPWM and a maximum (center) frequency of1000 Hz for the NIDCM and SLDCM.

4.2 Simulation results

In Figure 5, the oscillation frequency computed according to Eqns. (1), (5) and (23) is constant for the PWM while it is variable depending to the control voltage for the duty cycle modulators. This variation is fully parabolic for the symmetrical linear DCM and partially parabolic for the non-inverting DCM. Looking at Figure 6 based on Eqns. (2), (6), (8) and (25), it can be seen that the duty cycles of the SPWM and SLDCM vary linearly as a function of the control signal. That of the NIDCM presents a range of linearity in a control range of approximately -9V to +9V, in which its curve is confused with that of its linearized expression LNIDCM; beyond this range, a non-linearity of the duty cycle is observed.

Although the expression of the SPWM duty cycle is linear, it does not cover the whole range of the control signal and is limited between -7.5V and +7.5V unlike the SLDCM which sweeps the whole control range from -15$V$to +15V. As shown in Figure 7, the SLDCM as well as the SPWM and the NIDCM all have close THDs for the same values of the duty cycle. Figure 8 presents the output voltages for different control signal values.

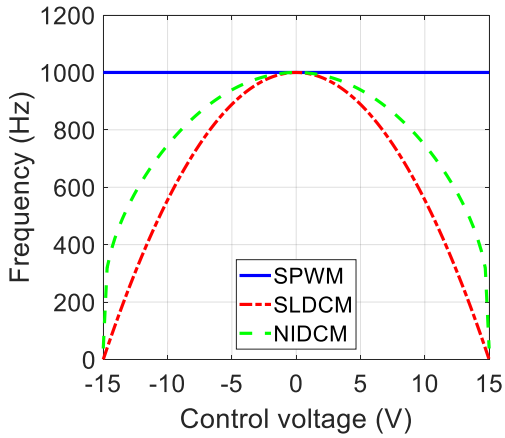


Figure 5. Frequency versus control voltage

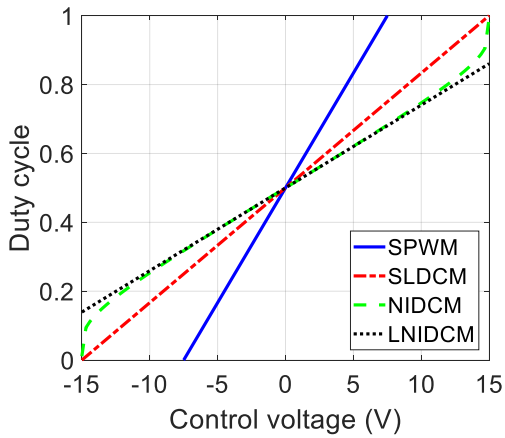


Figure 6. Duty cycle versus control voltage

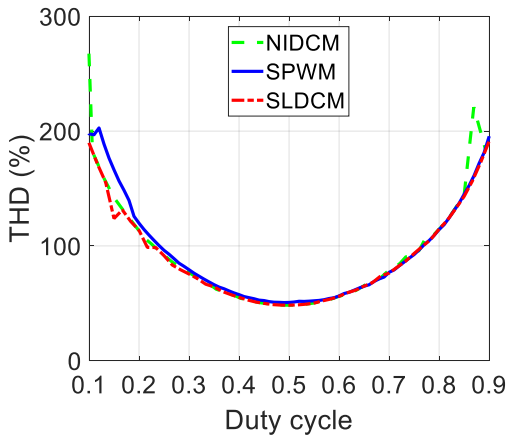
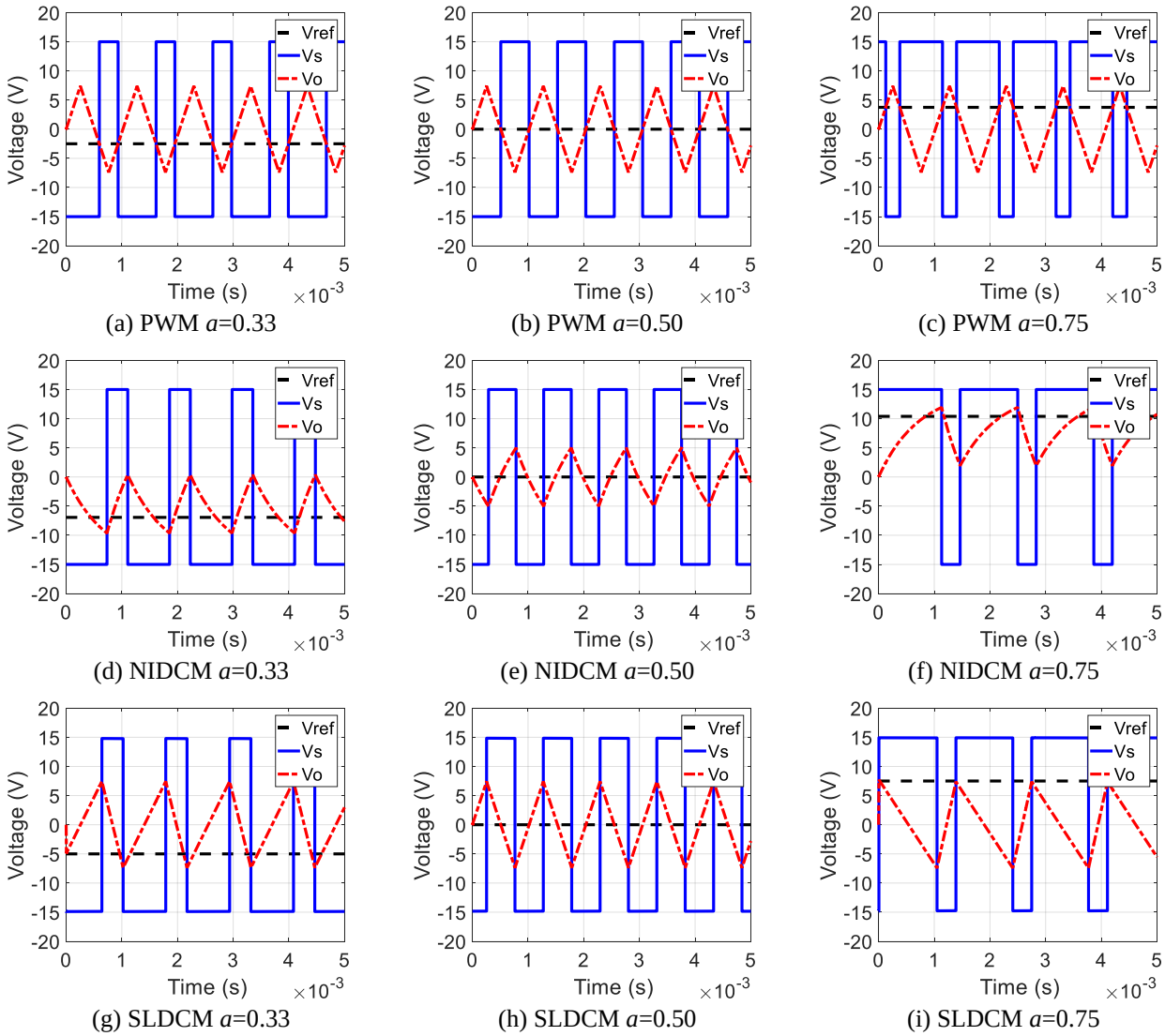


Figure 7. THD versus duty cycle



(a) PWM a=0.33 (b) PWM a=0.50 (c) PWM a=0.75

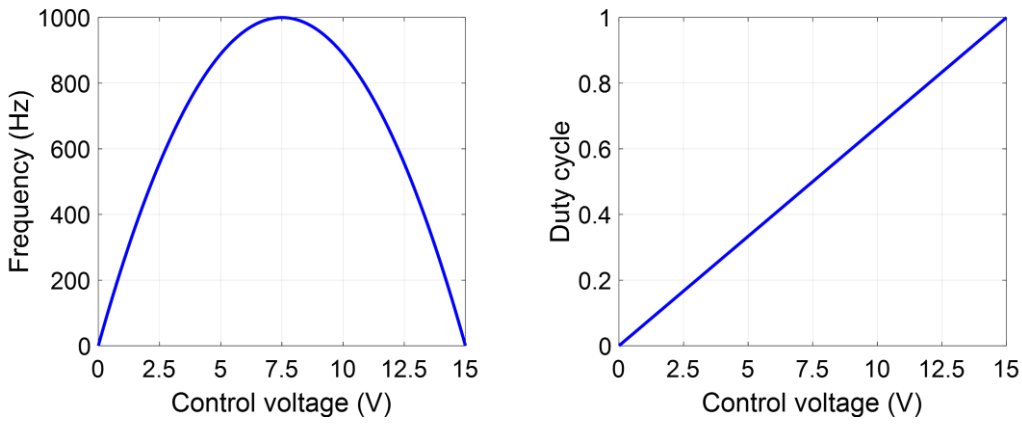
(d) NIDCM a=0.33 (e) NIDCM a=0.50 (f) NIDCM a=0.75

(g) SLDCM a=0.33 (h) SLDCM a=0.50 (i) SLDCM a=0.75

Figure 8. Output voltage of modulators versus duty cycle

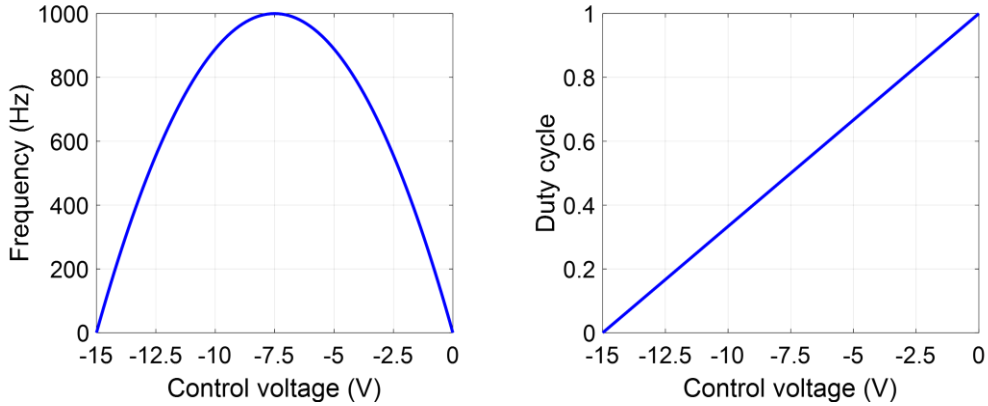
The values 0.35, 0.5 and 0.75 of the duty cycles correspond respectively to voltages of -5V, 0V and 7.5V for the SLDCM. It can be seen from the analysis of graphs that for duty cycles other than 0.5, the period and the associated control voltage are different for each modulator. For a=0.50, we have a frequency of 1000 Hz and a control voltage of 0V.

Figures 9 and 10 based on Eqns. (31) and (32) present the evolution of the frequency and the duty-cycle ratio of the GLDCM versus the control voltage for k=1 and k=-1 respectively, with R_3=R.



(a) Frequency (b) Duty cycle

Figure 9. Frequency and duty cycle of GLDCM versus control voltage for k=1



(a) Frequency (b) Duty cycle

Figure 10. Frequency and duty cycle of GLDCM versus control voltage for k=-1

Simulations of the GLDCM show that in both cases, the duty cycle varies linearly from 0 to 1 depending on the desired control voltage range [$0V$; $15V$] for k=1 and [$-15V$; $0V$] for k=-1. The curves of the frequency versus the control voltage remain parabolic with the (maximum) center frequency obtained for k=1 to V_{ref}=$7.5V$ and for k=-1 to V_{ref}=-$7.5V$.

4.3 Experimental test results

To validate simulations results, experimental tests were performed using an experimental setup as shown in Figure 11.

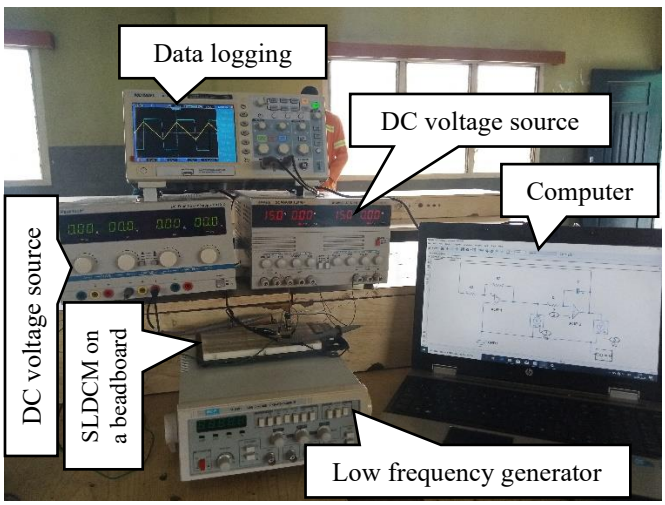


Figure 11. Experimental setup for SLDCM testing

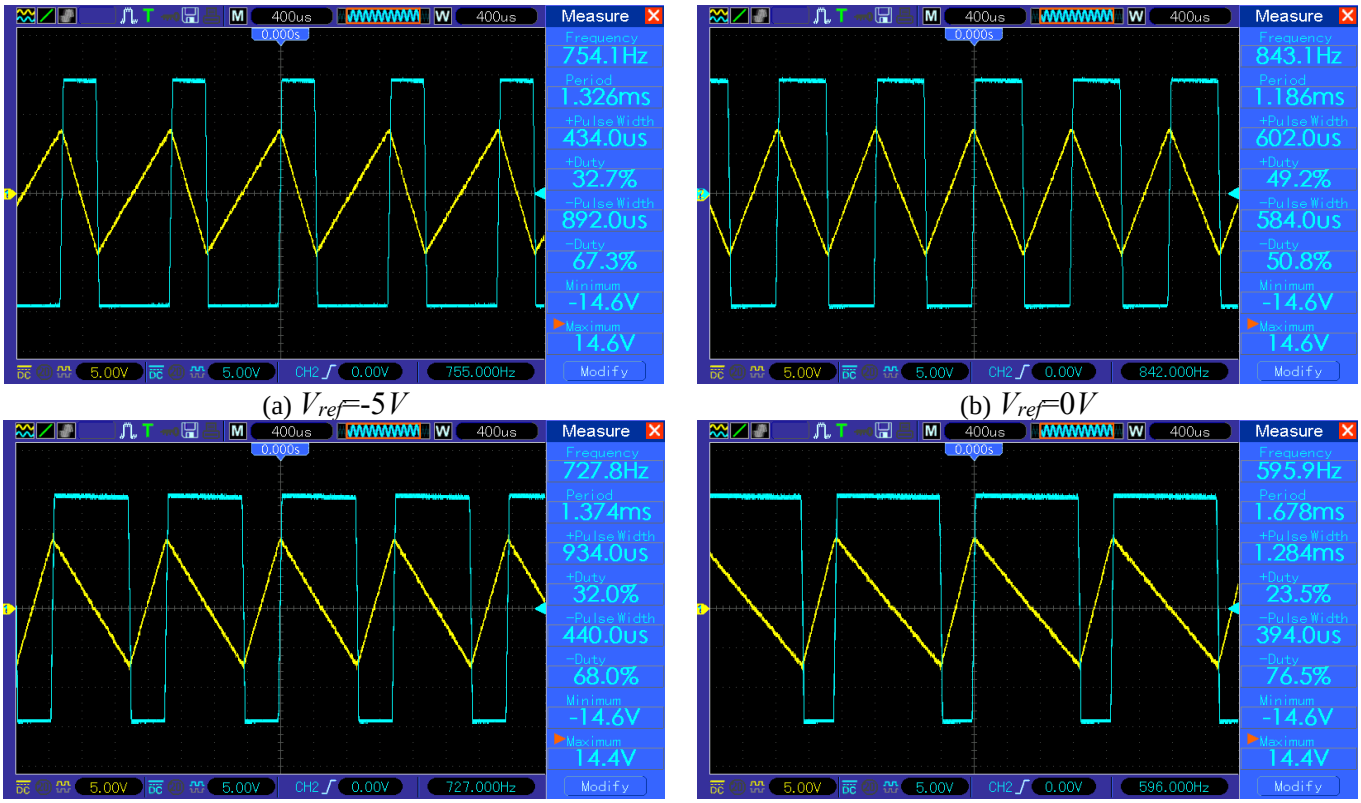
For the experimental test, we chose an operational amplifier of the TL084 family for its high switching speed. The passive components used are the same values as in the simulations. We used two DC voltage sources, one for the polarization of the operational amplifiers and the other for the control signal. A bead board was used to carry out the assembly and a digital oscilloscope was used to visualize the curves.

The tests carried out show the transformation of the constant amplitude control signal into a train of switching wave with a frequency and duty cycle dependent on this amplitude. Figure 12 presents the experimental results obtained and Table 2 shows the values of the theoretical and experimental frequencies and duty cycles obtained for the same control voltages.

Table 2. SLDCM output parameters obtained

Control voltage	Output parameters		
	Values	Frequency (Hz)	duty cycle
-5V	Theoretical	888.9	0.333
	Experimental	754.1	0.327
0V	Theoretical	1000	0.500
	Experimental	843.1	0.508
7.5V	Theoretical	750	0.750
	Experimental	595.9	0.765

For V_{ref}=-$5V$, we experimentally obtain a modulated signal of frequency 754.1Hz with a duty-cycle of 0.327, whereas theoretically we have obtained a modulated signal of frequency 888.9Hz with a duty-cycle of 0.333. For V_{ref}=$0V$, we experimentally obtain a modulated signal of frequency 843.1Hz with a duty-cycle of 0.508, whereas theoretically we have obtained a modulated signal of frequency1000Hz with a duty-cycle of 0.5. For V_{ref}=$5V$, the modulated signal obtained is symmetrical to that obtained in the case of V_{ref}=-$5V$. The two modulated signals have approximately the same frequency and the sum of their duty cycle gives 1. For V_{ref}=$7.5V$, we experimentally obtain a modulated signal of frequency 595.9Hz with a duty-cycle of 0.765, whereas theoretically we have obtained a modulated signal of frequency 750Hz with a duty-cycle of 0.75. The observed differences between the theoretical and experimental values of the frequency of the modulated signal are mainly explained by the fact that the period depends on the values of the passive components. With regard to the duty cycle, the differences between the theoretical and experimental values are much smaller due to the non-dependence of the latter on the values of the passive components. Nevertheless, these minor differences can be explained by the fact that the duty cycle depends on the values of the saturation voltages of the operational amplifier which, experimentally, are +14.6V and -14.6V.



(a) V_{ref}=-5V (b) V_{ref}=0V

(c) V_{ref}=5V (d) V_{ref}=7.5V

Figure 12. SLDCM output voltages for fixed amplitude control voltages

5. CONCLUSION

This work proposes two new duty-cycle modulator structures namely symmetrical linear duty-cycle modulation and general linear duty-cycle modulation. Their principle is based on a double time modulation; both frequency and duty cycle are modulated according to a reference control voltage. These systems have been implemented and observed under different conditions, then compared to the PWM and NIDCM modulators. From the analysis of the results obtained in simulation, several facts can be observed. The variation of the duty cycle is linear while that of the frequency is parabolic. The duty cycle is independent of the values of the passive components used for an analogic modulator, when it is not the case for PWM and NIDCM structures. In addition, it is possible to use a control voltage in [-V_{sat}; +V_{sat}] for the SLDCM and in [-V_{sat}; 0] or [0; +V_{sat}] for the GLDCM, which allows maximum resolution of the control voltage and flexibility in the control setup, as long as it's not for PWM and NIDCM structures. According to the experimental results obtained, we note a good similarity between the theoretical and practical duty cycles for the same control signal values. Future work should study digital SLDCM and GLDCM, and the use of proposed modulator in different applications.

ACKNOWLEDGMENT

The authors would like to express their gratitude to LA SALLE higher technical school for its support during the experimental test.

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NOMENCLATURE

ADC	Analog-to-Digital Conversion
CB-SVPWM	Carrier Based Space Vector Pulse Width Modulation
DCM	Duty Cycle Modulation
GLDCM	General linear Duty Cycle Modulation
LNIDCM	Linearized Non-Inverter Duty Cycle Modulation
NIDCM	Non-Inverter Duty Cycle Modulation
PWM	Pulse Wave Modulation
SDM	Sigma Delta Modulation
SLDCM	Symmetrical linear Duty Cycle Modulation
SPWM	Sinusoidal Pulse Wave Modulation
THD	Total Harmonic Distortion
V_{ref}	Reference or control voltage
V_{sat}	Saturation voltage
V_s	Output voltage
V_o	Integrator output voltage
Vc	Capacitor voltage

Greek symbols

α	Duty cycle