



## Power Loss Analysis in 15 Level Asymmetric Reduced Switch Inverter Using PLECS Thermal Model & SIMULINK Precise Models

Gireesh Kumar Devineni<sup>1,2</sup>, Aman Ganesh<sup>1\*</sup>, Neerudi Bhoopal<sup>2</sup>

<sup>1</sup> School of Electronics & Electrical Engineering, Lovely Professional University, Phagwara, Punjab 144411, India

<sup>2</sup> Department of Electrical & Electronics Engineering, B V Raju Institute of Technology, Narsapur 502313, India

Corresponding Author Email: [aman.23332@lpu.co.in](mailto:aman.23332@lpu.co.in)

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### ABSTRACT

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#### Keywords:

*switching losses, conduction losses, power losses, multilevel inverters, switching frequency*

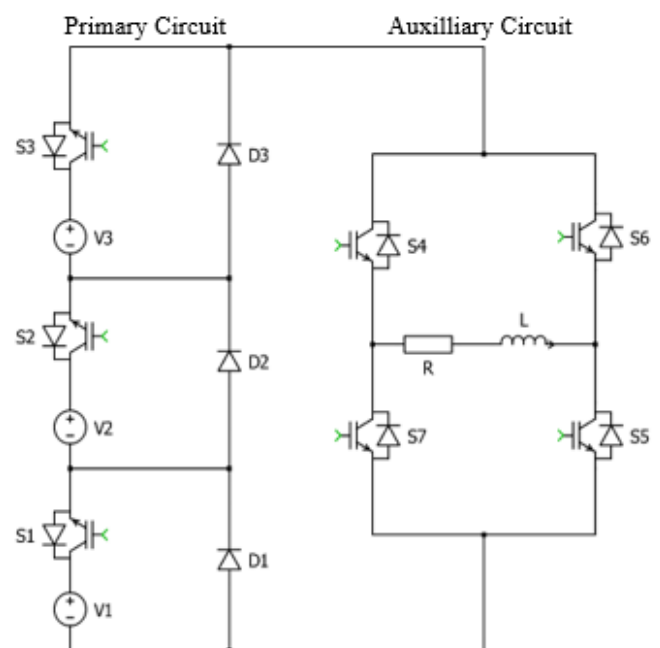
Power losses are the most critical metrics in power converters analysis and has a significant impact on economic and technological assessments due to its sufficient approximation. This article aims to prove that the power losses (Switching & Conduction losses) are very low in low frequency switching modulation in contrast with high switching frequency modulation. Two switching modulation techniques Phase Disposition (PD-multi carrier-based pulse width modulation at high switching frequency) and Selective Harmonic Elimination Pulse Width Modulation (SHEPWM-fundamental switching frequency) are considered for the power loss assessment in 15-level reduced switch asymmetric multilevel inverter. This work proposed a simplified model for calculation of switching losses in multilevel inverters using MATAB SIMULINK. Further, the thermal model of the proposed inverter is implemented on PLECS for analyzing the power losses. The comparative analysis of switching and conduction losses of the proposed inverter with the PLECS thermal model and MATLAB precise models are integral part of this research.

### 1. INTRODUCTION

The use of multilevel inverters has been more important during preceding decades with medium voltage and high-power level. Different power semiconductor switch combinations can help to achieve various multilevel inverter topologies for numerous configurations [1, 2]. In different implementations, various works on literature report effective use of different topologies. However, the reduced switch asymmetric topologies have drawn the most critics, out of three simple setups of NPC, DC and CHB, owing to its remarkable features [3], such as flexible construction, fast control, and function, suited to different modulation techniques. Researchers mainly focused on reducing the number of switches & electronic components in MLI design for reducing the switching losses and conduction losses with minimum number of commutations [4]. These reduced switch topologies use two circuits interconnected namely, level generation circuit and polarity generation circuit [5]. The level generation circuits are energized with isolated DC sources and the polarity generation circuits reverse the sign of voltage and current waveforms of level generation circuits is presented in Figure 1.

Each basic cell of proposed inverter is provided with a separate DC supply, the current on each cell is different from the load or source current on every power semi-conductor switch of a given cell. The action of power semiconductor switches is also crucially studied, and power losses are investigated. Power loss is perhaps the most critical aspect in the power system study and the economic and technological evaluations are measured accordingly [6]. The power losses of a power converter include switching losses, conduction losses, ON and OFF state losses, gate driver losses. Even so, during

off state, the semiconductor switches had negligibly small leakage current, hence off state losses and gate driver losses are neglected in IGBTs. Thus, it is only appropriate to consider switching losses and conduction losses [7]. The analysis power losses on multi-level inverters are quite complex. The control of power quality and the methods of modulation to mitigate power loss is equally significant.



**Figure 1.** An asymmetric 15-level reduced switch inverter topology

Many researchers recommended methods based on the SPWM to reduce harmonics and evaluate the overall power loss in multilevel inverters [8]. But since SPWM has a high switching frequency, there are also high-power losses. It is therefore necessary to optimize the switching frequency for reducing power loss while mitigating THD [9]. Few approaches including optimization of switching angles to provide gating pulse for various multi-level inverter switches are proposed to further minimize power losses (4% of power delivered to the load) to a larger degree as the switching frequency is substantially decreased [10].

This article presented the thermal analysis of IGBTs of proposed inverter for switching and conduction loss calculation using PDPWM and SHEPWM on PLECS software [11]. Further the simplified models are developed for each switch of the proposed inverter on SIMULINK. The suggested simplified models evaluate the switching and conduction losses using curve fitting method from the data sheet of the IGBT using SHEPWM [12-14]. The comparative analysis of power losses obtained from PLECS thermal analysis and SIMULINK simplified models is the intended part of this research.

## 2. SWITCHING CONTROL METHODOLOGY OF PROPOSED INVERTER

Various modulation methods have been used to control the output of the voltage waveform in multi-level inverters. These control techniques are categorized primarily based on the switching frequency into low or high frequency switching techniques. High frequency switching modulations are such as Sine pulse width modulation (SPWM), multi carrier-based modulation schemes like Phase Disposition (PDPWM), Phase opposition & disposition (PODPWM) Alternate phase opposition & disposition (APODPWM) etc., [15] in which the active switch can trigger several times in a cycle. Whereas Space Vector (SVPWM) [16] and Selective Harmonic Elimination (SHEPWM) [17] are low frequency switching techniques in which the active power switch is triggered only one or two times in a single cycle.

In this study, both high & low frequency switching methods are implemented on proposed 15-level inverter. For the better results, the Phase Disposition PWM (PDPWM) from high frequency switching and Selective Harmonic Elimination (SHEPWM) methods was proposed to control the inverter. The SHEPWM strategy had lower switching losses and less EMI due to its low switching frequency. Furthermore, the dominant low order harmonic can be eliminated and thus the required filter size at inverter output can be optimized. In both the switching methods, the power losses are calculated, and comparative analysis is the intended part of this research.

### 2.1 Phase disposition switching method (High frequency switching)

All the carrier signals are in-phase and level shifted in PDPWM switching pulse generation method as shown in Figure 2. The single-phase reference or modulating signal is 'V' and the carrier signals are C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13 and C14. The control signal to be provided to the corresponding phase leg switches is produced by comparison of these fourteen carrier signals with the corresponding modulating signal.

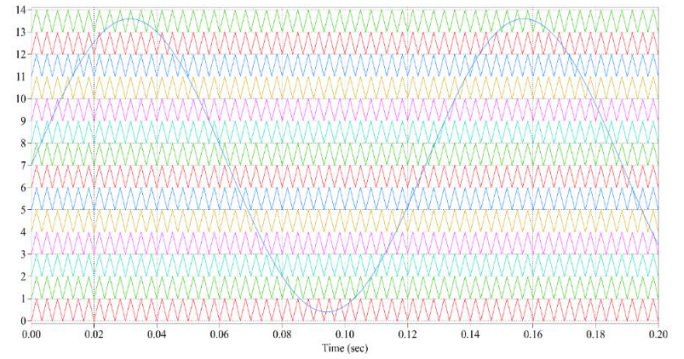


Figure 2. Phase disposition modulation

### 2.2 Selective harmonic elimination switching (Low frequency switching)

To get the desired multilevel fundamental Voltage, SHE uses predefined switching angles and eliminates dominant lower order harmonics that reduce the overall harmonic distortion (THD). The switching angles are pre-calculated off-line and thus this is called an open loop control technique. Figure 3 shows the 15-level MLI voltage waveform. It is obvious that there are 7 switching angles that can be pre-calculated in this scenario.

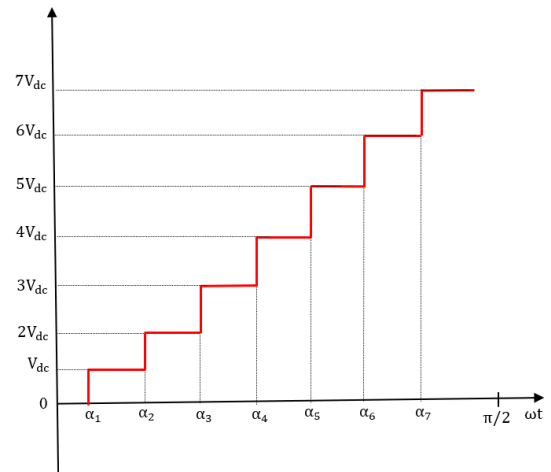


Figure 3. Quarter wave approximation of 15-level output of multilevel inverter

The stepped voltage wave form can be expressed in the sum of periodic sine and cosine signals and a constant by applying Fourier's expansion. The signal is made up of odd and even harmonics. The even harmonics and a dc constant are canceled due to the symmetry of the waveform quarter. Therefore, we consider only odd harmonics. All the triplen harmonics are zero for balanced three-phase systems. The output voltage waveform can usually be written as:

$$v(\omega t) = \frac{4V_{dc}}{\pi} \left\{ (\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \dots) \sin\omega t + (\cos 3\alpha_1 + \cos 3\alpha_2 + 2\cos 3\alpha_3 + \dots) \frac{\sin 3\omega t}{3} + (\cos 5\alpha_1 + 2\cos 5\alpha_2 + 2\cos 5\alpha_3 + \dots) \frac{\sin 5\omega t}{5} + \dots \right\} \quad (1)$$

From Figure 2. it is clear that the switching angles  $\alpha_1$  to  $\alpha_7$  must not exceed the  $\frac{\pi}{2}$ , therefore the switching angles should satisfy the constraint in Eq. (2)

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \quad (2)$$

$$\left. \begin{aligned} \frac{4V_{dc}}{\pi} [\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4 + \cos\alpha_5 + \cos\alpha_6 + \cos\alpha_7] &= f_1(\alpha) = M \\ \frac{4V_{dc}}{5\pi} [\cos5\alpha_1 + \cos5\alpha_2 + \cos5\alpha_3 + \cos5\alpha_4 + \cos5\alpha_5 + \cos5\alpha_6 + \cos5\alpha_7] &= f_2(\alpha) = 0 \\ \frac{4V_{dc}}{7\pi} [\cos7\alpha_1 + \cos7\alpha_2 + \cos7\alpha_3 + \cos7\alpha_4 + \cos7\alpha_5 + \cos7\alpha_6 + \cos7\alpha_7] &= f_3(\alpha) = 0 \\ \frac{4V_{dc}}{11\pi} [\cos11\alpha_1 + \cos11\alpha_2 + \cos11\alpha_3 + \cos11\alpha_4 + \cos11\alpha_5 + \cos11\alpha_6 + \cos11\alpha_7] &= f_4(\alpha) = 0 \\ \frac{4V_{dc}}{13\pi} [\cos13\alpha_1 + \cos13\alpha_2 + \cos13\alpha_3 + \cos13\alpha_4 + \cos13\alpha_5 + \cos13\alpha_6 + \cos13\alpha_7] &= f_5(\alpha) = 0 \\ \frac{4V_{dc}}{17\pi} [\cos17\alpha_1 + \cos17\alpha_2 + \cos17\alpha_3 + \cos17\alpha_4 + \cos17\alpha_5 + \cos17\alpha_6 + \cos17\alpha_7] &= f_6(\alpha) = 0 \\ \frac{4V_{dc}}{19\pi} [\cos19\alpha_1 + \cos19\alpha_2 + \cos19\alpha_3 + \cos19\alpha_4 + \cos19\alpha_5 + \cos19\alpha_6 + \cos19\alpha_7] &= f_7(\alpha) = 0 \end{aligned} \right\} \quad (3)$$

where, M is the modulation index and can be defined as Modulation index,

$$M = \frac{V_1}{V_{1max}} \quad (4)$$

where,  $V_{1max}$  is maximum obtainable fundamental voltage.

$$V_{1max} = \frac{4kV_{dc}}{\pi}$$

$V_1$  is Actual fundamental voltage.

k is Degree of freedom =  $(L - 1)/2$ .

L is Levels of output voltage.

Generally, Newton-Raphson's iterative approach was applied to solve such a scheme. The big challenge is that it becomes harder to get to the solution as the number of levels gets higher. Furthermore, good initial estimated values of the switching angles are expected. The Genetic Algorithm (GA) was applied in this paper to solve the transcendental Eq. (3) [10]. The objective function is to minimize the total harmonic distortion (THD) with minimization limits set to be transcendental Eqns. (2)-(3). It would result in the minimization of the 5<sup>th</sup>, 7<sup>th</sup>, 9<sup>th</sup>, 11<sup>th</sup>, 13<sup>th</sup>, 17<sup>th</sup> and 19<sup>th</sup> harmonics. Using the GA toolbox in MATLAB, the optimum switching angles of the 15-level proposed MLI under analysis at 0.9 modulation index were found to be 5.6°, 10.9°, 18.6°, 26.5°, 34.8°, 44.6° and 61.2° respectively.

### 3. POWER LOSS MODELS FOR THE PROPOSED INVERTER

While using power semiconductor devices in the design of power converters there are primarily 4-types power losses will occur in the devices during the operation. These types are including: (1) Switching losses (2) Conduction losses (3) Gate driver losses. (4) OFF state losses. Gate driver losses and OFF state losses are very small and generally neglected. Hence the focus is to estimate the switching and conduction losses of the inverter.

For the proposed 15-level inverter the possible harmonics can be eliminated are 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup>, 13<sup>th</sup>, 17<sup>th</sup>, 19<sup>th</sup> harmonics. To eliminate these harmonics, the nonlinear transcendental equations with seven switching angles are required to formulate using Selective Harmonic Elimination PWM as shown in Eq. (3).

### 3.1 Power losses in IGBT

The power losses in the ideal switch are negligible, while the static (conducting) and dynamic (switching) losses in the practical switch have been recorded over the switching cycle shown in Figure 4. During the turn-on and turn-off operation of the semiconductor switch, there would be a switching time of several microseconds and the device absorbs some power when the voltage and currents are non-zero. There is a certain on-state voltage drop on the device (several volts for IGBT) while the switch is in conduction, which results in power (conduction) losses.

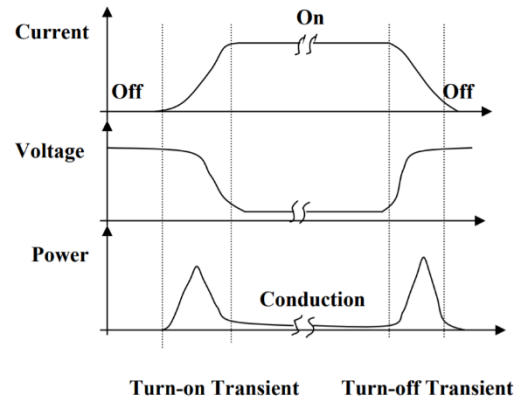


Figure 4. Switching cycle representation of IGBT over a cycle

Power loss in the IGBT limits its use and thus becomes an important problem that cannot be ignored while designing power inverters because it influences the efficiency of the inverter. Power losses act as a heat source inside the semiconductor switch, and this heat will raise the junction temperature and increase the temperature profile inside the device. This is considered a self-heating effect which is more significant when the device is tightly packed.

To prevent destruction and severe damage to the system, the  $T_j$  junction temperature must be retained to the healthy  $T_{jmax}$  operating value typically defined by the manufacturer. Better

configuration provided if the temperature gradient can be correctly predicted within the device under actual operating conditions. Thermal analysis is therefore a critical problem in the design of power converters for optimal stability, performance, and optimization of package design.

### 3.2 Datasheet specifications and thermal characteristics of IGBT

The IGBTs in the proposed 15-level inverter are chosen from Infineon manufacturer, the device model and specifications are given in Table 1.

**Table 1.** Datasheet specifications of IGBT

IGBT Model	IGA30N60H3
Make	Infineon
Collector- Emitter Voltage V <sub>CEO</sub> Max	600V
Continuous Collector Current at 25 <sup>o</sup> C	18A
Continuous Collector Current I <sub>c</sub> Max	11A
Pd - Power Dissipation	43W
Device temperature	25° to 175°C
Gate-Emitter Leakage Current	100nA
Maximum blocking voltage	400V
Device ON state current	120A at 175°C

The IGBT device should also provide with pre-calculated conduction energy losses, turn-on losses and turn-off losses at two different temperatures of 25° and 175° for base values of on-state voltage V<sub>on</sub> and conduction i<sub>on</sub> current as shown in Figure 5.

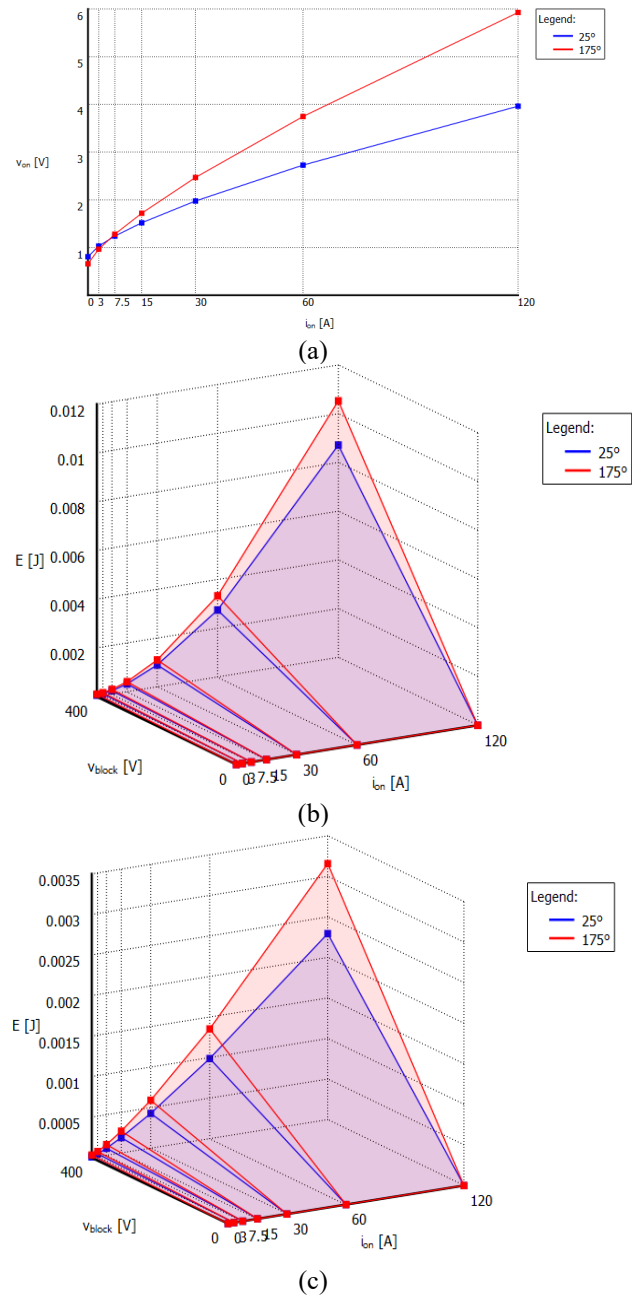
### 3.3 Thermal simulation: Accounting for switching and conduction losses

The thermal operation of electronic power systems is an important aspect, which becomes more important as the demands for portable packaging and greater power density. PLECS requires an early integration of the thermal system with the electrical design and provides a cooling method that is appropriate for each specific use. Furthermore, calculations of switching and conduction loss are quickly carried out. During loss simulations the speed of simulation is not adversely affected as ideal switching is preserved.

PLECS records semiconductor material operating conditions (forward current, voltage blocking, junction temperature) before and after any switching operation rather than evaluating semiconductor switching losses from current and voltage transients. The resulting dissipated energy is then read from a 3D look-up table using these parameters. The dissipated power is determined from the current and temperature of the device during the operation. This synthesis of optimal switching models and accurate loss data presents an inexpensive and precise alternative to detailed device simulation. PLECS integrated visual editor is used to access the appropriate datasets.

### 3.4 Thermal modelling of IGBT using PLECS

PLECS is a software tool that has been developed by Plexim to perform the system level simulation of electric circuits, particularly intended for power electronics but can be used for all power systems. Apart from the electrical system, PLECS includes the ability to model controls and various physical domains such as thermal, magnetic and mechanical systems.



**Figure 5.** Thermal characteristics of IGBT from look-up tables (a) Conduction losses (b) turn\_ON losses (c) Turn\_OFF losses

For IGBT, PLECS uses only one of its dc characteristics, the high-valve output of a control signal that is linearly interpolated according to the user points. With the dynamic properties of this IGBT, it is important especially to accurately model the dependencies of the entire energy from switching  $E_{ts}$  on several variables, such as  $T_j$ , the current collector  $I_C$ ,  $R_G$ , or overvoltage switching. These relationships can be used in PLECS and they are often interpolated linearly, as with the dc characteristics. The system also makes the reliance on the value entered by the user for switching energy losses. The energy values of the on and off losses are entered independently, both for the IGBT and for the reverse diode.

The thermal model of IGBT is shown in Figure 6, which is modelled for one of the IGBT switch of auxiliary circuit of proposed 15-level inverter. The impedance of the thermal model is designed from foster circuit model for junction temperature to case temperature.

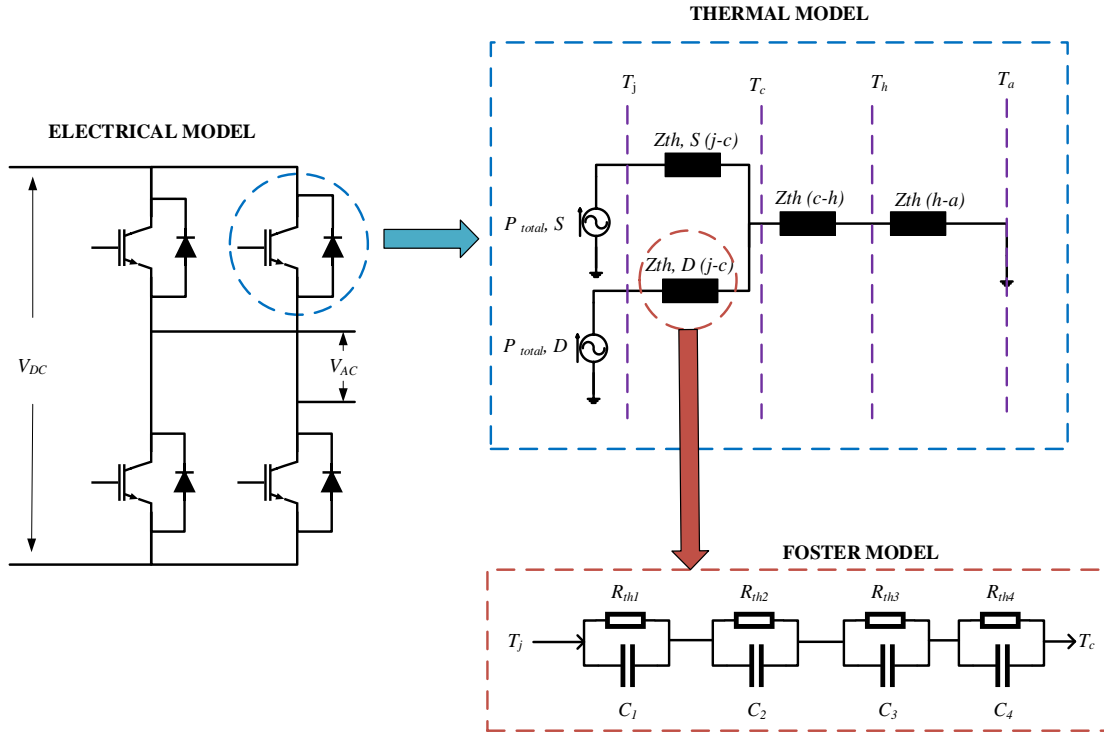


Figure 6. Power loss calculation for proposed 15-level inverter using thermal analysis of IGBTs in PLECS

Considering junction temperature as 1500 C and thermal impedance of  $1.25\Omega$  the foster thermal model is designed on PLECS for 15-level inverter. All the 7- IGBT switches are modelled thermally using heat sink in PLECS simulation for power loss analysis. Both the conduction losses and switching losses are measured using this analysis for both PDPWM (high frequency switching) switching and SHEPWM switching (low frequency switching).

### 3.5 Concept of heat sink

The heatsink absorbs the switching and conduction losses of all devices in its boundary. A heat sink simultaneously describe an isothermal atmosphere and distribute its temperature to the surrounding components. The semi conductors mounted on the heat sink will have same case temperature. The witching energy losses are modelled as direct type pulses on PLECS, having zero width and infinite height. Thus, either the thermal capacitance of the thermal sink needs to be specified or a thermal chain with a capacitance should be used, in order to avoid the infinite thermal resistance to switching energy pulses. The electrical equivalent of thermal circuit with heat sink is described in Figure 7.

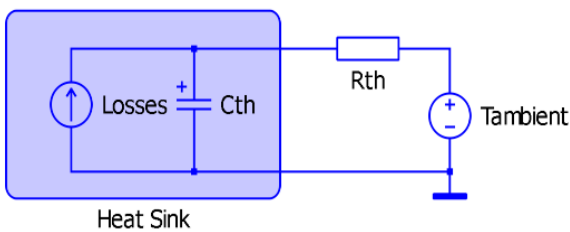


Figure 7. Electrical equivalent of thermal circuit

### 3.6 Calculation of total cycle-average losses

The total power dissipation of each semiconductor is also a factor of interest. The average losses for a device can be determined by adding the losses in the next switching period to the average power pulse. The average cycle method of loss calculation is shown in Figure 8. The C-Script PLECS Block is used to perform integrated loop summing on energy loss operations [18].

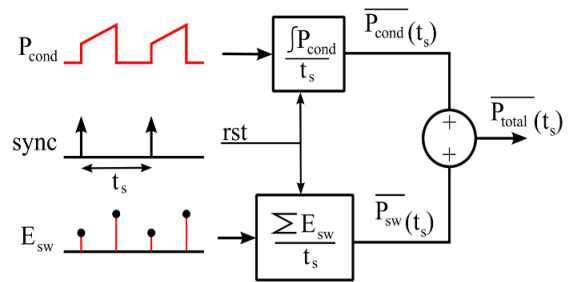


Figure 8. Calculation of total cycle-average losses

## 4. PRECISE CURVE FITTING MODELS FOR POWER LOSS CALCULATION USING SIMULINK

The calculation of inverter losses is a complex task for multilevel inverters relative to two level inverters. Standard methods used to evaluate losses in two-level inverters are not adequate for multilevel inverters. The main reason is that each semiconductor switch has distinct current in multilevel inverters relative to other switches, which involves different loss behavior for each switch. However, at higher levels, each device's switching frequency is not the same, bringing more difficulty to the calculation of losses.

A simplified model for the estimation of power losses of 15-level MLI is proposed in this article. The model being suggested uses the approach used in the ref. [9] with slight modifications. The maximum working temperature is supposed to be 150°. The model being evaluated online using the tool MATLAB-SIMULINK for modeling. The study considered the combined load of  $R = 26.83\Omega$  and  $L = 10\text{mH}$ . The effect is a transition from pure resistive load to pure inductive load contrasted with the situation in which the load varies. The goal is to provide a detailed analysis of the behavior of inverter losses under various load conditions.

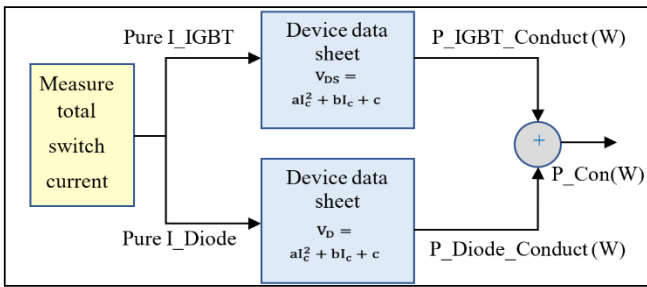
#### 4.1 Conduction loss calculation model

In power semiconductor devices the conduction losses take place during the on-state of the device with conduction current. In proposed inverter the conduction losses will increase proportionally with increase in number of levels. The conduction losses in any on-state device can be computed by taking the product of saturated voltage and conduction current of the device during on-state [10]. It is therefore represented with the following expression.

$$P_{\text{Conduction}} = |I_c| V_{\text{on}}$$

The value of current should be always positive; hence the absolute value is considered. Most literatures model on-state voltage by adding a  $V_o$  voltage that represents a voltage drop in the device called the threshold voltage and a  $R_{\text{on}}$  resistor that indicates the current dependency on the series with ideal device. The key drawbacks to this modeling method,

- 1) Additional elements added in series with the ideal devices, hence rebuilding the circuit is partial.
- 2) The model will not be reliable because it is not based on real device datasheet curves.



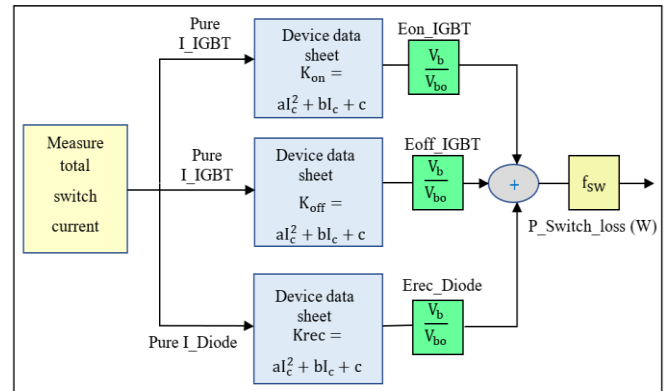
**Figure 9.** Conduction loss calculation process using curve fitting SIMULINK model

The proposed model shown in Figure 9 will compute the conduction losses in simpler and efficient method. Threshold voltage of the device is represented with second order expression in terms of conduction current. Using the curve fitting method, the quadratic equation is derived based on the real curves in the datasheet. The control system has two quadratic equations, one for the switch and one for the diode. The pure switch current and pure diode current must also be measured separately in the MATLAB SIMULINK model. Through measuring the on-state device current, the positive portion is pure switch current, and the negative portion is pure diode current. The conductive losses for the IGBT switch and the diode can be achieved easily by adding the following blocks.

#### 4.2 Switching loss calculation model

The power loss can be described as the dissipation of power while the power semiconductor is switched on and off. The switch and the parallel diode are involved in switching losses. The switching loss is strongly proportional to the frequency of switching and thus contributes significantly to the overall inverter loss, especially for SPWM. The turn-on loss ( $E_{\text{on}}$ ) and the turn-off loss ( $E_{\text{off}}$ ) occur with the power switch. In comparison, only the turn-off ( $E_{\text{rec}}$ ) loss is taken into account in the antiparallel diode because the turn-on loss is usually ignored because of the fast behavior of the diode during forward bias. Turn-on losses are less than 1% relative to turn-off losses in traditional diodes. In reality, there are five key factors influencing switching loss behavior, namely: switching current, blocking voltage, junction temperature, gate resistance and wiring inductance. Switching loss is considered a significant disadvantage in multi-level inverters causing high cost rises and decreased performance in HVDC applications.

This research suggested an online evaluation of losses based on the energy curves of switching given in the data sheet of the device. The curve of energy factor ( $K$ ) is obtained by splitting the current. The curve fitting method is then used to calculate the energy factor curves with polynomials of second order. The multiplication by the switching current of the energy factor curve equation will provide the energy loss, which is further multiplied by the switching frequency to achieve the power loss. Figure 10 displays the block used for the measurement of switching loss.



**Figure 10.** Switching loss calculation process curve fitting SIMULINK model

In general, the switching losses can be calculated during on and off times of the device operation.

Energy loss during MOSFET on time is:

$$E_{\text{on\_SW\_loss}} = V_{\text{CE}} * I_c * \frac{T_{\text{on}}}{2}$$

Energy loss during MOSFET off time is:

$$E_{\text{off\_SW\_loss}} = V_{\text{CE}} * I_c * \frac{T_{\text{off}}}{2}$$

The total energy loss during switching operation,

$$E_{\text{SW\_loss}} = E_{\text{on\_SW\_loss}} + E_{\text{off\_SW\_loss}}$$

The power loss in the operation switch= $(E_{\text{SW\_loss}})/T$ .

$$\text{Total switching losses} = (E_{\text{SW\_loss}}) * f_{\text{SW}}$$

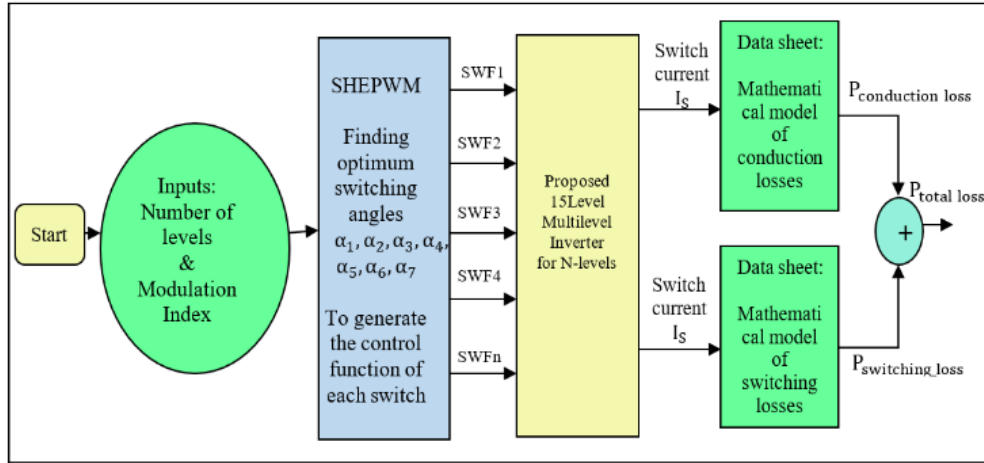
where,

$f_{\text{SW}}$  is Switching frequency,

$E_{\text{SW\_loss}}$  is Total energy loss during switching operation.

### 4.3 Total power loss calculation model

The total power losses by combining Figure 9 and Figure 10 can be evaluated using the model shown in Figure 11.



**Figure 11.** Total power loss calculations with SHEPWM switching curve fitting SIMULINK model

IGBT curve fitting equations from datasheet

$$v_{CE} = -2 * 10^{-7} I_c^2 + 0.0018 I_c + 0.9661$$

$$v_D = -1 * 10^{-7} I_D^2 + 0.0012 I_D + 0.7796$$

$$K_{IGBT-on} = 8 * 10^{-7} I_c^2 - 0.0023 I_c + 4.016$$

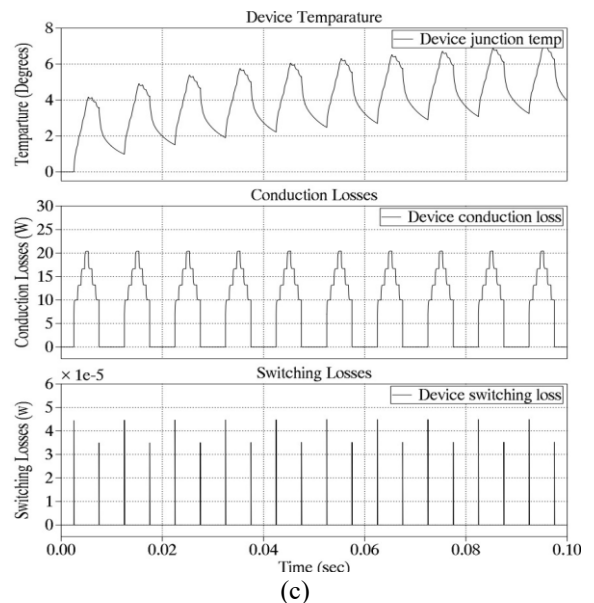
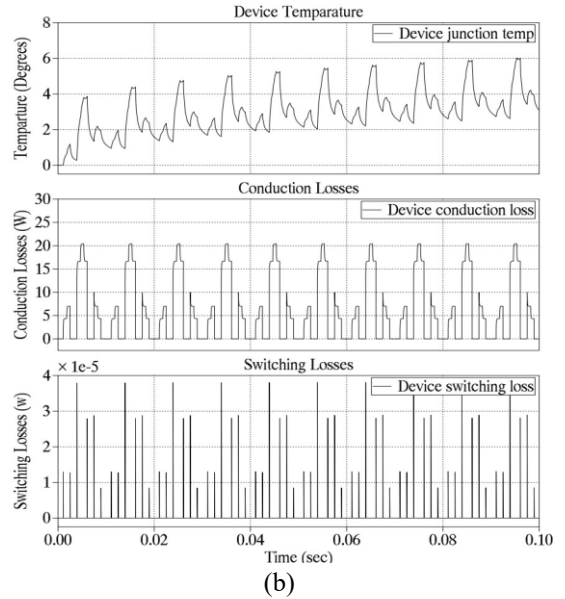
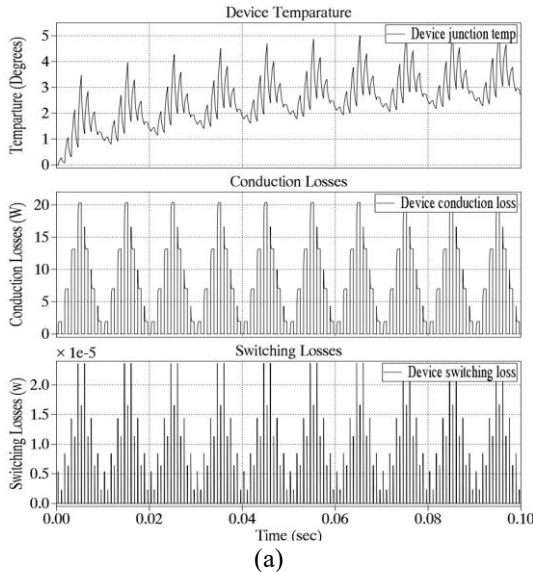
$$K_{IGBT-off} = 3 * 10^{-7} I_c^2 - 0.0011 I_c + 3.1584$$

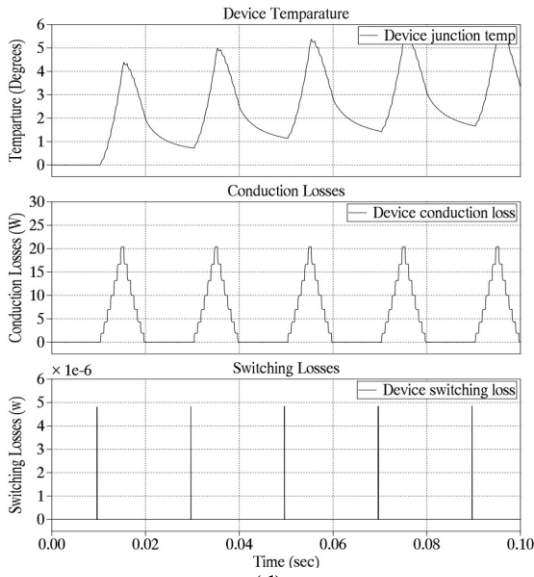
$$K_{Diode-rec} = 7 * 10^{-7} I_D^2 - 0.0039 I_D + 6.6546$$

## 5. RESULTS & DISCUSSIONS

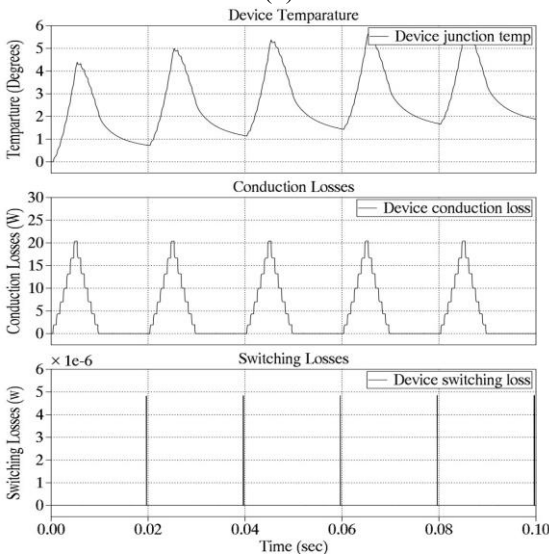
### 5.1 Power loss analysis using PLECS thermal modeling

The switching and conduction losses for both high and low switching frequency controls were plotted using PLECS simulation. The switch wise device temperature, conduction losses and switching losses are plotted in Figure 12 for PDPWM switching. The IGBT swatches 'S1', 'S2' and 'S3' are a high frequency switches in the operation of the proposed inverter hence it undergoes for on and off for several times resulting more switching losses. Similarly, the switches 'S4', 'S5', 'S6' and 'S7' are the low frequency switches, which has low power losses.

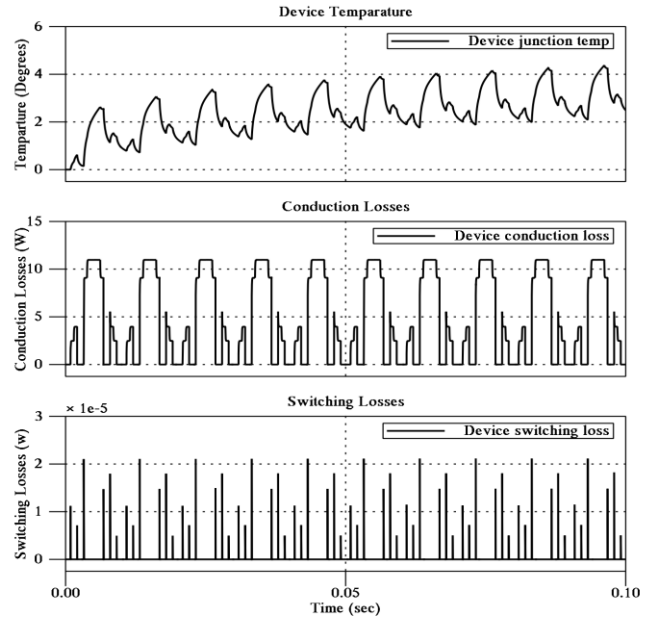




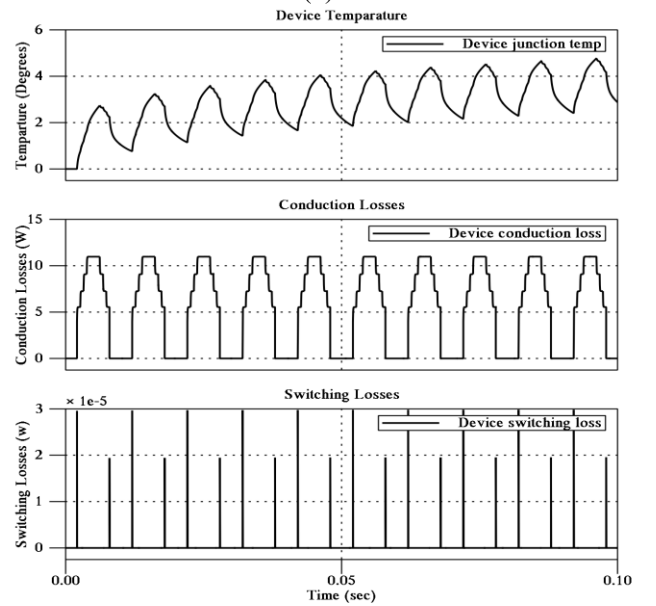
(d)



(e)

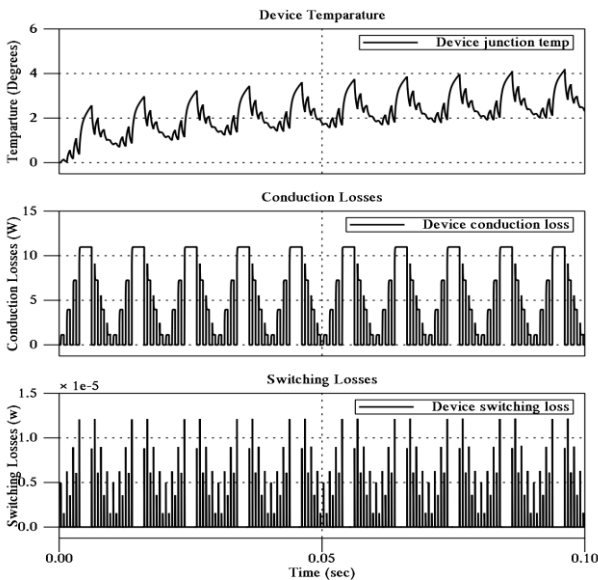


(b)

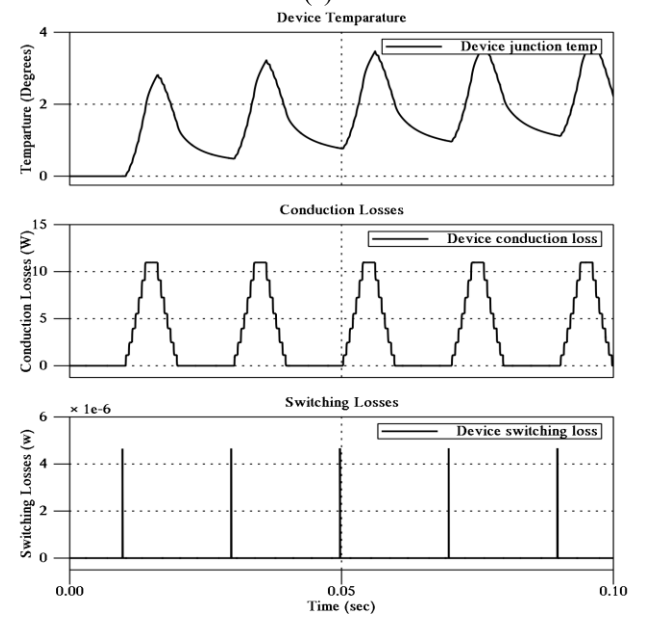


(c)

**Figure 12.** Device Temperature, Conduction Losses & Switching Losses with High Frequency (PDPWM) Switching (a) Switch 'S1' (b) Switch 'S2' (c) Switch 'S3' (d) Switches 'S4 & S5' (e) Switches 'S6 & S7' using PLECS

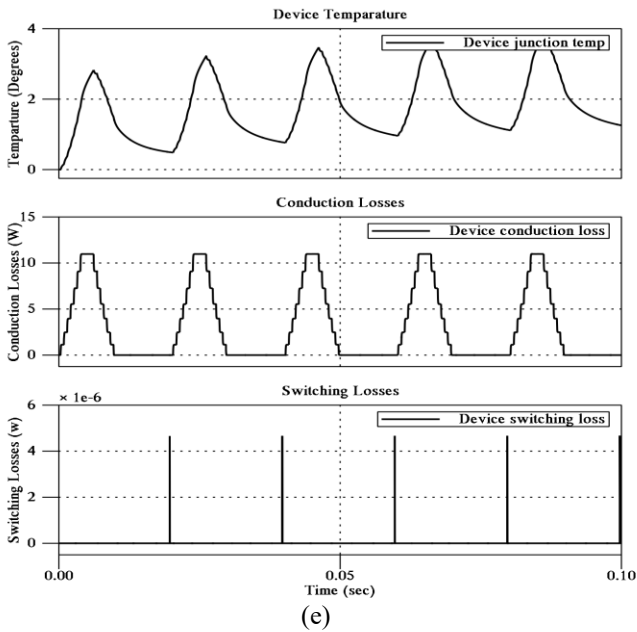


(a)



(d)





**Figure 13.** Device Temperature, Conduction Losses & Switching Losses with Low Frequency (SHEPWM) Switching

(a) Switch ‘S1’ (b) Switch ‘S2’ (c) Switch ‘S3’ (d) Switches ‘S4 & S5’ (e) Switches ‘S6 & S7’ using PLECS

The switch wise device temperature, conduction losses and switching losses are plotted in Figure 13 for SHEPWM switching. From Figures 12 and 13 the magnitude of switching and conduction losses are observed more in PDPWM switching compared to SHEPWM switching. The power losses calculated from both PDPWM and SHEPWM using PLECS simulation are tabulated in Table 2 for each IGBT switch of the 15-level inverter.

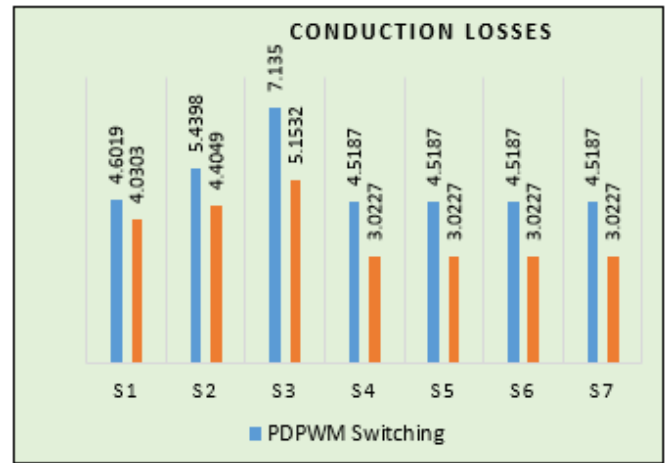
The comparative analysis of conduction losses with high and low switching frequency control methods are given in Figure 14. Here SHEPWM switching gives the less conduction losses than the PDPWM. Also, the switching loss comparison analysis is given in Figure 15 and observed that the switching losses are comparatively low in SHEPWM switching method than PDPWM.

The proposed inverter input power rating is 2500W at 259V and 9.65A of input current. The total power loss measured from high switching frequency method is 35.3W. Therefore,

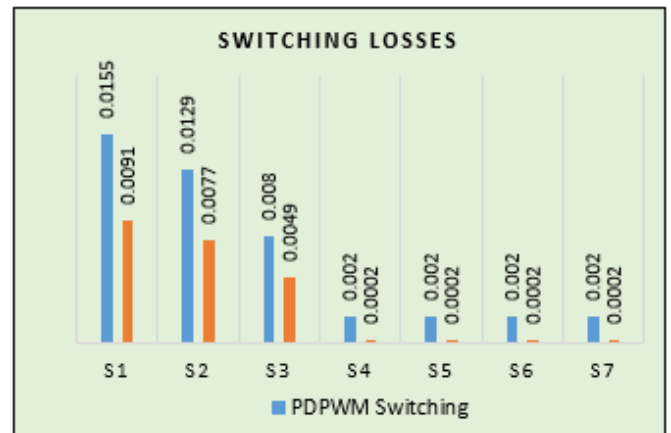
**Table 2.** Power losses & THD with phase disposition (High frequency switching)

Switches	High Frequency Switching (PDPWM)			Low Frequency Switching (SHEPWM)		
	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)
S1	4.6019	0.0155	4.6174	4.0303	0.0091	4.0394
S2	5.4398	0.0129	5.4527	4.4049	0.0077	4.4126
S3	7.135	0.008	7.143	5.1532	0.0049	5.1581
S4	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S5	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S6	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S7	4.5187	0.002	4.5207	3.0227	0.0002	3.0229

the power delivered to the load for high switching frequency control is 2464.7W, which gives the efficiency 98.59% as shown in Figures 16a and 16c. The total power loss measured by low switching frequency control is about 25.7W. The power delivered to the load in this control method is 2474.3W, which gives the efficiency of 98.97% as shown in Figures 16b and 16d.



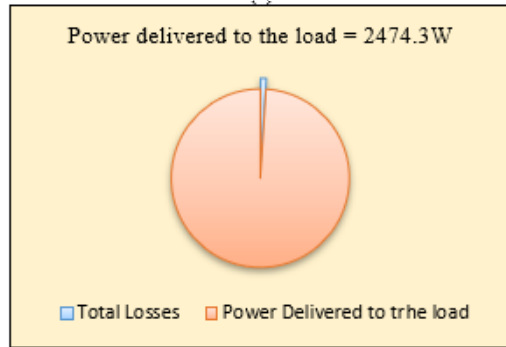
**Figure 14.** Conduction losses comparison with High & Low switching frequency



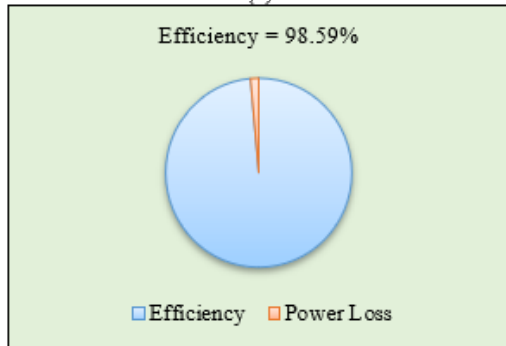
**Figure 15.** Switching losses comparison with High & Low switching frequency



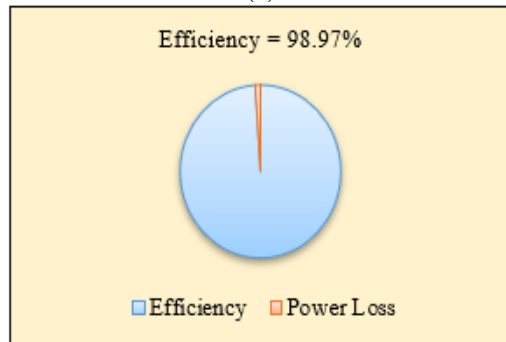
(a)



(b)



(c)



(d)

**Figure 16.** Power Loss Analysis using PLECS thermal modelling (a) High switching frequency (b) Low switching frequency (c) Efficiency with High switching frequency. (d) Efficiency with Low switching frequency

### 5.2 Power loss analysis using precise SIMULINK models

The precise models presented in Figures 9, 10 and 11 are implemented in MATLAB SIMULINK platform using curve fitting methods from device data sheet. The SHEPWM (low frequency switching) control method is implemented with Genetic Algorithm using GA toolbox. The power losses for all the switches in the 15-level inverter is tabulated in Table 3.

**Table 3.** Power loss calculation using SIMULINK models (Low Frequency switching)

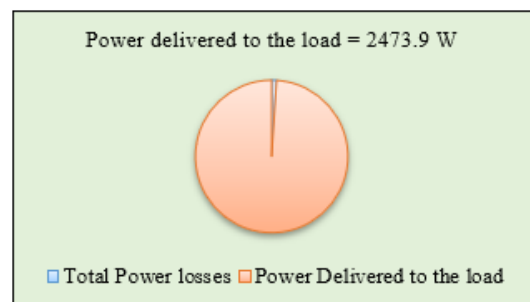
Switches	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)
S1	4.1024	0.00878	4.1112
S2	4.4312	0.00764	4.4388
S3	5.2341	0.00531	5.2394
S4	3.0622	0.00031	3.0625
S5	3.0622	0.00031	3.0625
S6	3.0622	0.00031	3.0625
S7	3.0622	0.00031	3.0625



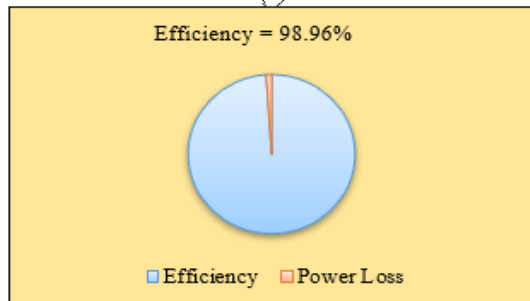
**Figure 17.** Power Loss Analysis using Low frequency (SHEPWM) Switching

The Switching losses, conduction losses and total power losses obtained from SIMULINK models are compared in Figure 17. The total power losses are calculated in this analysis is 26.1W, power delivered to the load is 2473.9W and the corresponding efficiency is 98.96% which are represented in Figure 18a and 18b.

The SIMULINK model presented in Figure 11 has been run for different modulation index and corresponding power losses and THD is tabulated in Table 4. The results show that 0.9 modulation index the THD is minimum of 5.75% and the power losses are 26.04W. The variation of power losses with modulation index is plotted in Figure 19.



(a)



(b)

**Figure 18.** Power Loss Analysis using Precise models in MATLAB SIMULINK (a) Low switching frequency. (b) Efficiency with Low switching frequency

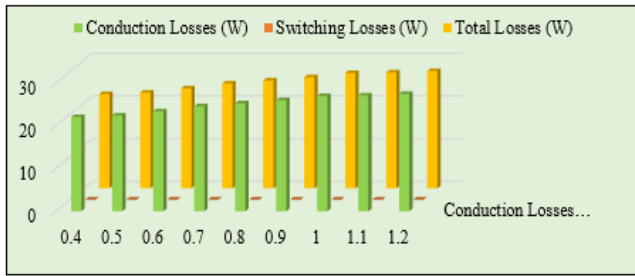


Figure 19. Power losses vs modulation index

Table 4. Power loss & THD variation with modulation index by SHEPWM control

Modulation Index	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)	THD %	Fundamental Voltage
0.4	22.062	0.025	22.08	6.88	209.27
0.5	22.423	0.025	22.44	6.59	220.23
0.6	23.382	0.024	23.40	6.32	232.56
0.7	24.561	0.024	24.58	5.99	234.26
0.8	25.257	0.023	25.28	5.86	240.92
0.9	26.016	0.023	26.03	5.75	245.61
1.0	26.984	0.022	27.00	5.78	252.72
1.1	27.125	0.021	27.14	5.61	258.45
1.2	27.459	0.022	27.48	5.73	258.06

## 6. CONCLUSIONS

Transient losses in semiconductor devices have a significant impact on the performance of the power converter circuit in which they are used. A 15-level asymmetric inverter is designed and implemented with reduced no. of switches suitable for PV applications. The performance of this asymmetric inverter can be analysed based on the total harmonic distortion and power losses. It is extremely crucial to analyse losses in multi-level inverters as accurately as possible. Conduction and switching losses are among the most common types of losses in multi-level inverters. In this paper the power loss analysis of 15-level asymmetric inverter has been presented using Thermal modelling in PLECS and simple and precise curve fitting models in SIMULINK. The switching and conduction losses are evaluated separately considering junction temperature as 150°C and thermal impedance of 1.25Ω the foster thermal model is designed on PLECS for 15-level inverter and corresponding plots were plotted for high frequency switching (PDPWM) and low frequency switching (SHEPWM). The efficiency of the inverter at 0.9 modulation index is proved 98.59% with PDPWM and 98.97% using SHEPWM. Further the precise Simulink curve fitting models are designed on SIMULINK and as per the system datasheet, the model uses exact voltage and energy curves. The overall inverter losses were found to constitute around 1.004% of the total power delivered by the inverter at low switching control with the inverter efficiency of 98.96%. It is concluded that the efficiency of the proposed inverter is approximately same as 98.97% using PLECS modelling and 98.96% using curve fitting models on SIMULINK at low switching frequency control method.

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