PWM strategies dedicated to three-phase two-levels VSI and their impact on AC drives

A review

Nicolas Patin[1], **Romain Cousseau**[1], **Najib Rouhana**[1,2], **The Dung Nguyen**[3]

1. Laboratoire d'Électromécanique de Compiègne,UTC
Rue Roger Couttolenc, 60200 Compiègne, France
nicolas.patin@utc.fr

2. Renault, Technocentre, 1 av. du Golf, 78084 Guyancourt cedex, France

3. Valeo Engine and Electrical Systems
rue André Boulle, 94046 Créteil cedex, France

ABSTRACT. *The aim of this paper is to present a large panel of Pulse Width Modulation (PWM) strategies dedicated to Voltage Source Inverters (VSI) in a generalized framework in order to exhibit their impact on a global system, especially disturbances introduced not only on the DC and AC sides but also on the static converter itself (switching losses). In the introduction, the context of this study is described. Section 2 recalls the model of the three-phase two-level VSI and a generalized carrier-based representation of PWM strategies studied in this paper is given. In section 3, three criteria are given in order to evaluate every strategy. They are applied on several strategies in section 4 and verified with a real test bench in section 5.*

RÉSUMÉ. *L'objectif de cet article est de présenter un large panel de stratégies de Modulation de Largeur d'Impulsions (MLI) dans le cadre le plus général possible afin de mettre en évidence leur impact sur un système global, tout particulièrement du point de vue des perturbations engendrées sur le bus continu et sur la charge mais aussi du point de vue du convertisseur lui-même (*via *des pertes par commutations). Après une description du contexte de cette étude, le modèle de l'onduleur de tensions triphasé à deux niveaux est rappelé et la représentation d'une MLI intersective généralisée est introduite. Trois critères d'évaluation des stratégies MLI sont définis. Ils sont ensuite appliqués à plusieurs stratégies et vérifiés sur un banc d'essai réel.*

KEYWORD: *three-phase VSI, PWM strategies, open-loop, performances, AC side, DC side, switching losses.*

MOTS-CLÉS : *onduleur de tensions triphasé, stratégies MLI, boucle ouverte, performances, côté AC, côté DC, pertes par commutations.*

DOI:10.3166/EJEE.17.203-231 © Lavoisier 2014

European Journal of Electrical Engineering – n° 3-4/2014, 203-231

1. Introduction

In industrial AC drives (Mukhtar, 2010 ; Obegard *et al.*, 1994) as well as in electric powertrains (Larminie and Lowry, 2012), three-phase two-level VSI (see Figure 1) are widely used to fed AC machines (induction (Santisteban and Stephan, 2001) or permanent magnet synchronous machines (Rudnicki *et al.*, 2011)). Even if they are the simplest converters that can be used for this purpose, their control allows a large variety of strategies (Trzynadlowski, 1996) because of two degrees of freedom, which will be highlighted in the following section.

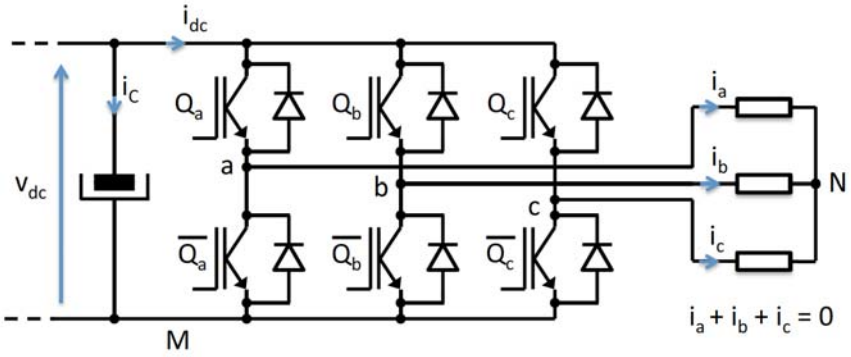

Figure 1. Battery-supplied three-phase two-level VSI

Since the switching mechanism is a key aspect of power electronic converters, its impact on the system has been deeply investigated in the literature. Three negative aspects of this technique are usually highlighted:

– Distortions of AC voltages/currents (Hava, 1998),

– Switching losses in transistors and diodes (Nguyen *et al.*, 2011a),

– RMS current in DC link capacitors (Kolar and Round, 2006).

In practice, a PWM strategy can mitigate its impact on one or two viewpoints among these 3 aspects (AC/DC sides, switching losses) but it is not possible to obtain an optimal behavior for all: a tradeoff is mandatory as it is shown in Section 4.

First, in Section 2, the modeling of the inverter is recalled. Then, three criteria evaluating performances PWM strategies are presented in Section 3. The harmonic flux, introduced in (Hava, 1998), is a synthetic parameter, which is equivalent to the Total Harmonic Distortion (THD), but taking into account the behavior of the three-phase inverter in the $\alpha\beta$ reference frame. Thus, it allows evaluating the quality of voltages provided to the load and, as a consequence, the quality of AC currents as it will be shown in this section.

Thereafter, switching losses are evaluated on the basis of a simplified model as presented in (Nguyen *et al.*, 2011a). The latter one will be especially used in section 4 when comparing Discontinuous PWM with other strategies. Moreover, this section presents a generalized structure of a three-phase PWM controller allowing treating most of the strategies used in practice.

The last criterion introduced in Section 3 is the RMS current in DC link capacitors: it is assumed in this study that this current corresponds to the AC component of the i_{dc} current at the input of the inverter (as shown in Figure 1). Thus, a low impedance of DC link capacitors is required in comparison with the source impedance (DC link inductance, battery impedance, etc.). In practice, this hypothesis is not strictly verified but it should be quite close to the behavior of an actual system. Indeed, it is required in order to limit DC voltage ripples and the electromagnetic interferences induced by a long unshielded cable between batteries and inverter in an electric vehicle for instance.

As mentioned earlier, section 4 is devoted to the evaluation of different families of PWM strategies with regards to the three criteria previously introduced. All PWM techniques studied in this paper can be considered as open-loop ones: closed-loop strategies such as hysteresis current control or Δ–Σ strategies are not treated. However, even if there is no comparison between references and measurements in all presented PWM schemes (open-loop strategies), measurements are used in various controllers that are studied here.

Then, validations are completed in section 5 with experimental results.

Finally, a conclusion presents general results about most of the open-loop PWM strategies that can be found in the literature.

2. Modeling

2.1. Switching functions and voltages

A classical approach for the modeling of a three-phase inverter (as shown in Figure 1) is based on three switching functions defined as follows:

$$\begin{array}{l} C_x = 0 \;\; if \;\; Q_x \; is \; ON \; (and \;\; \overline{Q_x} \;\; is \; OFF) \\ C_x = 1 \;\; if \;\; Q_x \; is \; OFF \; (and \;\; \overline{Q_x} \;\; is \; ON) \end{array} \quad (1)$$

where $x \in \{a, b, c\}$.

Thus, all voltages v_{xM} can be expressed as follows:

$$v_{xM} = v_{dc}.C_x \quad (2)$$

REMARK.– Turn-on, turn-off and dead times are neglected in this model.

However, the load is not sensitive to v_{xM} voltages.

Voltages v_{xN} should be expressed as functions of C_x. For this purpose, a hypothesis about the load must be introduced. Since the load is connected with three wires:

$$i_a + i_b + i_c = 0 \tag{3}$$

Then, it is assumed that this load is balanced. Thus:

$$v_{aN} + v_{bN} + v_{cN} = 0 \tag{4}$$

As a result, it gives:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \frac{v_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} C_a \\ C_b \\ C_c \end{bmatrix} \tag{5}$$

On the basis of the abc-to-αβ transformation, a three-phase vector (without zero-sequence component) can be expressed with αβ components x_α and x_β as follows:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}}_{C_{32}} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{6}$$

And the inverse transformation is:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} C_{32}^t \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{7}$$

The matrix C_{32} exhibits two main properties:

$$C_{32}^t . C_{32} = \frac{3}{2} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{8}$$

And:

$$C_{32} . C_{32}^t = \frac{1}{2} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{9}$$

Thus, Equation (5) can be rewritten as follows:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \frac{2v_{dc}}{3} \cdot C_{32} . C_{32}^t \begin{bmatrix} C_a \\ C_b \\ C_c \end{bmatrix} \tag{10}$$

As a consequence, equivalent voltages $v_{\alpha N}$ and $v_{\beta N}$ provided to the load in the αβ reference frame can be expressed as follows:

$$\begin{bmatrix} v_{\alpha N} \\ v_{\beta N} \end{bmatrix} = \frac{2v_{dc}}{3} \cdot C_{32}^t \begin{bmatrix} C_a \\ C_b \\ C_c \end{bmatrix} \tag{11}$$

This relationship leads to the well-known constellation (see Figure 2) of instantaneous voltages available at the output terminals of the inverter in the αβ reference frame (in this case, v_{dc} is supposed constant and noted V_{dc}).

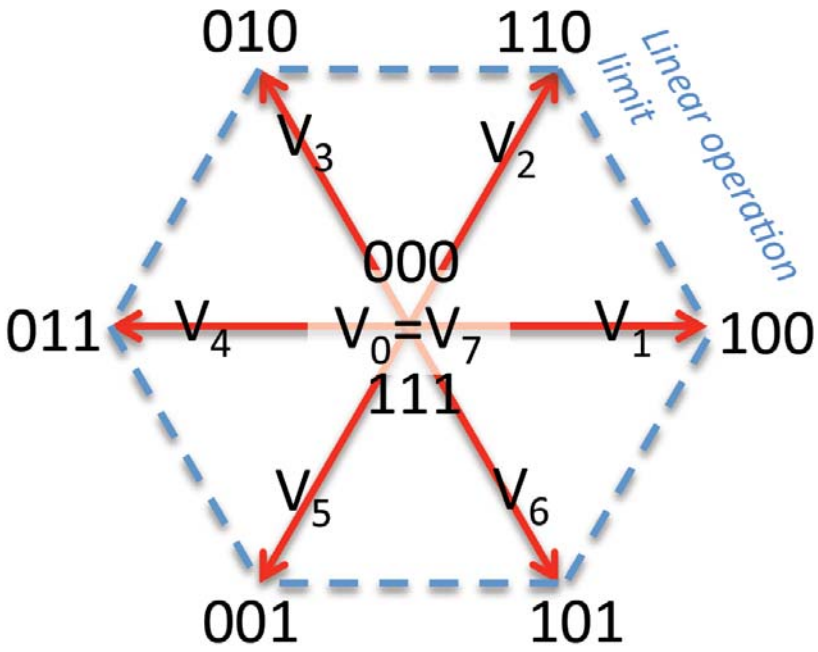

Figure 2. Constellation of instantaneous output voltage vectors in the αβ reference frame

2.2. Currents

The model of the inverter is usually limited to Equation (11). Indeed, the equation related to the input current i_{dc} is omitted. This choice can be justified by the fact that the input voltage source v_{dc} is idealized but this assumption is not strictly verified in practice.

In this case, this input current model must be taken into account. It can be seen that:

$$i_{dc} = C_a.i_a + C_b.i_b + C_c.i_c \tag{12}$$

A *dot product can be recognized* and can be expressed, with the matrix formalism, as follows:

$$i_{dc} = [C_a \quad C_b \quad C_c].\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{13}$$

Then, output currents vector can be expressed according the abc-to-αβ transformation defined in Equation (6) since the sum of these currents is null (see Equation (3)):

$$i_{dc} = [C_a \quad C_b \quad C_c].C_{32} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{14}$$

On the basis of Equation (11), it can be seen that:

$$[C_a \quad C_b \quad C_c].C_{32} = \frac{3}{2v_{dc}} \cdot [v_{\alpha N} \quad v_{\beta N}] \tag{15}$$

Thus, Equation (14) can be rewritten as follows:

$$i_{dc} = \frac{3}{2v_{dc}} \cdot [v_{\alpha N} \quad v_{\beta N}] \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{16}$$

As a consequence, the instantaneous DC current can be seen *as the orthogonal projection* of the αβ current vector on the *line defined by the instantaneous voltage vector* provided to the load. This important result is illustrated in Figure 3 and is used in section 4.

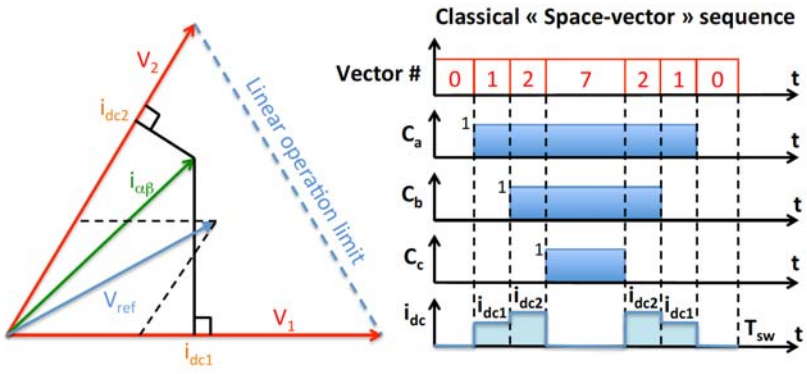

Figure 3. DC current deduced from an αβ-approach

3. Performance criteria

3.1. AC Distortion

In single phase systems, the quality of a given voltage (or current) in comparison with an ideal sinusoidal waveform is evaluated with a quantity called Total

Harmonic Distortion (THD). Two definitions of this quantity can be found in the literature.

First, let us consider a_k and b_k, two coefficients corresponding to the Fourier series of a given T-periodic quantity x(t) defined as follows:

$$x(t) = \sum_{k=1}^{\infty} a_k.\cos\left(\frac{2k\pi t}{T}\right) + b_k.\sin\left(\frac{2k\pi t}{T}\right) \tag{17}$$

With:

$$a_k = \frac{2}{T}\int_0^T x(t).\cos\left(\frac{2k\pi t}{T}\right).dt \text{ and } b_k = \frac{2}{T}\int_0^T x(t).\sin\left(\frac{2k\pi t}{T}\right).dt \tag{18}$$

Then, the first definition corresponds to the IEEE/DIN standard and can be lower or higher than 1:

$$THD_{IEEE/DIN} = \frac{\sqrt{\sum_{k=2}^{\infty} a_k^2 + b_k^2}}{\sqrt{a_1^2 + b_1^2}} \tag{19}$$

The second one is associated to the IEC standard:

$$THD_{IEC} = \frac{\sqrt{\sum_{k=2}^{\infty} a_k^2 + b_k^2}}{\sqrt{\sum_{k=1}^{\infty} a_k^2 + b_k^2}} \tag{20}$$

REMARK.– The signal *x(t)* defined in Equation (17) has a null average value. It is not the most usual expression of a T-periodic quantity but it is usually the case of quantities evaluated with a THD.

This kind of analysis could be used in a three-phase context but an analysis in the αβ reference frame is usually preferred in the literature as it can be seen in (Hava, 1998). The criterion that is obtained from this approach is called *harmonic flux*.

It is based on several hypotheses such as a normalized (according to $v_{dc}/2$) voltage reference $\overrightarrow{V^*}$ (in the αβ reference frame) supposed to be constant during a switching period T_{sw}. This normalized voltage reference is then compared with the normalized instantaneous voltage vector $\overrightarrow{V_l}$ produced by the inverter (with $l = 0\ to\ 7$). The difference $\overrightarrow{\Delta_l}$ between actual voltages vectors (in Volts) can be expressed as follows:

$$\overrightarrow{\boldsymbol{\Delta_l}} = \frac{\boldsymbol{v_{dc}}}{\mathbf{2}}\underbrace{\left(\overrightarrow{\boldsymbol{V_l}} - \overrightarrow{\boldsymbol{V^*}}\right)}_{\overrightarrow{\boldsymbol{\delta_l}}} \tag{21}$$

where $\overrightarrow{\delta_l}$ is a normalized difference (in p.u.).

By means of integration, the harmonic flux, which is a vector noted $\vec{\boldsymbol{\Sigma}}$, is then deduced (Equation (22)):

$$\vec{\Sigma}(t) = \int_0^t \vec{\Delta_t}.d\tau = \frac{v_{dc}}{2}\int_0^t \vec{\delta_t}.d\tau \qquad (22)$$

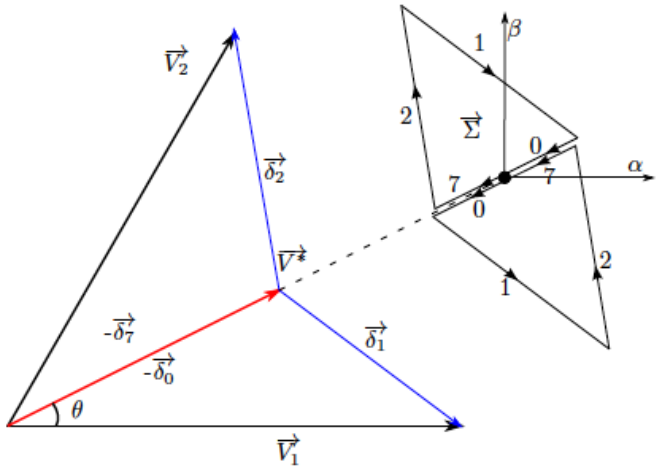

Figure 4. Example of the trajectory of the vector $\vec{\Sigma}$ with a classical SVPWM strategy (in the sector delimited by $\vec{V}_1$ and $\vec{V}_2$)

An example of the trajectory of this vector is illustrated in Figure 4 for a SVPWM strategy in the sector delimited by active vectors $\vec{V}_1$ and $\vec{V}_2$ in the αβ reference frame. The voltage reference $\vec{V^*}$ is obtained as an average output voltage on the basis of application of the following successive instantaneous voltages: $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_2$, $\vec{V}_7$, $\vec{V}_2$, $\vec{V}_1$, $\vec{V}_0$. Since $\vec{\delta}_t = \vec{V}_t - \vec{V}^*$ is a piecewise-constant vector during the switching period, the trajectory of $\vec{\boldsymbol{\Sigma}}$ in the αβ reference frame can be easily split in several segments (numbered with the corresponding output voltage vector: 0, 1, 2, 7, 2, 1, 0) as it is shown in this figure.

REMARK – $\vec{V}_0 = \vec{V}_7 = \vec{0}$ and $\vec{\delta}_t = \vec{V}_t - \vec{V}^*$, thus $\vec{\delta}_0 = \vec{\delta}_7 = -\vec{V}^*$ when $\vec{V}_0$ and $\vec{V}_7$ are applied.

In this case (with a symmetric switching period), it can be seen that the analysis can be limited to a half switching period $T_{sw}/2$ in order to describe this trajectory. Moreover, since $\vec{\delta_t}$ is a piecewise constant vector, the integral can be split in several terms:

$$\vec{\Sigma} = \int_0^t \vec{\Delta_t}.d\tau = \frac{v_{dc}}{2}\cdot\frac{T_{sw}}{2}\int_0^y \vec{\delta_t}.dy \qquad (23)$$

Where $y=2t/T_{sw}$ is the "normalized time".

The factor $\frac{v_{dc}}{2}\cdot\frac{T_{sw}}{2}$ is then noted Σ_0 and a normalized vector $\vec{\sigma}(t)$ is introduced:

$$\vec{\sigma}(t) = \int_0^y \overrightarrow{\delta_\iota} . dy \tag{24}$$

In the case of a classical Space-Vector PWM (SVPWM) strategy, as shown in Figures 3 and 4, the integral (24) can be split into 4 terms during a half switching period:

$$\vec{\sigma}(t) = \int_0^{y_0} \overrightarrow{\delta_{\iota 0}} . dy + \int_{y_0}^{y_0+y_1} \overrightarrow{\delta_{\iota 1}} . dy + \int_{y_0+y_1}^{y_0+y_1+y_2} \overrightarrow{\delta_{\iota 2}} . dy + \int_{y_0+y_1+y_2}^{1} \overrightarrow{\delta_{\iota 7}} . dy \tag{25}$$

With:

- $y_0 = \frac{t_0}{2T_{sw}}$ where t_0 is the time of application of the output voltage vector $\vec{V}_0$,
- $y_1 = \frac{t_1}{2T_{sw}}$ where t_1 is the time of application of the output voltage vector $\vec{V}_1$;
- $y_2 = \frac{t_2}{2T_{sw}}$ where t_2 is the time of application of the output voltage vector $\vec{V}_2$;
- $y_7 = \frac{t_7}{2T_{sw}}$ where t_7 is the time of application of the output voltage vector $\vec{V}_7$

REMARK.– In the classical SVPWM strategy, the times of application of $\vec{V}_0$ and $\vec{V}_7$ are equal (t_0=t_7, thus y_0=y_7).

Even if all calculations can be performed with 2D vectors, it is useful to replace all quantities by equivalent complex ones. Indeed, the normalized voltage reference $\overrightarrow{V^*}$ can be associated to the complex voltage $\overline{V^*}$ as follows:

$$\overrightarrow{V^*} = \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \rightarrow \overline{V^*} = v_\alpha^* + j v_\beta^* = m.e^{j\theta} \tag{26}$$

where $\theta = \omega t$ with $\omega = 2\pi/T_f$ in steady state operation (in this case, m and T_f are constant and are respectively the modulation index and fundamental period).

And all $\overrightarrow{\delta_{\iota k}}$ (with $k \in \{0,1,2,7\}$) can be expressed as follows:

$$\overrightarrow{\delta_{\iota k}} = \vec{V}_\iota - \overrightarrow{V^*} = \frac{4}{3} e^{j\zeta_k} - m.e^{j\theta} \tag{27}$$

Where:

$$\zeta_k = \frac{(k-1)\pi}{6} \quad if \;\; 1 \le k \le 6 \tag{28}$$

And:

$$\zeta_k = 0 \;\; if \;\; k = 0 \; or \; k = 7 \tag{29}$$

The quality of the voltage vector in comparison with an ideal circular trajectory (corresponding to $\overrightarrow{V^*}$ in steady state operation) is then evaluated with the integral of squared norm of $\vec{\Sigma}$ over a switching period:

$$\psi_{T_{sw}}^2 = \int_0^1 \left\|\vec{\Sigma}\right\|^2 . dy \tag{30}$$

Obviously, the analysis of a PWM strategy cannot be limited to a single switching period as in Equations (24)-(25). It is then necessary to analyze over a fundamental period (T_f) that corresponds to one turn of the voltage reference $\overrightarrow{V^*}$ in the αβ reference frame. In practice, $T_f \gg T_{sw}$ and it can be considered that the ratio between these two periods is an integer $N = T_f/T_{sw}$:

$$\psi_{T_f}^2 = \frac{1}{T_f} \sum_{k=0}^{N-1} \int_0^1 \left\|\vec{\Sigma}\right\|^2 . dy \tag{31}$$

Since switching periods are small intervals in comparison with the fundamental period, Equation (31) can be considered as a Riemann's sum that tends to the following integral:

$$\psi_{T_f}^2 = \frac{1}{T_f} \int_0^{T_f} \int_0^1 \left\|\vec{\Sigma}\right\|^2 . dy . dt \tag{32}$$

Due to symmetries over the six sectors defined in Figure 2, Equation (31) can be rewritten as follows:

$$\begin{aligned} \psi_{T_f}^2 &= \frac{6}{T_f} \int_0^{T_f/6} \int_0^1 \left\|\vec{\Sigma}\right\|^2 . dy . dt \\ &= \Sigma_0^2 \times \underbrace{\frac{3}{\pi} \int_0^{\pi/3} \int_0^1 \left\|\vec{\Sigma}\right\|^2 . dy . d\theta}_{\psi_f^2} \end{aligned} \tag{33}$$

The quantity called ψ_f is a normalized harmonic flux that allows comparing different PWM strategies independently from the DC voltage and the switching frequency $F_{sw} = 1/T_{sw}$.

3.2. Switching losses

Losses in the inverters have two origins:

– Conduction losses which are due to the switching resistance R_{DSON} in the conductive state. Hence, they are considered independent of the PWM strategy used for the control;

– Switching losses that deeply depend on the PWM strategy. They are influenced by the actual number of switching cycles per second and can be reduced with dedicated strategies.

Thus, this second term is a good indicator of the performances of a PWM strategy because, whatever the operating point of the load, conduction losses cannot be impacted by the PWM strategy. Indeed, it is possible to compare different

strategies from this point of view, which impacts the efficiency of the static converter and the size of the required heat sink.

A simplified model of the switches is often used for the purpose. Indeed, the dissipated energy E_{sw} during a switching period can be expressed as follows:

$$E_{sw} = \frac{1}{2}(t_{ON} + t_{OFF}).V_{CE}.|i_k| \tag{34}$$

Where:

– t_{ON} and t_{OFF} are turn-on and turn-off times (not neglected only in this paragraph) ;

– V_{CE} is the switched voltage (v_{dc} in the case of the inverter) ;

– i_k is the output current of a given leg ($k \in \{a, b, c\}$)

REMARK.– This model is based on strong hypotheses concerning waveforms because, in order to obtain the Equation (34), voltages and currents in switches are supposed to follow trapezoidal waveforms.

As a consequence, the average switching losses (in Watts) over a fundamental period, in one leg *k*, are:

$$\langle p_{sw} \rangle = \frac{(t_{ON} + t_{OFF}).v_{dc}}{T_f} \sum_{k=1}^{N} |i_k(kT_{sw})| \tag{35}$$

REMARK.– In Equation (35), the current i_k is assumed constant during a switching period.

Same as Equation (31), a Riemann's sum appears in Equation (35) and it leads to:

$$\langle p_{sw} \rangle = \frac{1}{2\pi} \frac{(t_{ON} + t_{OFF}).v_{dc}}{T_{sw}} \int_0^{2\pi} |i_k(kT_{sw})|.d\theta \tag{36}$$

However, it must be noticed that this formula can only be applied in the case of Continuous PWM (CPWM) in opposition to Discontinuous PWM (DPWM) that will be presented in the next section.

In fact, all continuous PWM strategies lead, in sinusoidal steady state operation, to the following result:

$$\langle p_{sw} \rangle_0 = \frac{2}{\pi} \cdot \frac{(t_{ON} + t_{OFF}).v_{dc}}{T_{sw}} \cdot \hat{I} \tag{37}$$

where $\hat{I}$ is the amplitude of AC currents in the load.

In the case of DPWM strategies, Equation (36) should be replaced by the following one:

$$\langle p_{sw} \rangle = \frac{1}{2\pi} \frac{(t_{ON} + t_{OFF}).v_{dc}}{T_{sw}} \int_0^{2\pi} |f_k(kT_{sw})|.d\theta \quad (38)$$

where $f_k(t)$ is equal to:

– $i_k(t)$ if the leg k is switched during the considered time interval ;

– 0 if the leg is not switched during the considered interval.

Then, all strategies are compared to CPWM ones with a ratio called Switching Loss Factor (SLF) defined as follows:

$$SLF(\%) = 100 \times \frac{\langle p_{sw} \rangle}{\langle p_{sw} \rangle_0} \quad (39)$$

3.3. RMS Capacitor current

The two previous criteria evaluate performances of PWM strategies with respects to AC side and internal losses in the inverter. The third criterion to be introduced in this paper allows us to evaluate the capability of a given PWM strategy to reduce the stress of DC link capacitors at the input of an inverter.

Indeed, it has been shown in (Nguyen *et al.*, 2010) that the DC voltage ripples are not really an issue in such a design: the main constraint is the capability for DC link capacitors to support the AC component of the DC current absorbed by the inverter. Thus, these capacitors, especially in low voltage applications (such as in micro-hybrid vehicles for instance), are not chosen by the power electronics designer on the basis of their capacitance but on their rated RMS current.

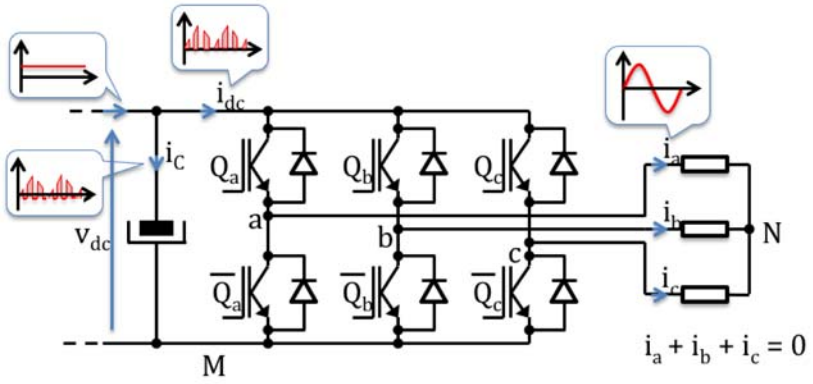

Figure 5. Separation hypothesis between AC and DC currents on the DC bus (respectively in the capacitor and the DC source)

The theoretical framework (illustrated in Figure 5) used within this context supposes that the current flowing through the DC cable from the source (e.g. a

battery) to the converter (and to the DC link capacitors) is constant. Thus, the RMS value I_C^{RMS} of the capacitor current is expressed as follows:

$$I_C^{RMS} = \sqrt{(I_{dc}^{RMS})^2 - \langle i_{dc} \rangle^2} \tag{40}$$

Where:

$$\left(I_{dc}^{RMS}\right)^2 = \frac{1}{T_f}\int_0^{T_f} i_{dc}^2(t).dt \tag{41}$$

And:

$$\langle i_{dc} \rangle^2 = \left(\frac{1}{T_f}\int_0^{T_f} i_{dc}(t).dt\right)^2 \tag{42}$$

Moreover, the currents in the load are supposed to be sinusoidal.

It will be shown in the next section that this capacitor current can be analytically expressed in the case of a large class of PWM strategies (including the SVPWM strategy) and can be reduced by the use of Double Carrier PWM (DCPWM) strategies. Thus, as for SLF, a comparison can be easily performed with a ratio I_C^{RMS}/I_{C0}^{RMS} where I_{C0}^{RMS} is the RMS capacitor current obtained for a strategy used a reference (usually the SVPWM).

4. PWM Strategies

4.1. Generalized controller

As it is shown in (Hava et Çetin, 2011), a generalized PWM strategy can be obtained with the control scheme presented in Figure 6.

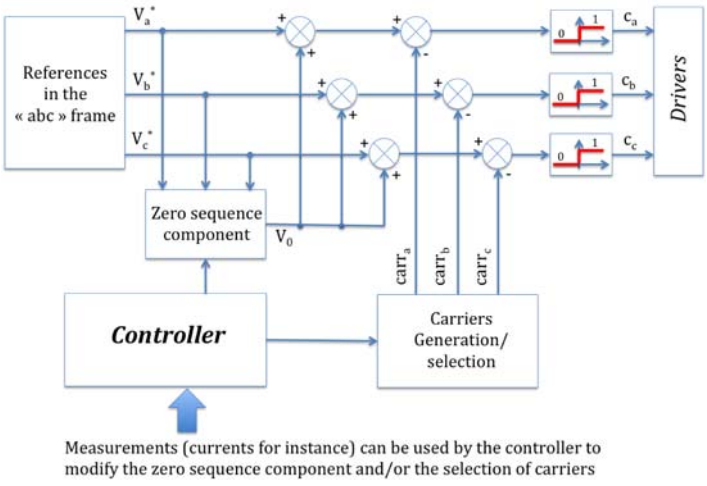

Figure 6. Generic structure of a three-phase PWM controller

Indeed, the average value of a switching function (*i.e.* duty ratio) does not depend on the carrier. Moreover, the zero sequence component V_0, injected to the three voltage references in Figure 6, does not appear in the line-to-line voltages thus it has no impact on the three-phase load connected to the inverter.

This important result can be easily verified with the expression of the complete abc-to-αβ0 transformation that adds the zero sequence component x_0 to the Equation (6):

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}}_{C_{32}} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} + \underbrace{\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}}_{C_{31}} \cdot x_0 \tag{43}$$

Then, it must be noticed that:

$$C_{31}^t . C_{32} = [0 \quad 0] \tag{44}$$

And:

$$C_{32}^t . C_{31} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{45}$$

Thus, according to the Equation (10), the introduction of a zero sequence component in the vector $[C_a \quad C_b \quad C_c]^t$ or more precisely on its average value $[\alpha_a \quad \alpha_b \quad \alpha_c]^t$ (*i.e.* duty ratios $\alpha_k = \langle C_k \rangle$, $k \in \{a, b, c\}$) has no impact on $[v_{aN} \quad v_{bN} \quad v_{cN}]^t$ (or at least $[\langle v_{aN} \rangle \quad \langle v_{bN} \rangle \quad \langle v_{cN} \rangle]^t$).

4.2. Categories

It can be considered two main categories according to the choice of a zero sequence component:

– A class of PWM strategies that uses a continuous function for this purpose, they are called Continuous PWM strategies (CPWM);

– A complementary class that uses a discontinuous function (they are so-called Discontinuous PWM – or DPWM) allowing maintaining the state of a leg (*i.e.* without commutation) for all switching periods;

Obviously, DPWM strategies avoid commutations and allow the reduction switching losses in comparison with CPWM ones

4.2.1. Carriers – One degree of freedom

Considering the choice of carriers, only two different types are actually used in practice (corresponding strategies are called Double Carrier PWM – or DCPWM): opposite ones as shown in Figure 7.

REMARK.– Obviously, different waveforms can be used (triangles, sawtooth, etc.).

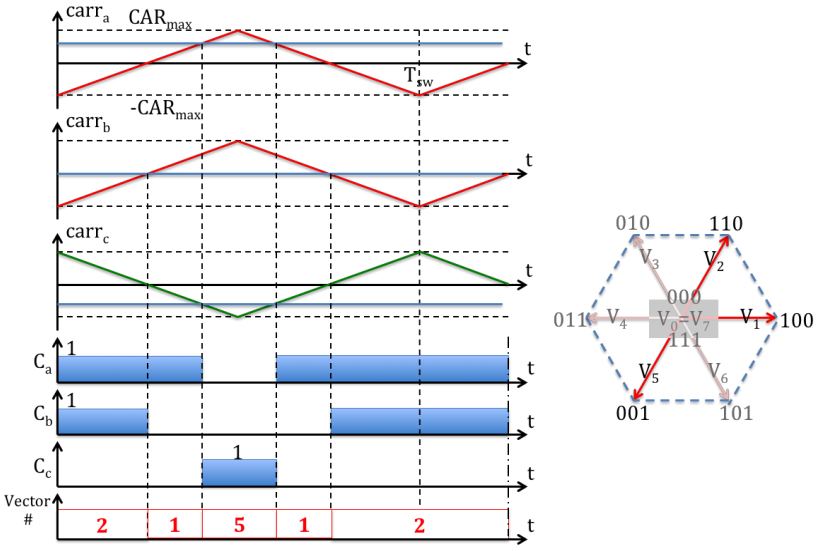

Figure 7. Double carrier strategy and active vectors

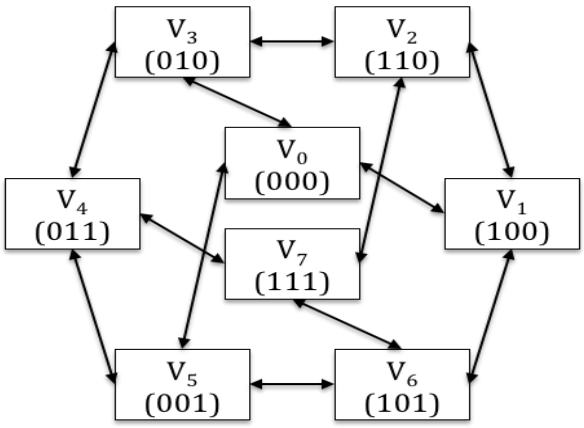

Figure 8. Useable transitions between all voltage vectors

As it can be noticed from Figure 7, the sequence generated is composed of three non-adjacent active voltage vectors. Please notice that the transition from voltage vector 2 to vector 1 induces one commutation per transition. For the transition from 1 to 5 or 5 to 1, it induces simultaneous commutations per transition which are not completely feasible because simultaneous commutations are not guaranteed practically (feasible transitions are illustrated in Figure 8). Nevertheless, these kinds

of sequences has been studied in (Hava et Çetin, 2011) for the mitigation of the common mode voltage applied to the load (with regards with the ground reference, in order to reduce bearing currents for instance).

Moreover, with this sequence, it can be seen that null vectors V_0 and V_7 are avoided. This property of Double Carrier PWM techniques is of a great interest if a reduction of the RMS capacitor current is needed.

This result can be explained by the fact that a null voltage vector corresponds to a null DC input current. Thus, if a reduction of the variations of i_{dc} current is targeted, the use of only active voltage vectors should be preferred as for the DCPWM presented in (Hobraiche *et al.*, 2009). In this first study, it has been shown that the global hexagon defined in Figure 2 can be split into several areas (see Figure 9) corresponding to different control schemes.

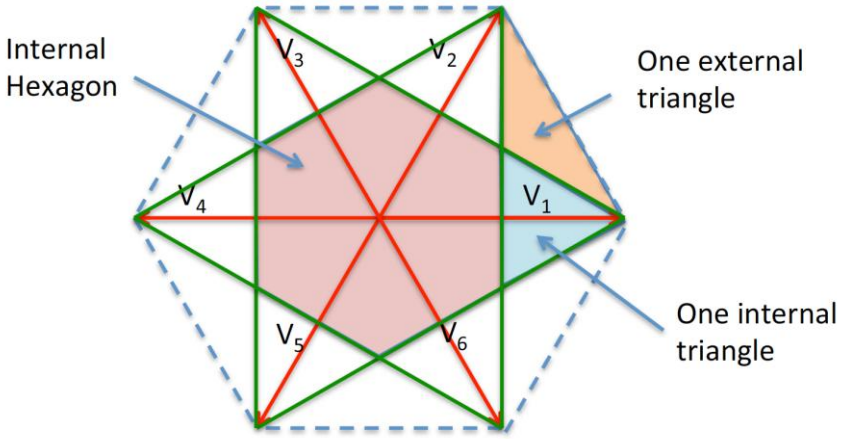

Figure 9. Decomposition of the hexagon in the DCPWM strategy

In the internal triangles (such as the one aligned with V_1 in Figure 9), the voltage reference can be obtained with three active vectors (V_6, V_1 and V_2) during a switching period. Null vectors are not needed and as a consequence, i_{dc} is always different from zero. Thus, in major cases, the RMS current in DC link capacitors is significantly reduced (in fact, performances depend on the power factor of the load). However, the drawback of this technique is that, since three active vectors (with 120° between V_6 and V_2) are used, induced AC currents ripples are intuitively higher than the ones obtained with a SVPWM strategy. This is confirmed in the next paragraph with the corresponding harmonic flux ψ_f.

In the external triangles (and for instance, in the one pointed in Figure 9), the same strategy with three consecutive active vectors can be applied. However, the solution is not unique: two sequences can be used:

– V_6, V_1 and V_2 ;

– V_1, V_2 and V_3

This choice is free and can be made based on another objective, other than the fact of reducing the DC link capacitor current: to minimize the switching losses in the inverter. Indeed, it must be noticed that both sequences maintain one leg in a given state:

– In the case (V_6, V_1, V_2), it can be seen (in Figure 8) that $C_a = 1$ during all time ;

– In the case (V_1, V_2, V_3), it can be seen that $C_c = 0$ during all time

Thus, this strategy belongs to the *Discontinuous PWM family*.

In the internal hexagon, the application of null vectors is mandatory and this strategy cannot be used anymore. In fact, the use of a Double Carrier seems to be useless but in more recent studies (Nguyen *et al.*, 2011b), it has been shown that it is still applicable and efficient.

4.2.2. Zero sequence component – the second degree of freedom

As it is shown in the previous paragraph, it is always possible to maintain the state of a leg for all switching periods in an inverter. Many strategies based on this principle and grouped into a category called DPWM, have been extensively studied in the literature. Nowadays, an optimal strategy (for all operating points of the inverter/load) is known and called Generalized Discontinuous PWM (GDPWM) (Narayanan *et al.*, 2006). A direct digital technique (DDT-GDPWM) for the implementation of the GDPWM in a real time context (on a DSP, not only for the steady state operation mode) has been also proposed in (Nguyen *et al.*, 2011a).

The principle of this implementation can be described as follows:

Algorithm 1. DDT-GDPWM algorithm

Let us consider a given triplet $(\alpha_a, \alpha_b, \alpha_c)$
Calculate the M and m indexes of respectively $max(\alpha_a, \alpha_b, \alpha_c)$ *and* $min(\alpha_a, \alpha_b, \alpha_c)$
Measure currents in all legs: i_a, i_b, i_c
Compare i_M *and* i_m
  if $|i_M| > |i_m|$ **then**
    calculate *the following zero sequence* α_0: $\alpha_0 = 1 - \alpha_M$
  else
    calculate *the following zero sequence* α_0: $\alpha_0 = -1 - \alpha_m$
  end if
The actual duty ratios applied to the inverter are $(\alpha_a + \alpha_0, \alpha_b + \alpha_0, \alpha_c + \alpha_0)$

This algorithm can be translated in a single simple sentence: “the duty ratios are shifted in order to maintain the state of the leg, which is crossed by the maximum current in absolute value, blocked.”

4.2.3. The Uni-DCPWM: a mixed strategy

The use of two carriers is not exclusive. It can be associated to the use of a discontinuous zero sequence component as it is naturally obtained with the DCPWM presented in the paragraph 4.2.1.

However, in this strategy, two opposite carriers are only used in internal and external triangles. In the internal hexagon, a single carrier strategy is used (a GDPWM for instance).

The initial principle of this strategy is to avoid the usage of null voltage vectors in order to reduce the DC current ripples. It can be easily shown that this solution is possible only outside the internal hexagon. But, even if null voltage vectors cannot be avoided in this case, the time of applications of these vectors can be minimized if two non-adjacent active voltage vectors are applied during the switching period.

Indeed, for a given voltage reference (in sector I, between V_1 and V_2 for instance), a classical SVPWM strategy applies V_1 and V_2 during time intervals $\lambda_1.T_{sw}$ and $\lambda_2.T_{sw}$ respectively and then, switching period is completed with null vectors during a global time interval $(1-\lambda_1-\lambda_2).T_{sw}$. If non-adjacent voltage vectors are used (V_1 and V_3 or V_6 and V_2 for instance), the corresponding application times will be longer than the ones obtained with the SVPWM strategy. Thus, the time interval devoted to the null vectors will be reduced as needed.

This kind of behavior is reached by using a GDPWM (with the same algorithm that the one presented in the previous paragraph) associated to 2 opposite carriers. This modified GDPWM, called Unified DCPWM (or Uni-DCPWM) in (Nguyen *et al.*, 2011b) can be easily implemented on a DSP or a FPGA because its behavior can be summed up as follows:

– One leg is maintained in a constant state during a switching period (as the classical GDPWM);

– The two other legs are controlled by two PWM signals generated with two opposite carriers.

The waveforms presented in Figure 10 allow verifying that Uni-DCPWM can produce either three (consecutive) active vectors or two non-adjacent vectors during a switching period.

Table 1 synthesizes the classification of all the strategies presented in this paper.

Table 1. Classification of PWM strategies

Zero-sequence / Carriers	Continuous function	Discontinuous function
Single carrier	SVPWM	DPWMx, GDPWM
Double carrier	*Not studied here*	DCPWM, Uni-DCPWM

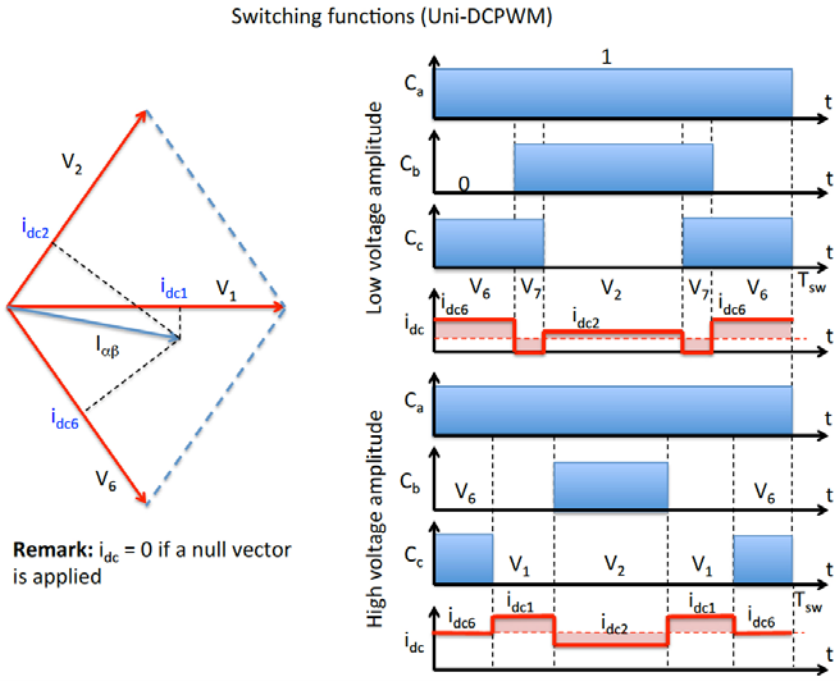

Figure 10. Waveforms at two different operating points with a Uni-DCPWM strategy

4.3. Theoretical performances

4.3.1. SVPWM and analytical results

The interest of the SVPWM is that it is a widely used PWM strategy in industrial applications. Moreover, its simplicity allows obtaining analytical results for all criterions introduced in section.

The expression of the *harmonic flux* ψ_f with this strategy has been established in (Hava, 1998):

$$\psi_f(m) = \sqrt{\frac{3}{\pi}\left[\frac{\pi}{36}m^2 - \frac{2\sqrt{3}}{27}m^3 + \left(\frac{\pi}{32} - \frac{3\sqrt{3}}{128}\right)m^4\right]} \quad (46)$$

It must be noticed that, in this case, it only depends of the modulation index m that is linked to the amplitude of the voltage reference ($0 \leq m \leq \frac{2}{\sqrt{3}}$ in the linear operation mode, *i.e.* without over-modulation). The corresponding curve is given in Figure 11 and it is noted ψ_{f0} since it is considered as a reference for all other PWM strategies.

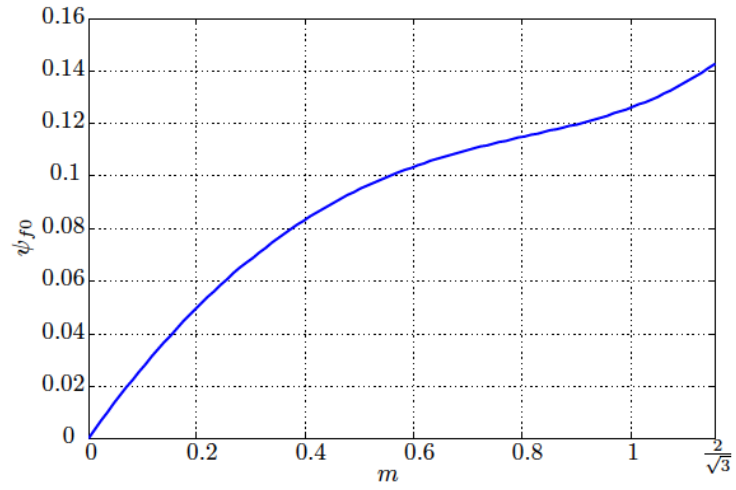

Figure 11. Harmonic flux ψ_f vs. modulation index m for the SVPWM

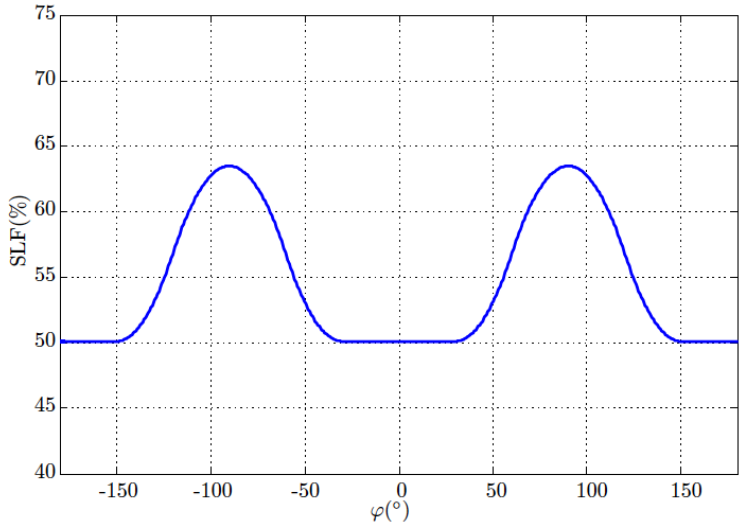

Figure 12. Switching Loss Factor vs. φ for the GDPWM

The *Switching Loss Factor* (SLF) for this strategy is the same that for all other CPWM strategies (such as Sinusoidal PWM – SPWM): it *is equal to 1* since *SVPWM is used as the reference for switching losses* as it is explained in the paragraph 3.2 with the expression (35) of switching losses in this case.

Finally, the calculation of the RMS current in DC link capacitors has been proposed for the SVPWM in (Dahono *et al.*, 1996). The obtained result is the following:

$$I_C^{RMS} = \hat{I} \times \sqrt{\frac{\sqrt{3}m}{4\pi} + \left(\frac{\sqrt{3}m}{\pi} - \frac{9m^2}{16}\right) \times \cos^2(\varphi)} \tag{47}$$

Where m is the modulation index, $\hat{I}$ is the amplitude of the load currents and φ is the phase between the current vector $I_{\alpha\beta}$ and the voltage reference V^* in the αβ reference frame.

4.3.2. GDPWM and reduction of switching losses

As it has been explained previously, the interest of the GDPWM is to reduce as much as possible the switching losses in the inverter. It can be verified with the SLF given in Figure 12.

For reasonable power factors ($-30° \leq \varphi \leq +30° \Rightarrow \cos\varphi \geq 0.866$), switching losses are divided by 2 in comparison with the ones obtained using a SVPWM strategy.

Obviously, this kind of strategy is still based on adjacent active vectors during a switching period. Thus, the DC link capacitor current is equivalent to the one obtained with this strategy.

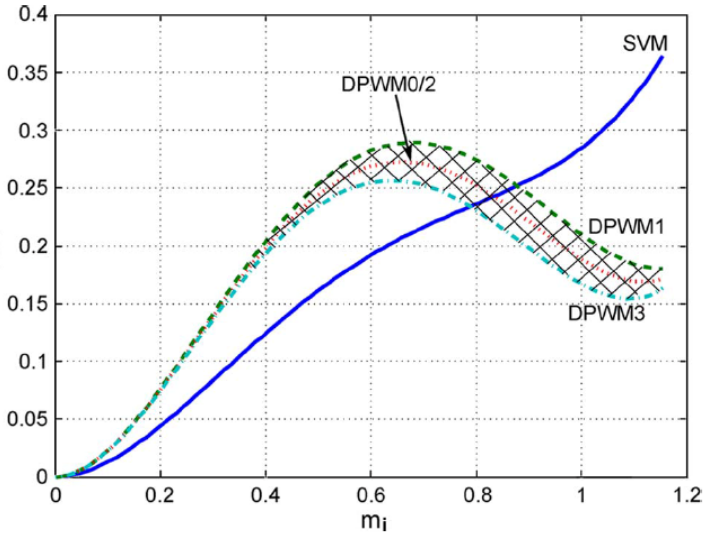

Figure 13. Harmonic flux ψ_f vs. modulation index m (noted here m_i)

On the other hand, the harmonic flux obtained with this strategy is more complex to analyze as it can be seen in Figure 13. The curve noted SVM corresponds to the SVPWM already presented in Figure 11 and the shape between curves noted DPWM3 and DPWM1 (two particular DPWM strategies) corresponds to the envelop in which the curve associated to the GDPWM takes place. As a result, it can be noticed that the distortion introduced by this strategy can be higher or lower than the one obtained with the SVPWM. For low voltages, the SVPWM is always the better strategy but with high voltages (for $m \geq 0.8/0.9$ approximately), the DPWM strategies (and more particularly, the DPWM3) are much better solutions.

4.3.3. Uni-DCPWM, DC current, switching losses and AC distortion

The main objective of the Uni-DCPWM is to reduce the RMS current in DC link capacitors. As it is shown in Figure 14, this goal is reached in all practical cases both in motor and in generator operating modes (around $\varphi = 0°$ and $\varphi = 180°$).

In this cartography, it can be seen that the RMS current in DC link capacitors is reduced (ratio inferior to 1) for all values of the modulation index (from 0 to $\frac{2}{\sqrt{3}} \approx 1.155$) with power factors higher (in absolute value) than 0.643.

Thus, these performances are very satisfying even if this current can be increased in comparison with the SVPWM for low power factors. It could be explained with the fact that, in this case, even if active vectors are applied, at least one of these vectors will lead to a *negative* i_{dc} current. The fact that null vectors are avoided *does not guarantee for all cases that the best result is reached*: it is only a good choice for realistic cases.

As for the switching losses, since the Uni-DCPWM is based on the algorithm of a GDPWM, the same performances are obtained. Thus, the curve of the SLF is identical to the one presented in Figure 12.

Two key criteria are satisfied with this strategy: SLF and RMS current in DC link capacitors. Unfortunately, it is not possible to obtain good performances for all criteria with a single PWM strategy. Indeed, a tradeoff is always required, as for all engineering domains, because the Uni-DCPWM brings a significant distortion in output voltages as it can be seen in Figure 15 with the corresponding harmonic flux.

Even if the harmonic flux depends on the voltage-current phase shift φ, it can be seen that it is always greatly higher than the one obtained with the SVPWM.

It will be shown in the next section that it is not critical because AC currents ripples can be acceptable if the switching frequency is correctly tuned (@ F_{sw} = 10kHz, AC currents ripples are satisfying in our test bench for instance). However, a designer should pay attention about this drawback of the Uni-DCPWM strategy because it tends to produce a noisy AC drive. Indeed, harmonic content of currents could be important enough to be able to excite mechanical resonances of the supplied machine.

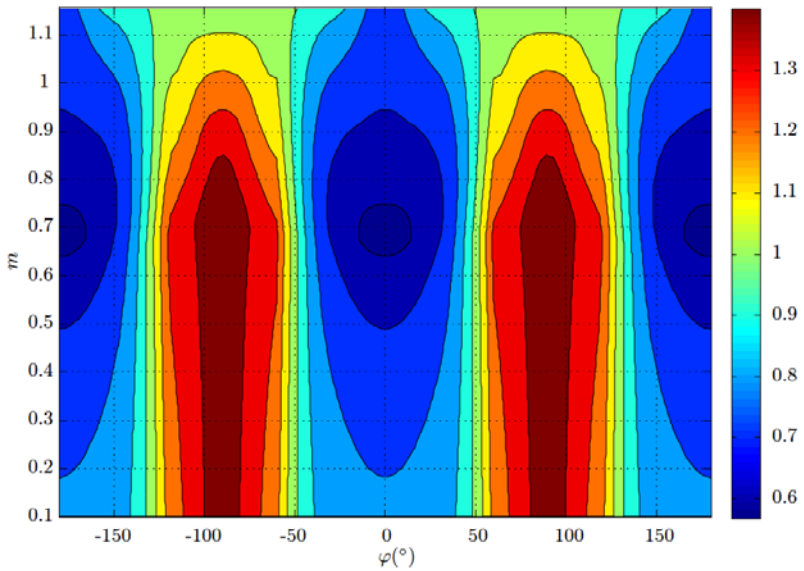

Figure 14. Cartography of the ratio between I_C^{RMS} for the Uni-DCPWM and the one obtained with the SVPWM

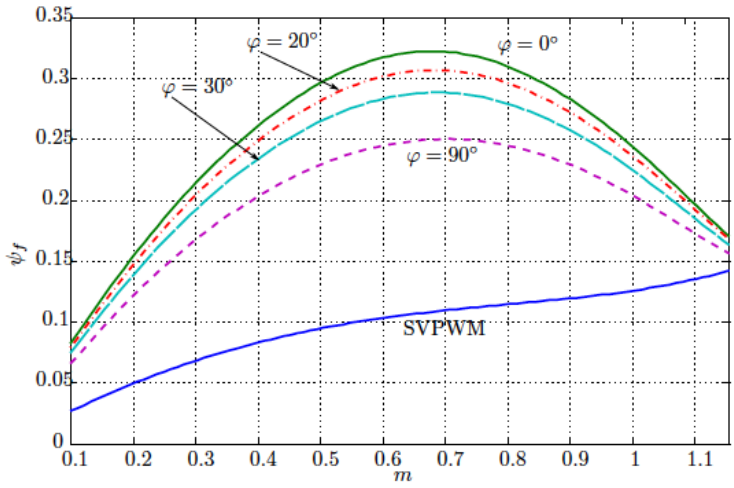

Figure 15. Harmonic flux ψ_f for the Uni-DCPWM

5. Experimental results

All theoretical results presented in the previous section are based on strong hypotheses that must be checked in order to validate results in practice.

The main problem is that AC currents are supposed to be sinusoidal in order to evaluate:

– The switching losses;

– The RMS current in DC link capacitors.

For this second criterion, it is also supposed that the current flowing through the cable connecting the DC source to the inverter (and its DC link capacitors) is strictly constant.

Obviously, these two hypotheses are not strictly verified but can be good approximations of practical measurements, more particularly if the switching frequency is high enough to facilitate the filtering of high frequency harmonics (at AC and DC sides).

At high frequencies, all classical loads behave as inductances. Thus, the αβ current $\overrightarrow{I_{\alpha\beta}}$ is linked to the instantaneous voltage $\overrightarrow{V_{\alpha\beta}}$ provided to the load by the inverter:

$$\overrightarrow{I_{\alpha\beta}} = \frac{1}{L}\int \overrightarrow{V_{\alpha\beta}}.dt \tag{48}$$

As a consequence, currents ripples are directly linked to the harmonic flux or more precisely to $\vec{\Sigma}$ according to Equation (22).

Since $\vec{\Sigma}$ is proportional to $\Sigma_0 = \frac{v_{dc}}{2}\cdot\frac{T_{sw}}{2} = \frac{v_{dc}}{4F_{sw}}$, the higher F_{sw} is, the lower the AC currents ripples are.

5.1. GDPWM experiments

Qualitatively, this result is obvious but it must be verified in practice for a given test bench described in the Table 2.

However, even for a switching frequency equal to 10kHz that is applicable in our system, it is too high to evaluate distortions: no difference can be highlighted with the actual measurements. As a consequence, F_{sw} is fixed at 5kHz in the experimental results shown in Figure 16.

Table 2. Microhybrid vehicle VSI test bench

Test bench parameters	
Rated DC voltage	12V
DC cable + source resistance	10mΩ
DC cable + source inductance	1.5μH
Rated switching frequency	10kHz
MOSFET R_{DSON}	1.8mΩ
DC link electrolytic capacitors	4 x Evox Riga PEG225 / 4800μF – 25V
DC link polypropylene capacitors	6 x 10μF
AC load resistance (1 phase)	50mΩ
AC load inductance (1 phase)	408μH

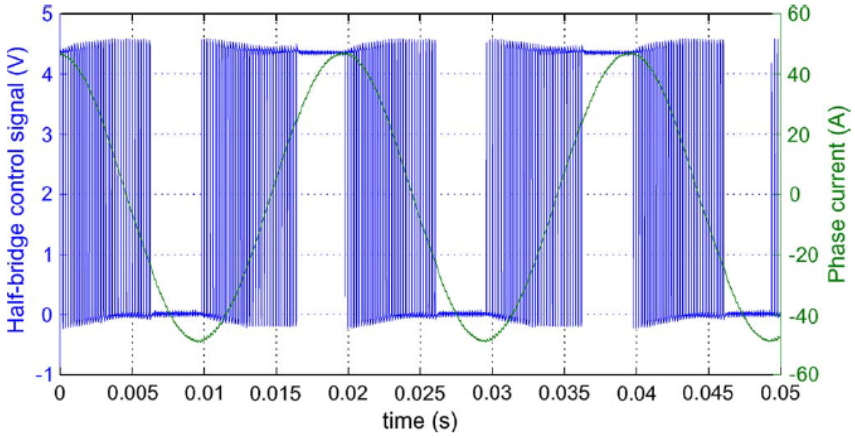

Figure 16. AC current waveform and switching function measured with the GDPWM

Global losses (including conduction and driver's losses) have been evaluated in the inverter at the same operating point for the SVPWM and GDPWM ($m = 1$, $\cos\varphi = 0.73$, $\hat{I} = 48$A) and the reduction observed is around 25%. The reduction of switching losses has been evaluated to 37%: it is lower than the predicted value (50% as it can be seen in Figure 12) but it validates the concept of this Generalized Discontinuous PWM.

Moreover, it must be noticed that the AC current (as it is shown in Figure 16) is practically sinusoidal: this hypothesis is well verified in the experimental test bench.

5.2. Uni-DCPWM experiments

In Figure 17, two experiment results are presented for two PWM strategies (SVPWM and Uni-DCPWM) tested in the same conditions. The switching frequency is fixed at 4kHz and the fundamental frequency is equal to 29Hz in both cases. The modulation index m is equal to 0.77 and $\varphi = 14°$. On one hand, this operating point lead to significant differences of the stress (RMS current) in DC link capacitors. On the other hand, it induces a high contrast between AC currents distorsions. Indeed, it can be seen that the distortion of the AC current is higher with the Uni-DCPWM strategy than with SVPWM. However, the switching frequency is very low because this distortion would be immeasurable at 10kHz (using current probes with a 1% accuracy).

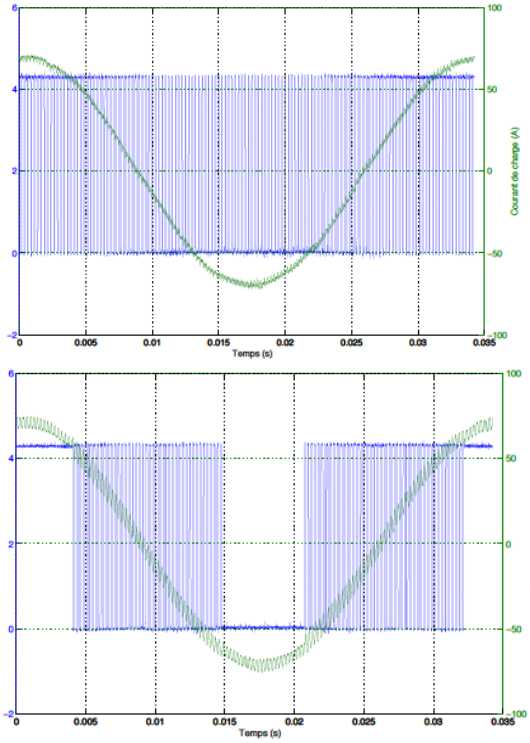

Figure 17. Comparison of AC currents for SVPWM (on the left) and Uni-DCPWM (on the right)

Even if the distortion is visible, it is quite moderate and the hypothesis of sinusoidal AC currents is still correctly verified in practice.

Results about switching losses with the Uni-DCPWM are similar to the ones obtained with the GDPWM and presented in the previous paragraph.

Finally, DC link capacitors current has been measured (using a Rogowski coil) and the reduction of its RMS value has been verified as it can be seen in Table 3.

The reduction of the RMS current in DC link capacitors is close to the predictions given with the theoretical cartography presented in Figure 14 since both operating points belong to the area with a reduction of 30-40% (ratio between 0.6 and 0.7)

Table 3. Comparison of SVPWM and Uni-DCPWM at two operating points

	Operating point : m = 0.77 and φ = 14°		
	SVPWM	Uni-DCPWM	Reduct. Ic
Ic (A RMS)	30,10	19,20	36,21%
THD	2,16%	6,21%	
	Operating point : m = 0.77 and φ=40°		
	SVPWM	Uni-DCPWM	Reduct. Ic
Ic (A RMS)	26,00	17,40	33,08%
THD	2,16%	6,21%	

6. Conclusions

In this paper, simple and powerful analytical techniques are utilized to illustrate and compare the performance characteristics of various PWM methods. The waveform quality comparisons indicate SVPWM at low modulation and DPWM methods at the high modulation range have superior performances. Concerning the switching losses, DPWM methods present the highest gain in term of their and comparisons between these various DPWM strategies indicate that DDT-GDPWM method have superior performance for every voltage-current phase shift. Moreover, a new PWM strategy aiming at reducing the RMS current value of DC link capacitor has been proposed. Analytical results show that this strategy, called Uni-DCPWM, effectively reduces RMS current value in comparison with SVPWM for high power factor load. This strategy also reduces the switching losses compared to SVPWM. Nevertheless, the output current quality is degraded: as a consequence, the acoustic noise or iron losses induced in the machine can be probably increased. However, since the harmonic flux is a synthetic criterion masking the spectrum distribution of harmonic current terms, it cannot be directly used to conclude about these possible issues. It is especially the case about iron losses that are linked to the amplitude and

frequencies of the harmonic currents (through the magnetic flux density, according the Bertotti's model). This uncertainty is due, on one hand to this lack of information about spectrum location and, on the other hand to the fact that these phenomena are strongly coupled to the design of the machine and/or to a lack of knowledge about behavior of materials or at least about parameters introduced in the corresponding laws of physics. The algorithm implementing this strategy on DSP boards is quite simple and can be applied in transient as well as steady state conditions on real time systems. As a consequence, this strategy is particularly adapted for automobile application. In can be concluded that every PWM strategy can only mitigate its impact on one or two aspects among three (downstream side: DC bus current ripple, Inverter side: Switching losses and upstream side: AC machine current waveform quality) but it is not possible to obtain an optimal behavior for all three aspects at once hence, a tradeoff is mandatory. The analytical tools presented in this paper give quantitative information about performances brought by different PWM strategies from input/output and internal losses viewpoints. Thus, on this basis, a system engineer can easily choose the adapted technique(s) for a given application.

Bibliography

Hava A. M. (1998). *Carrier-based PWM-VSI drives in the overmodulation region*, PhD Thesis, University of Wisconsin, Madison.

Hava A.M., Çetin N.O. (2011). A Generalized Scalar PWM Approach With Easy Implementation Features for Three-Phase, Three-Wire Voltage-Source Inverters, *IEEE Transactions on Power Electronics*, vol. 26, n° 5, p. 1385-1395.

Hobraiche J., Vilain J. P., Macret P., Patin N. (2009). A new PWM strategy to reduce the inverter input current ripples. *IEEE Trans. Power Electron.,* vol. 24, n° 1, p. 172-180.

Kolar J., Round S. D. (2006). Analytical Calculation of the RMS Current Stress on the DC Link Capacitor of Voltage-PWM Converter Systems. *IEE Proceedings, Electric Power Applications*, vol. 53, n° 4, p. 535-543.

Larminie J., Lowry J. (2012). *Electric Vehicle Technology Explained*, 2nd edition, Wiley.

Mukhtar A. (2010). *High Performance AC drives*, Springer, Berlin.

Narayanan G., Krishnamurthy H. K., Zhao D., Ayyanar R. (2006). Advanced bus-clamping PWM techniques based on space vector approach. *IEEE Transactions on Power Electronics*, vol. 21, n° 4, p. 974-984.

Nguyen T.D., Patin N., Friedrich G. (2010). Analyse des sollicitations sur les condensateurs de filtrage du bus continu d'onduleur pour applications embarquées en fonction de la stratégie de modulation. *Electronique de Puissance du Futur EPF'10*, Saint-Nazaire, France, 30 juin-2 juillet.

Dahono P.A., Sato Y., Kataoka T. (1996). Analysis and minimization of ripple components of input current and voltage of PWM inverters. *IEEE Transactions on Industry Applications*, vol. 32, n° 4, p. 945-950.

Nguyen T. D., Hobraiche J., Patin N., Friedrich G., Vilain J.-P. (2011a). A Direct Digital technique implementation of general discontinuous pulse width modulation strategy. *IEEE Transactions on Industrial Electronics*, vol. 58, n° 9, p. 4445-4454, Sept.

Nguyen T. D., Patin N., Friedrich G. (2011b). PWM Strategy dedicated to the reduction of DC bus capacitor stress in embedded three phase inverter. *IEEE Vehicle Power and Propulsion Conference VPPC'11*, Chicago, USA, 6-9 Sept.

Obegard B., Stulz C. A., Steimer P. K. (1994). Industrial application of variable speed drive system for high speed in megawatt power range. *in Proc. IEEE IAS Annual Meeting*, Denver, USA, 2-6 Oct.

Rudnicki T., Czerwinski R., Frechowicz A. (2011). Permanent magnet synchronous motor control driver. *in Proc. IEEE Mixed Design of Integrated Circuits and Systems MIXDES'11*, Gliwice, Poland, 16-18 June.

Santisteban J. A., Stephan R. M. (2001). Vector control methods for induction machines: An overview. *IEEE Transactions on Education*, vol. 44, n° 2, p. 170-175.

Trzynadlowski A. M. (1996). An overview of modern PWM techniques for three-phase, voltage-controlled, voltage-source inverters. *in Proc. IEEE International Symposium on Industrial Electronics ISIE'96*, Warsaw, Poland, 17-20 June.

Received: 30 July 2014
Accepted: 2 June 2015