
A new AC – AC converter with buck and boost options

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ABSTRACT. This paper proposes a novel AC-AC converter capable of operating in non-inverting and inverting buck boost modes. The projected AC-AC converter uses six IGBTs with reverse blocking capability, two capacitors and one inductor. The main advantage of this AC-AC converter is that it is free from shoot through problem even when all the six IGBTs are in ON condition. Hence dead time between two pulse width modulation signals is not necessary, which results in load voltage waveform with very less Total Harmonic Distortion (THD). Furthermore elimination of dead time, eradicates the commutation problem even in the absence of hefty snubbers or with soft commutation methods. The switching losses of the proposed converter are very less since only two devices are switched at high frequency that too only in a half cycle. The remaining switches are switched at fundamental frequency, which in turn increases the efficiency of the converter. The proposed converter is a suitable candidature in dynamic voltage restorer and single phase solid state transformer applications.

RÉSUMÉ. Cet article propose un nouveau convertisseur CA - CA capable de fonctionner en modes Buck-Boost non inversé et inversé. Le convertisseur CA - CA projeté utilise le transistor bipolaire à grille isolée (IGBT, de l'anglais Insulated Gate Bipolar Transistor) avec la capacité de blocage inverse, deux condensateurs et un inducteur. Le principal avantage de ce convertisseur CA - CA réside dans le fait qu'il ne présente aucun problème de déclenchement, même lorsque les six-IGBT sont activés. Par conséquent, le temps mort entre les deux signaux modulés en largeur d'impulsion n'est pas requis, ce qui entraîne un taux très bas de distorsion harmonique (THD, de l'anglais total harmonic distortion) de la forme d'onde de la tension de charge. De plus, le temps mort peut être éliminé et le problème de commutation peut être éliminé même sans un grand nombre d'amortisseurs ou une méthode de commutation douce. Les pertes de commutation du convertisseur proposé sont très faibles car seuls deux appareils sont commutés à haute fréquence, ce qui ne représente qu'un demi-cycle. Les autres commutateurs sont commutés à la fréquence fondamentale, ce qui augmente

l'efficacité du convertisseur. Le convertisseur proposé convient parfaitement aux applications de restauration dynamique de la tension et de transformateurs à à l'état solide monophasé

KEYWORDS: commutation, AC-AC converter, buck-boost modes, inverting and non-inverting.

MOTS-CLÉS: commutation, convertisseur CA - CA, modes Buck-Boost, inversé et non-inversé.

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1. Introduction

Conventional thyristor-based ac-ac converters are used in industries for the past few decades, which uses either integral cycle control or phase angle control to obtain the required output voltage across the loads. But the major drawbacks of the conventional ac voltage controllers are large THD in the input current, less efficiency and low input power factor, which restricts their applications as described by Nguyen *et al.* (2010). In certain applications where both variable voltage and frequency is demanded, indirect ac-ac converters (i.e.AC-DC-AC Converters) with DC link or direct ac-ac converters (i.e. Matrix converters) are used because of their improved efficiency and power factor as shown in Liu *et al.* (2009). In addition, their filter size requirements are also less when compared to ac voltage controller. On the other hand, applications which demands only voltage control, Pulse Width Modulation (PWM) ac voltage regulators are used because of their compact size and low cost as described by Jacobina *et al.* (2006). These PWM ac voltage regulators shown in Alemi *et al.* (2015), Ecklebe *et al.* (2009) and Cardenas *et al.* (2012) are modified versions of the DC-DC converters, where all the unidirectional devices are changed into bi-directional switches. On the contrary, all they type of PWM ac voltage regulators have their own boundaries; for example, boost type PWM ac voltage regulator can only boost up the input voltage whereas on other hand the buck type PWM ac voltage regulator can only step down the input voltage. There are other versions like buck boost and cuk regulators where it is possible to increase the load voltage above the level of input voltage and also decrease it below the input voltage. But the main restriction of the buck-boost and cuk type topology is that the load voltage phase is reversed with respect to the input voltage as demonstrated in Metidji *et al.* (2013), Xia *et al.* (2014) and Ge *et al.* (2014). Additionally, in both these topologies the voltage stresses across the switches are much higher which limit their applications.

Furthermore, in buck boost topology, both the input and output current are discontinuous in nature which restricts its usage. Where as in the case of cuk regulator the input and output currents are continuous in nature, because of its additional passive components, but this increases its cost and size of the converter. Quasi Z source (qZS) ac-ac converters are also proposed in the literature, which operates in the buck and buck boost modes. During the operation of qZS in buck mode the phase of the load voltage reverses with respect to the input voltage, further during the shoot through state of the switches enormous amount of current flow through the device which limits their use. Flying capacitor based buck type multilevel inverter is proposed in Peng *et al.* (2003), Sarnago *et al.* (2014) and Kim *et al.* (1998), which improves the load voltage profile in terms of its total harmonic distortion (THD) and also reduces the voltage stress on the switches. But in this

topology in order to maintain flying capacitor voltages at a constant value an RLC network is added which increases its size and complexity as in Vicuna *et al.* (2009), Moghe *et al.* (2015) and Li and Zhong (2012).

All these topologies have commutation problem. Ideally complementary devices do not have any overlap or dead-time, but practically there is a very small overlap between the gating signals of the complementary switches as in Fang *et al.* (2005), Nguyen *et al.* (2012) and Banaei *et al.* (2015). During this overlap, either a short circuit of voltage source occurs or two capacitors of different voltages come in parallel to each other. This results in large current spikes across the devices which lead to damage them. To evade this damage to the switching devices a small dead time is added to the gating signals to avoid overlap, further hefty and lossy RC snubbers are used to protect the devices from voltage or current spikes as in Tang *et al.* (2007) and He, Duan and Peng. (2013). Gagliano and Nocera (2017). proposes the effective way for electric energy storage in residential applications.

To solve the above drawbacks of existing and conventional ac-ac converters, a direct ac-ac converter is proposed which combines the functions of inverting buck-boost converters and non-inverting buck-boost converters in a single topology.

2. Proposed convertor topology

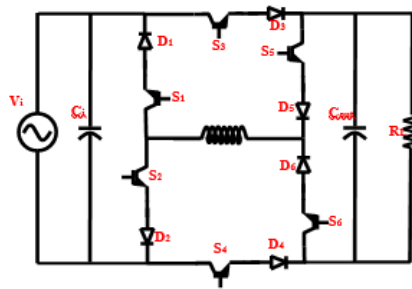


Figure 1. Proposed AC-AC converter

Figure 1 shows the proposed AC-AC converter topology which has six power electronic devices, six diodes, two filter capacitors and one inductor. The proposed AC-AC converter topologies is capable of operating as inverting buck and boost converter as well as non-inverting buck and boost converter. The main application of the proposed AC-AC converter topology is that it can be used as Dynamic Voltage Restorer (DVR), where the non-inverting buck and boost converters can be operated to compensate voltage dips and the inverting buck and boost converters can be operated to compensate the voltage swells. Further the main advantage of the proposed converter topology is that it is free from commutation problem.

2.1. Study of Commutation Strategy in the projected converter

In the proposed converter topology switches S_1 and S_2 are complementary to each other. Similarly switches S_3 and S_4 , S_5 and S_6 are complementary to each other. Generally if there is no dead band between complementary switches which may lead to short circuit at the input side or at the output side based on the operation. But here in the projected converter topology, when S_1 & S_2 are turned on at the same instant of time as shown in figure 2(a), diode D_1 will not allow the current to flow through the devices S_1 & S_2 which prevents the problem of short circuit the input capacitance. Hence switches S_1 and S_2 are commutation free switches. Further as shown in figure 2(b) the switches S_3 and S_4 can be turned on at the same instant of time, during this mode of operation diode D_4 prevents current flowing through the devices S_3 and S_4 , which eliminates the problem of short circuit the output filter capacitance. Similarly as shown in figure 2(c) when switches S_5 and S_6 are turned on at the same instant of time, diode D_6 eliminates the short circuit problem of the load side capacitance. Hence from figures 2(a), 2(b) and 2(c) the proposed AC-AC converter topology is free from the commutation problem.

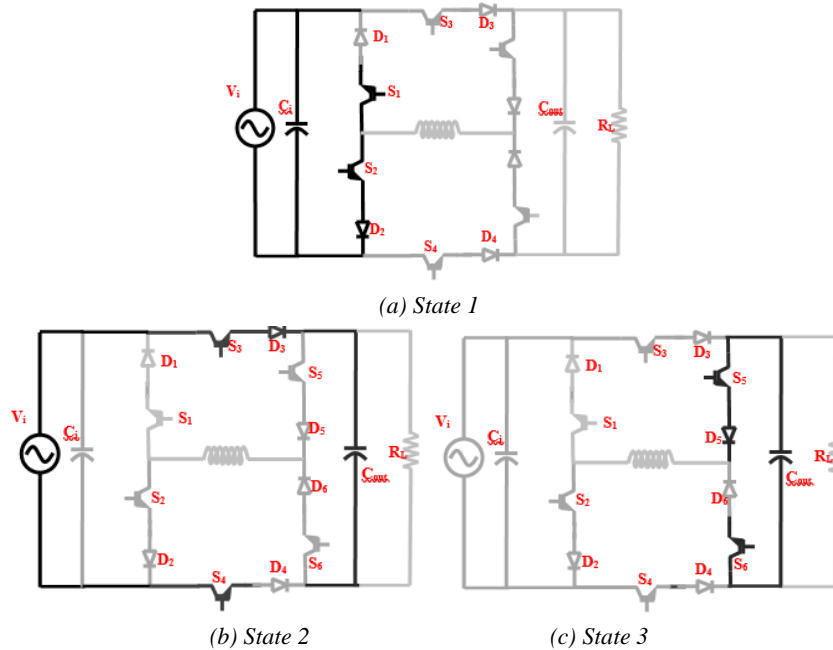


Figure 2. Possible shoot through

2.2. Non-inverting mode of operation

The proposed inverter can operate in both non-inverting and inverting modes of operation. Further in each of these modes the converter is capable of operating as

buck and boost converter. In this section the operation of the proposed converter in non-inverting mode is dealt in detail.

2.2.1. Proposed topology operating as buck converter

The proposed topology has four modes of operation as indicated in Table (1). Figure 3(a) shows the proposed topology operating as buck converter in non-inverting mode when the input voltage is greater than 0 during duty cycle interval. Similarly figure 3(b) shows the operation of the proposed topology operating as buck converter in non-inverting mode when the input voltage is greater than 0 during OFF duty cycle interval. Furthermore figure 4(a) and 4(b) shows the operation of the proposed converter as buck converter in non-inverting mode when the input voltage is greater than 0 during duty cycle and OFF duty cycle interval respectively. Figure 7(a) shows the key operating waveforms of the proposed converter topology in buck mode.

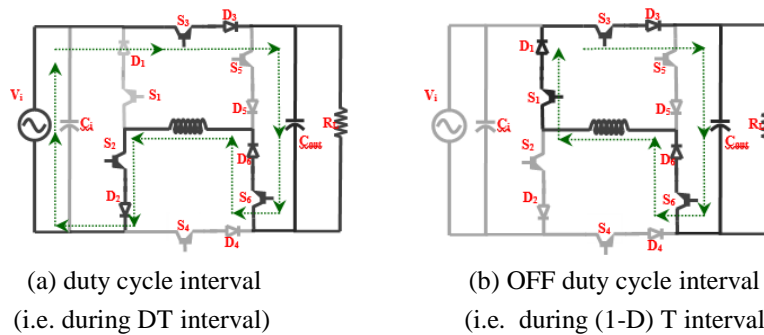


Figure 3. Buck operation - non-inverting mode when input voltage > 0 during

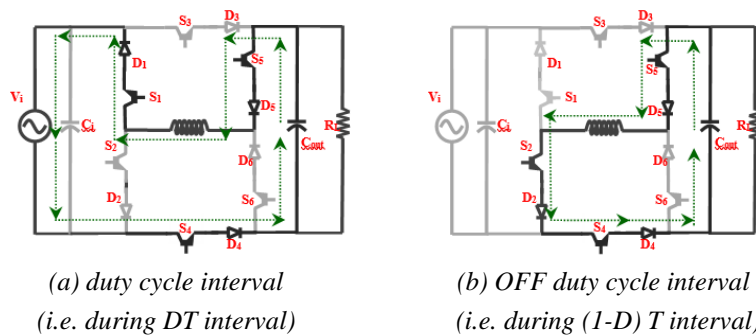


Figure 4. Buck operation – non-inverting mode when input voltage < 0 during

For $V_{in} < 0$, switches S_2, S_4, S_5 are always turn on while switches S_3, S_6 are always turn off, and S_1 becomes high frequency switch. The operation for $V_{in} < 0$ is same as

explained for $V_{in} > 0$, with only difference is that now the switch S_1 performs same as S_2 (for $V_{in} > 0$), and vice versa. The equivalent circuits during this negative half-cycle are shown in Figure. 4(a) and (b).

Table 1. Switching table for non-inverting buck mode

Input Voltage	S_1	S_2	S_3	S_4	S_5	S_6	Reference
$V_{in} > 0$	OFF	ON	ON	OFF	OFF	ON	Figure 3(a)
	ON	OFF	ON	OFF	OFF	ON	Figure 3(b)
$V_{in} < 0$	ON	OFF	OFF	ON	ON	OFF	Figure 4(a)
	OFF	ON	OFF	ON	ON	OFF	Figure 4(b)

2.2.2. Proposed topology operating as boost converter

The switching table of proposed topology operating as boost converter in non-inverting mode is given in Table (2). Figure 5(a) shows the operation of the proposed topology operating as a boost converter in non-inverting mode. From figure 5(a) switches S_2 , S_3 and S_5 are in ON condition when the input voltage V_{in} is greater than 0 (i.e. during the positive half cycle of the input voltage). Immediately after this operation switch S_5 is turned off and S_6 is turned on as shown in Figure 5(b). The switching sequence of the proposed converter during non-inverting boost mode operation and key waveforms are shown in Figure. 7(a). For $V_{in} > 0$, switches S_2 , S_3 , S_6 are always turn on and S_1 , S_4 are always turn off, while switch S_5 is switched at high frequency.

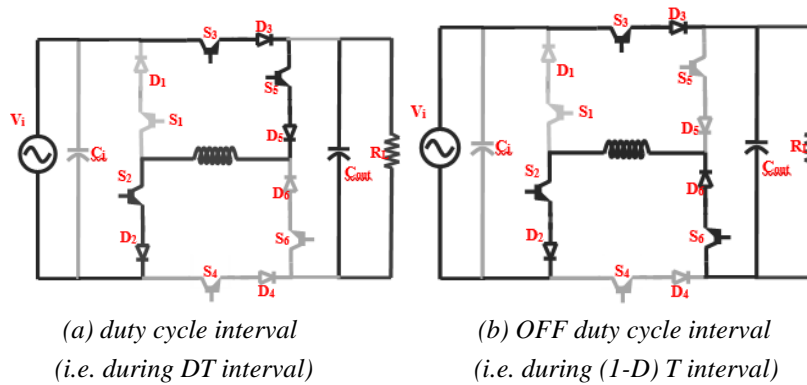


Figure 5. Boost operation – non-inverting mode when input voltage > 0 during

Figure 5 and figure 6 shows the equivalent circuits of the proposed converter for $V_{in} > 0$. The circuit shown in Figure. 5(a) is during DT interval in which switch S_5 is turned on and the input energy is stored in inductor L . The switch S_6 is also turned on; however, its external series diode becomes reverse biased because of inverse

output voltage V_0 across it. Therefore, no current flows through switch S_6 during this interval, as shown in Figure. 6(b).

Table 2. Switching table for Non-Inverting buck mode

Input Voltage	S_1	S_2	S_3	S_4	S_5	S_6	Reference
$V_{in} > 0$	OFF	ON	ON	OFF	ON	OFF	Figure 5(a)
	OFF	ON	ON	OFF	OFF	ON	Figure 5(b)
$V_{in} < 0$	ON	OFF	OFF	ON	OFF	ON	Figure 6(a)
	ON	OFF	OFF	ON	ON	OFF	Figure 6(b)

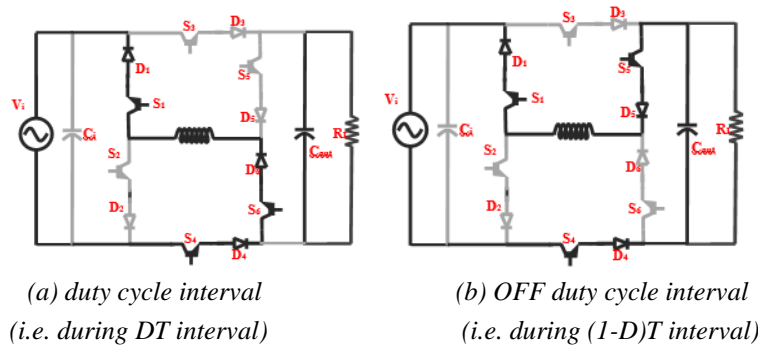


Figure 6. Boost operation - non-inverting mode when input voltage < 0 during

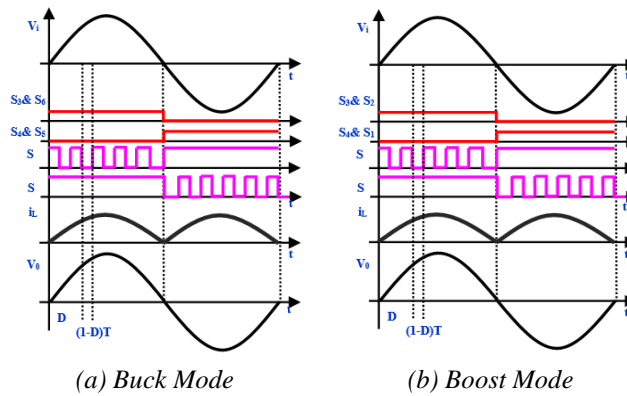


Figure 7. Non inverting modes of operation key waveforms

For $V_{in} < 0$, switches S_1, S_4, S_5 are always turn on while switches S_2, S_3 are always

turn off, and S_6 becomes high frequency switch. The operation for $V_{in} < 0$ is the same as explained for $V_{in} > 0$, with only difference is that now the operation of switch S_6 is same as that of S_5 (for $V_{in} > 0$), and vice versa. The equivalent circuits during this half-cycle are shown in Figure. 7(a) and (b).

2.3. Inverting mode of operation

The switching sequence of the proposed converter during inverting buck–boost mode operation and key waveforms are shown in Figure. 8. For $V_{in} > 0$, switches S_2, S_4, S_5 are always turn on and S_1, S_6 are always turn off, while switch S_3 is switched at high frequency. Figure 9 shows the equivalent circuits of the proposed converter for $V_{in} > 0$. The circuit shown in Figure 9(a) is during DT interval in which switch S_3 is turned on and the input energy is stored in inductor L . The switch S_4 is also turned on; however, its external series diode becomes reverse biased because of inverse voltage ($V_{in} + V_o$) across it. Therefore, no current flows through switch S_4 during this interval, as shown in Figure 9(a).

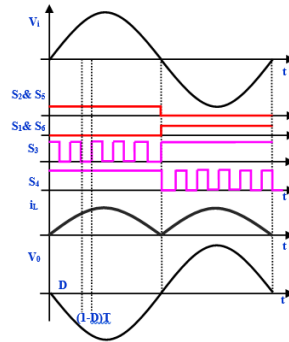


Figure 8. Inverting mode of operation key waveforms in buck-boost mode

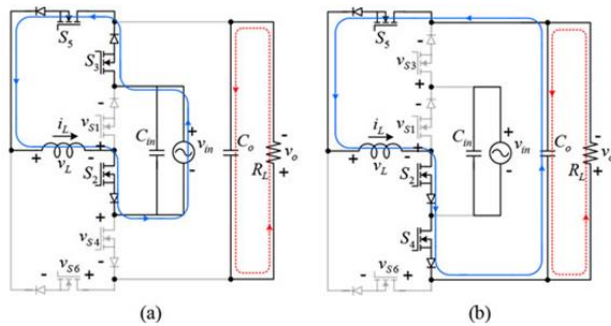


Figure 9 Boost operation - inverting mode when $V_{in} > 0$ (a) during DT interval (b) $(1-D) T$ interval

For $V_{in} < 0$, switches S_1, S_3, S_6 are always turn on while switches S_2, S_5 are always turn off, and S_4 becomes high frequency switch. The operation for $V_{in} < 0$ is the same as explained for $v_{in} > 0$, with only difference is that now the switch S_4 acts the same as S_3 (for $V_{in} > 0$), and vice versa. The equivalent circuits during this half-cycle are shown in Figure. 10(a) and (b). The details of switching strategy are shown in table (3).

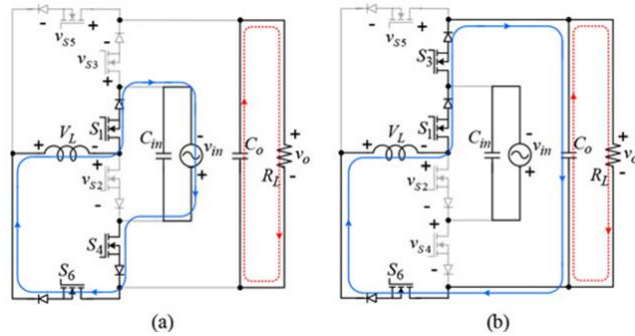


Figure 10. Boost operation - inverting mode when $V_{in} < 0$ (a) during DT interval (b) $(1-D)T$ interval

3. Simulation results

To validate the proposed AC-AC converter, a simulation model is developed in MATLAB/SIMULINK environment and the simulation results are presented in this section. The various simulation parameters used in this study are shown in Table (3). The switching signals of all the switches in non-inverting mode for Buck action is shown in Figure 11. From Figure 11 it can be seen that two switches operate at fundamental frequency and remaining four switches operate at high frequency.

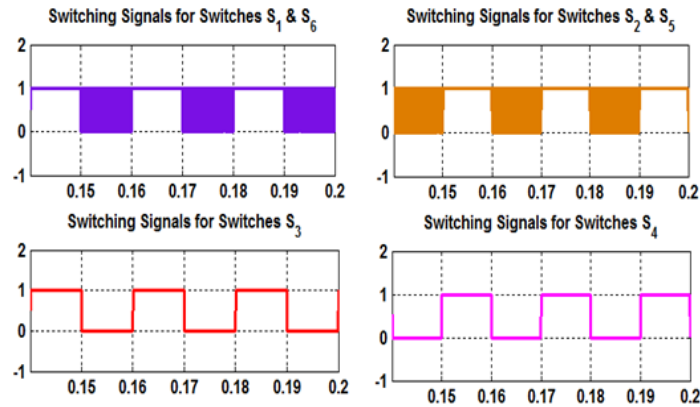


Figure 11. Switching signals of Non-Inverting mode buck AC-AC converter

Table 3. Simulation parameters

Switching Frequency	25kHz
Peak input Voltage	135V
Frequency	50Hz
Load Resistance	100 ohms
Input Capacitance	1.5 micro farads
Output Capacitance	4.5 micro farads
Solver type	Ode23s (stiff/Mod. Rosen Brock)
Max step size	1e-6
Min step size	1e-7

Figure 12 shown the input voltage, load voltage and load current of the proposed ac-ac converter operating in non-inverting mode (in buck mode) for duty cycle of 0.4. It is evident from Figure 12 that the load voltage is below 100-volt peak whereas the input voltage is 135V peak. It should be noted that when the duty cycle is between 0 to 0.5 it operates in buck mode, whereas for the proposed converter to be operated in boost mode the duty cycle of the converter should be more that 0.5 and less than 1.

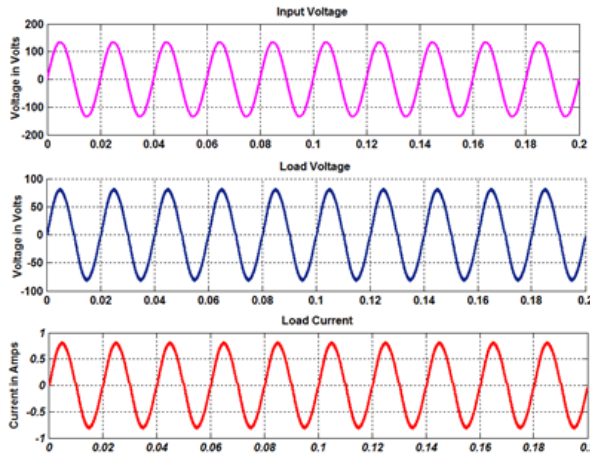


Figure 12. Input voltage, load voltage and load current for Non-inverting mode in buck action

Figure 13 shows the input voltage, load voltage and load current waveform of the proposed converter when operating in boost non-inverting mode. The Figure 13 corresponds to the duty cycle of 0.8. It is evident from the Figure 13 that the load

voltage is greater than the input voltage i.e. the load voltage has a peak value of 500 volts whereas the peak value of the input voltage is 135 volts. Hence the proposed inverter operates much conveniently in the boost mode. Further the load current is also boosted up as shown in Figure 13.

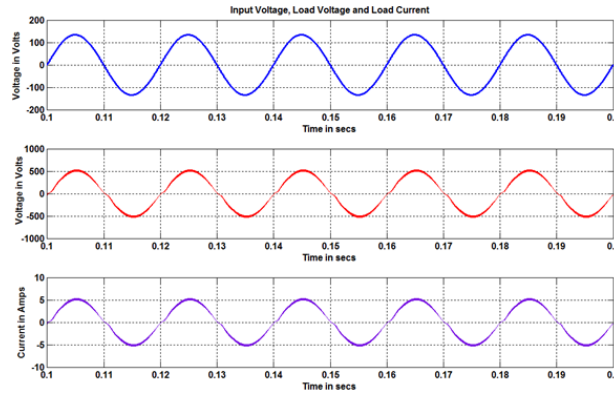


Figure 13. Input voltage, load voltage and load current for Non-inverting mode in boost action

Figure 14 shows the switching signals of all the six switches when the converter is operating in inverting buck mode. From Figure 14 it is evident that switches S_1, S_2, S_5 and S_6 operate in low fundamental frequency whereas switches S_3 and S_4 operate at high (i.e. carrier) frequency. The above switching pattern is used to drive the switches for inverting buck mode of operation. Figure 15 shows the input voltage, load voltage and load current of the proposed ac-ac converter when it is operated in inverting buck mode. From Figure 15 it is evident that there is a phase shift of 180 degrees between the input voltage and load voltage, which means that the proposed converter is operating in inverting mode. Further the load voltage peak value is also less than that of the input voltage, which means that the converter is operating in buck mode.

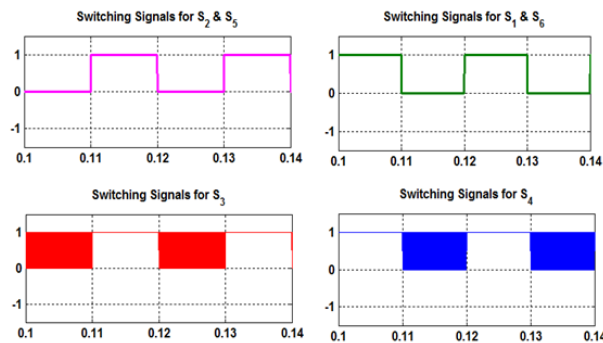


Figure 14. Switching Signals for the proposed converter for inverting mode

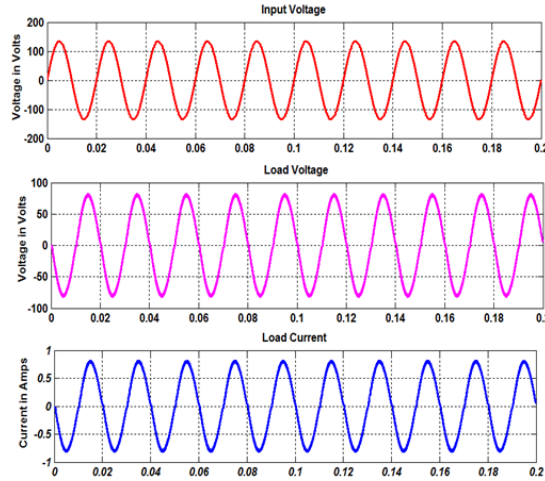


Figure 15. Input voltage, load voltage and load current for inverting mode in buck action

Figure 16 shows the input voltage, load voltage and load current waveform of the proposed ac-ac converter operating in inverting boost mode. From Figure 15 it is evident that the load voltage has a phase shift of 180 degrees with respect to the input voltage and also the load voltage magnitude is greater than that of the input voltage magnitude. Thus the proposed ac-ac converter is capable of operating in inverting buck as well as boost modes.

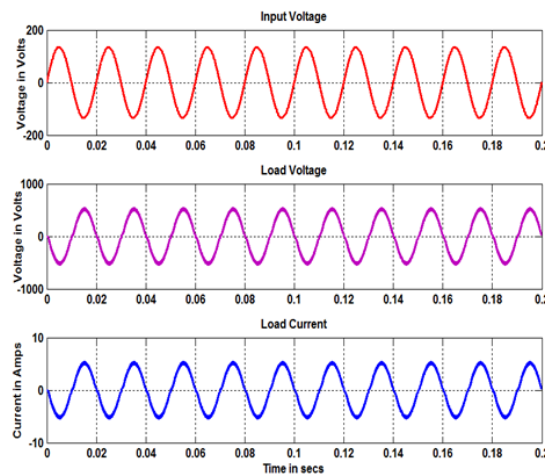


Figure 16. Input voltage, load voltage and load current for inverting mode in boost action

4. Conclusions

In this paper, a single-phase PWM ac–ac converter has been proposed which combined the operation of non-inverting buck and boost converters and inverting buck–boost converter in one topology. The proposed converter uses six unidirectional current flowing bidirectional voltage blocking switches, two capacitors, and one inductor. The proposed converter has no shoot-through problem even when all switches are turned on simultaneously, and therefore, can eliminate PWM dead-times to produce high quality output voltage. Furthermore, the proposed converter can solve commutation problem without using bulky and lossy RC snubber or dedicated soft commutation strategy. In the proposed converter, only two switches are switched at high frequency during each half-cycle, which reduces the switching losses. Moreover, since body diode of switches never conducts the proposed converter can use power IGBTs, which benefits in low switching loss, resistive conduction voltage drops, fast switching speed, etc.

The proposed converter can operate in non-inverting buck and boost modes to replace the inverting buck–boost ac–ac converter with following benefits; decreased switch voltage stresses, inductor current and current ripple, increased reliability because of no commutation problem, and no need of PWM dead-times. In its application as DVR, the inverting buck–boost mode of the proposed converter can also be utilized along with non-inverting buck and boost modes, to compensate both voltage sags and swells. A detailed analysis of the proposed converter has been presented.

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