IIETA International Information and Engineering Technology Association
Advancing the World of Information and Engineering

Traitement du Signal
Vol. 37, No. 6, December, 2020, pp. 939-953
Journal homepage: http://iieta.org/journals/ts

Design and Realization of a Hyperchaotic Memristive System for Communication System on FPGA

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https://doi.org/10.18280/ts.370607

Received: 8 July 2020
Accepted: 13 December 2020

Keywords:
chaos, circuit implementation, communication systems, FPGA, memristor, optimization

ABSTRACT

In this study, a memristor based hyperchaotic circuit is presented and implemented for communication systems on FPGA platform. Four dimensional hyperchaotic system, which contains active flux controlled memristor is designed by using a smooth continuous nonlinearity. Dynamical characteristics of designed hyperchaotic circuit are examined such as equilibrium points, chaotic attractors, Lyapunov exponents and bifurcation diagram. Furthermore, an electronic circuit model of hyperchaotic system has been modeled and results are submitted. Chaotic circuits are used in communication systems especially in secure communication due to their sensitive dependence on the initial conditions, not periodic, and having a spread spectrum. By using nonlinearity of memristor, the signals obtained from memristor based hyperchaotic system have been realized to analog and digital communication schemes on FPGA platform, which is suitable for re-programmable and reconfigurable systems. The success of memristor based hyperchaotic circuit with FPGA based communication is demonstrated by both simulation and experimental results.

1. INTRODUCTION

After Leon O. Chua introduced the memristor in 1971 and the HP team submitted the first physical memristor to the literature, studies on the memristor have been rapidly increasing [1, 2]. The memristor described by flux and charge is considered to be the fourth basic circuit element [1]. The memristor has brought a completely new field of development in various interdisciplinary fields. In particular, many researchers have begun to benefit from memristor based application circuits due to the unique characteristics of memristor over the last few years [3-6].

In order to construct various new memristor based chaotic circuits, the memristor element is integrated into some existing linear or nonlinear electronic circuits. The use of chaotic dynamics is important in many areas and there is increasing interest particularly in engineering applications that aim to create effective chaos through simple physical systems such as electronic circuits [7-9]. Due to the nonlinear property of the memristor element [1], a chaotic signal can easily be obtained from chaotic circuits based on memristor, which increases the interest of researchers to use memristor in the design of chaotic circuits [10-13]. However, due to technical disadvantages and the high costs of manufacturing nanoscale devices, memristor design is realized with the help of emulators. Chaotic signals which are used as a carrier in spreading spectrum communication systems are obtained with simple circuits and it is easy to do as hardware and provides an advantage in information security because chaos contains non-periodic signals. As a model for practical application, it is much more important to produce a hyperchaotic signal with more complex dynamics when comparing with chaotic signals. It is more advantageous than other systems because it has a complex structure, higher unpredictability, and more random features. The designed hyperchaotic system can be used to enhance the reliability of the secure communication system. In this respect, new hyperchaotic circuits are crucial [14]. After the discovery of the hyperchaotic Rössler system presented by Rössler, many hyperchaotic systems have been developed and presented to the literature [15]. It is used in many areas of nonlinear sciences such as secure communication, neural network, image processing, laser physics, and nonlinear circuits [16-19].

Chaotic and hyperchaotic systems are widely used for realizing analog and digital communication modulation techniques. A study by Pecora-Carroll in 1990, which showed that chaotic communication systems can be synchronized, paved the way for the use of chaotic signals in spread spectrum communication systems [20]. Chaos based analog communication systems are well affected by noise in real-time applications, despite their good performance in noiseless environments. Chaos based digital communication systems are less affected by noise than analog communication and therefore digital modulation techniques are preferred [21]. Many studies have been performed in the literature by using digital modulation techniques. Chaos shift keying (CSK) [22], chaotic on-off keying (COOK) [23] and differential chaos shift keying DCSK [24] show digital modulation techniques.

Chaotic circuit models are diversified to increase and expand chaos based engineering applications. Chaotic applications designed on an FPGA (Field Programmable Gate Array) environment have more flexible structures in which parameter changes of a chaotic system can be made easily. By changing the parameters of the designed system, the dynamic

behavior of the system can be easily changed. Therefore, the realization of chaotic signal generators based on an integrated digital platform such as FPGA enables us to take advantage of these features [25]. Because of their high speed and capacity, FPGA chips have an important potential to improve information security capacity, especially in applications such as cryptology and secure communications requiring high performance and processing power [26]. Studies on digital FPGA based modeling of chaotic oscillators are of great importance in the literature [26-28]. Memristor based applications have also been studied on FPGA platform [29, 30].

In this study, a hyperchaotic circuit based on memristor is designed. Especially considering the importance of newly designed hyperchaotic circuits in communication systems, dynamic analysis of the designed system is presented and real-time implementation is performed. For chaotic communication and especially secure communication system, the signals obtained from this hyperchaotic circuit are modeled on the FPGA platform in communication systems. FPGA has made it possible to complete the work in the chaos area faster and to make it easier to develop new methods. The communication application of the designed chaotic systems is synthesized by using Xilinx Spartan-3E family XC3S500E board. Synchronization of hyperchaotic circuits obtained from the designed system is very important for a good signal transmission in the analog communication system. In order to solve the synchronization problem of this model, system gains are obtained by using a PID control scheme based on the Firefly algorithm. Using the algorithm, optimal control gains are achieved in PID controller gains. Moreover, as an application, the proposed system is implemented on the FPGA platform to a chaotic communication system. Likewise, COOK modulation, which is one of the digital communication methods, is realized in the FPGA platform and presented to the literature. BER performances of FPGA applications of memristor based hyperchaotic generators are submitted. The success of memristor based hyperchaotic circuit with FPGA based communication is demonstrated by both simulation and experimental results.

This paper is arranged as follows. First, the model of the hyperchaotic circuit based on memristor is designed in Sect. 2. Then, in order to examine dynamical characteristics; the equilibrium points, Lyapunov exponents, and bifurcation diagrams are given in Sect. 3. Next, Chaotic communication schemes for analog and digital modulation systems are modeled for memristor based hyperchaotic circuit in Sect. 4. After that, applications of these modulations systems on FPGA are given in Sect. 5. Finally, the results are submitted in Sect. 6. Block diagram of paper organized is given in Figure 1.

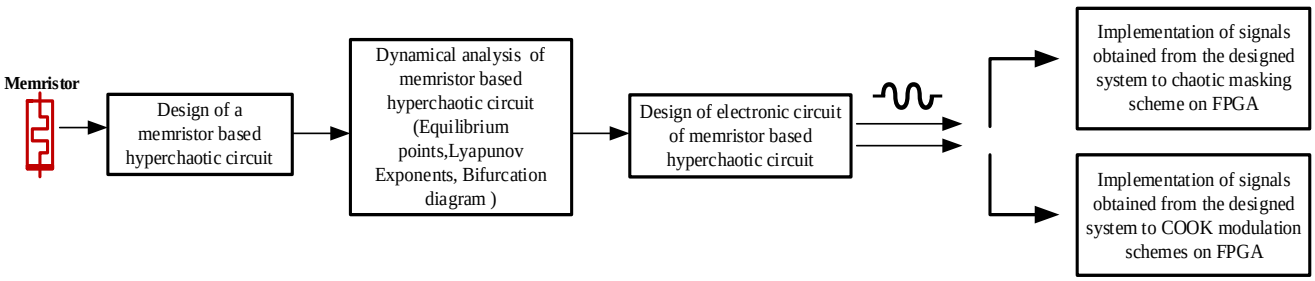


Figure 1. Block diagram of paper organized

2. MEMRISTOR BASED CHAOTIC CIRCUT

The memristor represents a nonlinear relationship between *charge* q and *flux* φ. A characteristic memristor emulator is designed to perform a voltage controlled memristor as shown in Figure 2 and memristor based hyperchaotic circuit is modeled by using memristor emulator with a smooth continuous nonlinearity [10, 31-33].

The used memristor emulator's fundamental relationship for designing memristor based hyperchaotic circuit can be given by Cam and Sedef [31] and Sahin et al. [33]. If the circuit in Figure 2 is analyzed by using the definition relations of circuit elements, the voltage on the C_M capacitor can be expressed as $v_{CM} = q_{CM}/C_M$. In addition, provided that q_0 is the initial value, it is expressed as $q_{CM}(t) = \int_0^t i_{CM}(\tau)\, d\tau + q_0$. If this equation is expressed in terms of voltage, it will be ($i_{CM} = -\frac{v_M}{R_1}$), $q_{CM}(t) = -\frac{1}{R_1}\int_0^t v_M(\tau)\, d\tau + q_0$. The memristor is developed for cubic form and schematic of memristor based hyperchaotic shown in Figure 3, the form emulator equations are given following, (for more details, the study [33] can be examined).

$$M(t) = \pm \frac{R_1 R_2}{k^2 R_M v_{CM}(t)^2} \tag{1}$$

$$i_M = \frac{k^2 R_M v_M(t) v_{CM}(t)^2}{R_1 R_2} \tag{2}$$

$$\dot{v}_{CM}(t) = -\frac{1}{R_1 C_M} v_M(t) \tag{3}$$

When the system is designed by using Kirchhoff laws, the state equations of the system are as follows:

$$\begin{aligned} \dot{v}_{C1}(t) &= \frac{i_L(t)}{C_1} - \frac{i_M(t)}{C_1} \\ \dot{v}_{C2}(t) &= \frac{v_{C2}(t)}{RC_2} - \frac{i_L(t)}{C_2} \\ \dot{i}_L(t) &= \frac{v_{C2}(t)}{L} - \frac{v_{C1}(t)}{L} \\ \dot{v}_{CM}(t) &= -\frac{1}{R_1 C_M} v_{C1}(t) \end{aligned} \tag{4}$$

When Eq. (4) is arranged by using Eqns. (2) and (3) of

memristor emulator, in the state equations, x, y, z, u are the states and a, b, c, d, n, m_0 and m_1 are parameters. When Eq. (4) is redefined according to $V_{C1} = x, V_{C2} = y, i_L = z, V_{CM} = u$, $a = \frac{1}{C_1}, b = \frac{1}{C_2}, c = \frac{1}{L}, d = \frac{1}{R}, n = -1/R_1 C_M$:

$$\begin{aligned} \dot{x} &= az - ax(m_0 + m_1 u^2) \\ \dot{y} &= bdy - bz \\ \dot{z} &= cy - cx \\ \dot{u} &= nx \end{aligned} \tag{5}$$

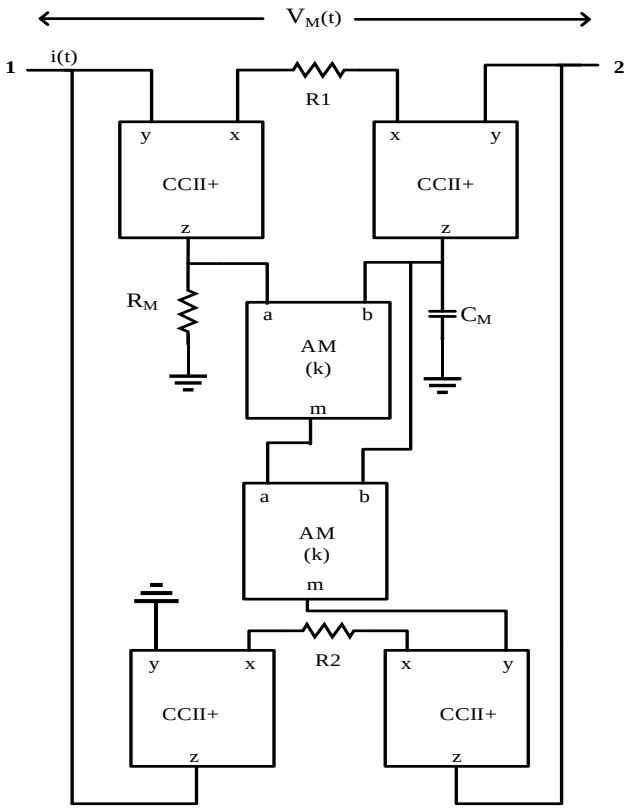


Figure 2. Design of memristor emulator circuit

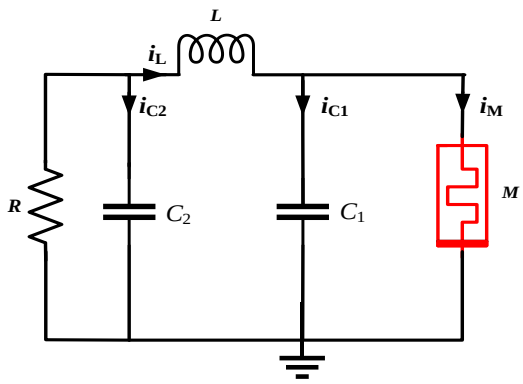


Figure 3. Schematic of memristor based hyperchaotic circuit

3. NUMERICALLY SIMULATED DYNAMICAL ANALYSIS

The basic dynamics of the hyperchaotic system are analyzed in this section. Some of the analysis methods: equilibrium points, phase portraits, Lyapunov exponents and bifurcation diagrams of the system are examined and results are given about the designed system. Numerical analysis are performed in MATLAB to confirm the analytical estimates obtained in the previous section.

3.1 Chaotic attractor

The attractors are a set of points or dots showing possible stable states of a system in the phase space. MATLAB Runge Kutta "*ode.m*" algorithm is utilized to draw phase portraits. By using Eq. (5), results of this system are obtained. Chaotic attractors are given in Figure 4 when parameters of a=7, b=1, c=2.5, d=1, m_0=-1.2, m_1=1 and n=-6, initial conditions $x(0)$=0.1, $y(0)$=0, $z(0)$=0 and $u(0)$=0 are fixed these values. Three dimensional graphs of attractors of memristor based hyperchaotic circuit is shown Figure 5.

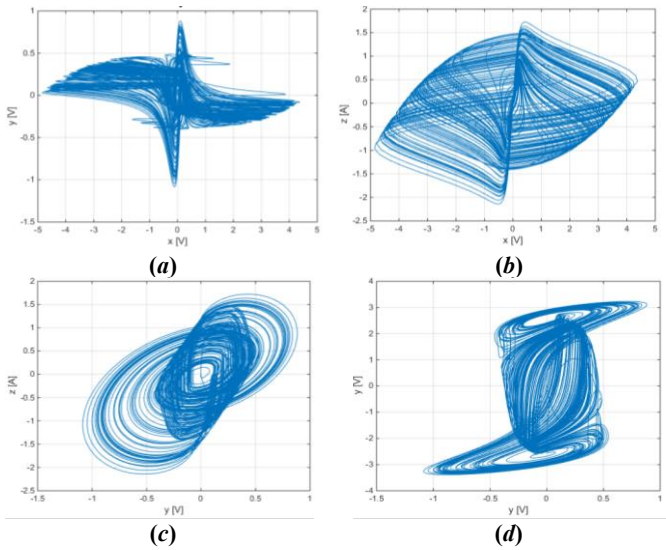


Figure 4. Chaotic attractors of memristor based hyperchaotic circuit (*a*) *x-y* (*b*) *x-z* (*a*) *y-z* (*b*) *y-u*

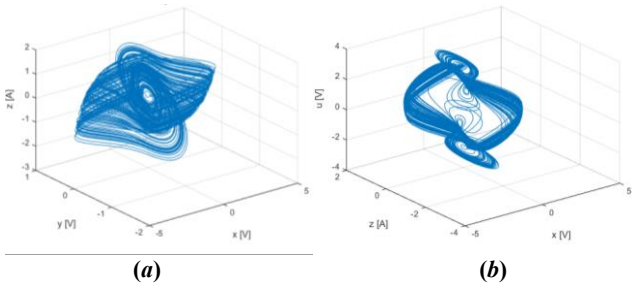


Figure 5. Three dimensional graphs of attractors of memristor based hyperchaotic circuit (a) *x-y-z* and (b) *x-z-u*

When the numerical simulation results obtained from the designed memristor based hyperchaotic circuit are examined, it is observed that the numerical range of each variable parameter varies between nearly −5V and + 5V. The electronic circuit of the designed hyperchaotic system in Eq. (5) is modeled in the OrCAD-PSpice circuit design program, which is given in Figure 6. An electronic model of system which is experimentally established in a laboratory environment is submitted. The components values are given in Table 1. Real time results are observed with the help of oscilloscope which is illustrated in Figure 7. The real time results of this system are consistent with the MATLAB simulation results.

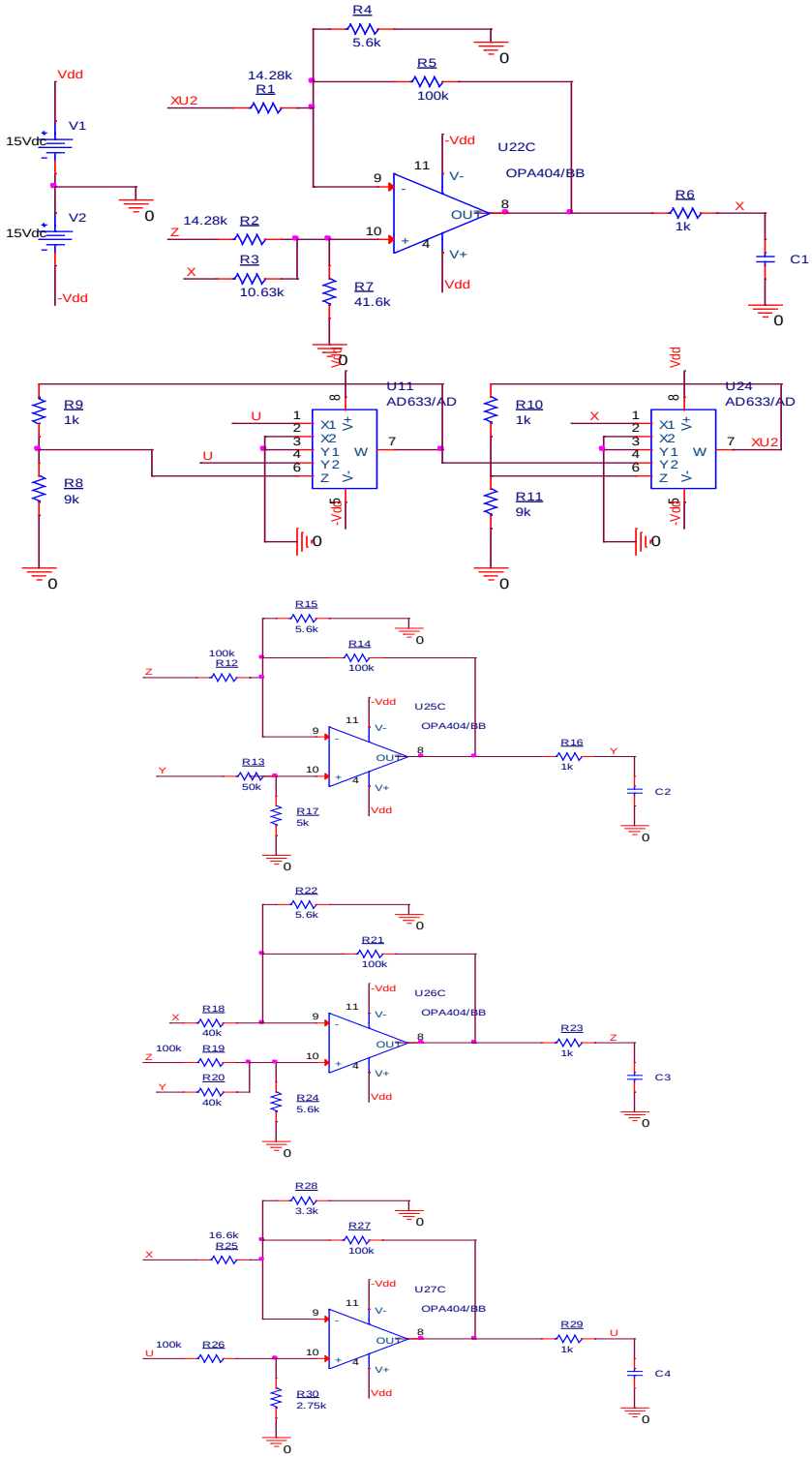


Figure 6. The electronic circuits of the memristor based hyperchaotic system

Table 1. Components of memristor based hyperchaotic circuit

Source	Value	Source	Value
AM	AD633JN	$R_8=R_{11}$	9 kΩ
Opamp	OPA404/TL084	R_{13}	50 kΩ
$R_1=R_2$	14.28 kΩ	R_{17}	5 kΩ
R_3	10.63 kΩ	$R_{18}=R_{20}$	40 kΩ
$R_4=R_{15}=R_{22}=R_{24}$	5.6 kΩ	R_{25}	16.6 kΩ
$R_5=R_{12}=R_{14}=R_{19}=R_{21}=R_{26}=R_{27}$	100 kΩ	R_{28}	3.3 kΩ
$R_6=R_9=R_{10}=R_{16}=R_{23}=R_{29}$	1 kΩ	R_{30}	2.75 kΩ
R_7	41.7 kΩ	$C_1=C_2=C_3=C_4$	1nF-100 nF
		V_s	± 15 V

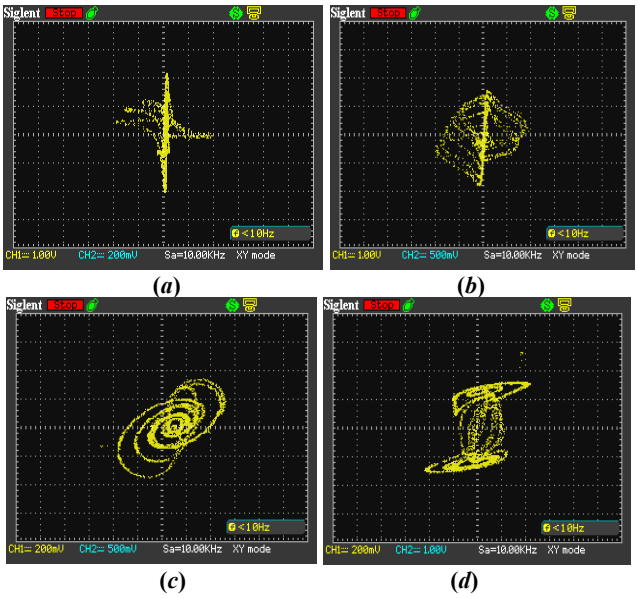


Figure 7. Experimental chaotic attractors (*a*) *x-y* (*b*) *x-z* (*c*) *y-z* (*d*) *y-u*

3.2 Equilibrium points

Behaviors around equilibrium points are important for explaining the stability of the system. If the orbits around the equilibrium points converge to these points, the system is asymptotically stable. If it diverges, the system is unstable. The system is stable in an orbit around the equilibrium point, unless asymptotically unstable. Designed memristor based hyperchaotic circuit's state equations are equaled to zero and this is given Eq. (6) when the parameters are used as a=7, b=1, c=2.5, d=1, e=3.75, f=3, n=-6, m_0=-1.2 *and* m_1=1, initial conditions $x(0)$=0.1, $y(0)$=0, $z(0)$=0 and $u(0)$=0.

$$\begin{aligned} 0 &= az - ax(m_0 + m_1 u^2) \\ 0 &= bdy - bz \\ 0 &= cy - cx \\ 0 &= nx \end{aligned} \tag{6}$$

Equations are set to zero and solved as shown above to find the solution of equilibrium points E= (E_1, E_2, E_3, E_4) of the designed system. If the expressions found in the solution of the equations are real numbers, it can be said that the system has equilibrium points. By examining the eigenvalues obtained using equilibrium points, comments can be made about the equilibrium point. The equilibrium points are asymptotically stable if the real eigenvalues (or real parts of complex eigenvalues) are negative. Stable nodes and stable focus are given as examples of such equilibrium positions. The corresponding equilibrium point is unstable if the real part of at least one eigenvalue is positive such as a saddle. If the system has purely imaginary roots, equilibrium point is a center. For this system, E= (0, 0, 0, ρ) equilibrium points are given and ($\rho = 1.261$) can be used. After finding the equilibrium points, the Jacobian matrix is created and analyzed according to the equilibrium points of the system.

$$Jac(x,y,z,u) = \begin{pmatrix} -am_0 - am_1u^2 & 0 & a & -2am_1ux \\ 0 & bd & -b & 0 \\ -c & c & 0 & 0 \\ n & 0 & 0 & 0 \end{pmatrix} \tag{7}$$

The characteristic equation of is shown by,

$$\det(\lambda I - J) = 0 \tag{8}$$

Eq. (6) is solved and roots are λ_1= 0, λ_2= -1.152+4.15i, λ_3= -1.152-4.15i and λ_4=0.574. The eigenvalues found in order to express the stability or instability of the system are examined. If at least one of the eigenvalues obtained should have positive, the system is unstable. Since λ_4 meets this requirement for the designed system, the system is chaotic.

3.3 Lyapunov exponents

The Lyapunov exponents method is a mathematical analysis method that shows whether the time series of the system has chaotic components. In addition, this method shows the numerical expression of the sensitivity to initial conditions, one of the most important features of chaotic systems and the Lyapunov exponent is represented by L [34]. L_1=0.31, L_2=0.0097, L_3=-0.0098 and L_4=-30.21 are obtained when the parameters are fixed as specified (a=7, b=1, c=2.5, d=1, m_0=-1.2, m_1=1 and n=-6) and this system is started to run for initial conditions (0.1, 0, 0, 0). To mention the chaotic of a system, the system must have at least one positive Lyapunov exponent. Lyapunov graph of the designed memristor based hyperchaotic circuit is shown in Figure 8.

$$D_L = j + \frac{\sum_i^j L_i}{L_{j+1}} = 3.01 \tag{9}$$

As can be seen, two of the Lyapunov exponents in Figure 8 has a positive value. This is a necessary condition to be hyperchaotic. The system maintains positive Lyapunov exponents values even if the time is increased. Therefore, it is said that the designed circuit is a hyperchaotic system [35].

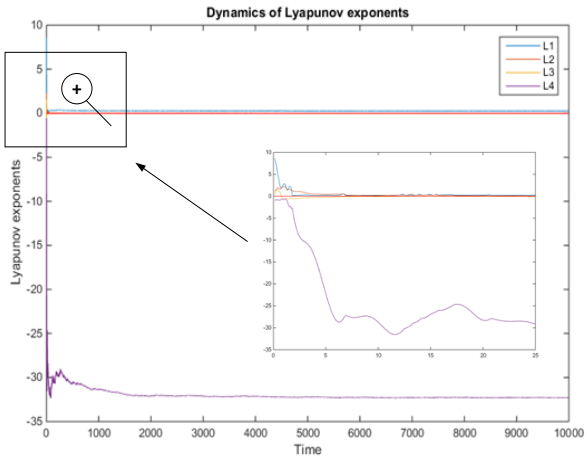


Figure 8. Dynamics of Lyapunov exponent

3.4 Bifurcation diagram

Bifurcation can be defined as small changes in the parameters affecting the behavior of the system in dynamic systems, causing sudden changes in the equilibrium of the system. While the bifurcation diagram is obtained, the differential equation system in Eq. (5) is solved with on MATLAB software and bifurcation diagram is given in Figure 9.

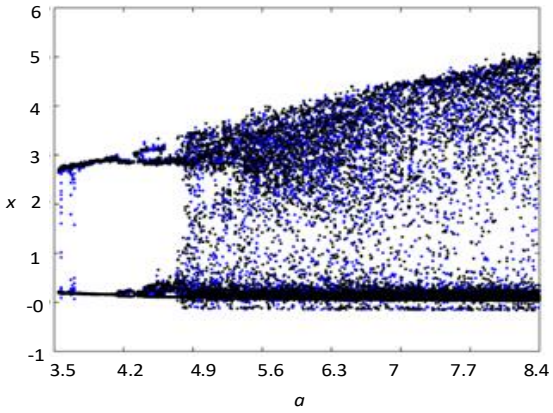


Figure 9. Bifurcation diagram of memristor based hyperchaotic circuit (for "*a*" parameter)

The results of the orbits are expressed in different colors shown for different initial conditions such as black (0.1, 0, 0, 0) and blue (0.1, 0, 0.01, 1) in Figure 9. These colors provide some information in bifurcation schemes. The initial conditions of the system for the parameter is selected in the range of 3.5 to 8.4, with the other parameters remaining constant. It can be seen from the figure that the circuit will show periodic behavior for $a \in$(3.5-4.1), quasi-periodic behavior for $a \in$(4.2-4.6) and chaotic behavior for $a \in$(4.3-8.4). Bifurcation analysis given above has been obtained by applying some dynamic properties to the designed system.

4. CHAOTIC COMMUNICATION FOR ANALOG AND DIGITAL MODULATION TEQHNIQUE

4.1 Chaotic masking

When the studies are examined, one of the methods used in the chaos based secure communication systems is the chaotic masking method. The idea of transmitting and encrypting data using chaos in communication systems emerged in 1990. It has been shown by Pecora and Carroll that synchronization is possible in two different chaotic oscillators [36]. The first study on communication is chaotic masking. In 1993, Cuomo and Oppenheim [7, 37] established and demonstrated a secure communication system using the Lorenz equation system. These studies are important in terms of being the first application in chaotic communication system design, since they show how synchronization concept can be used in masking the information sign by adding chaotic signals to an information signal. Synchronization ensures that two or more systems with different chaotic behavior show the same chaotic behavior. Due to the importance of the synchronization concept in the receiver circuit, PID controls have been preferred to ensure synchronization of chaotic circuits operated with different initial conditions. The optimization method is preferred in obtaining the gain coefficients of the PID controller. PID gain coefficients are obtained by using the Firefly algorithm. Blocks diagram of synchronization chaotic system is given Figure 10.

In order to make numerical designs of differential equations, it is necessary to make the equations independent of time. There are many discretization methods in the literature. These methods have advantages and disadvantages compared to each other. For example, while one method uses less hardware than the other does, the same method can discriminate with a higher margin of error than the other can. Due to the circuit structure used in this study, the margin of error should be within the appropriate limits. Since the design of chaotic behavior on a digital platform is obtained, less resource usage makes the chosen method even more important [38, 39]. For this reason, Euler method is chosen as the discretization method. Comparison of discretization methods is illustrated in Table 2.

The state equations of the memristor based hyperchaotic circuit model are converted to the following discrete time equations with a step interval of T= 1e-3. Euler method is given Eq. (10).

$$x[n+1] = x[n] + Ty[n] \tag{10}$$

Discrete master circuit:

$$\begin{aligned} x_{m1}[n+1] &= T(ax_{m3}[n] - ax_{m1}[n]m_0 - am_1 x_{m1}[n]x_{m4}[n]^2) + x_{m1}[n] \\ x_{m2}[n+1] &= T(b(dx_{m2}[n] - x_{m3}[n])) + x_{m2}[n] \\ x_{m3}[n+1] &= T(-c(x_{m1}[n] - x_{m2}[n])) + x_{m3}[n] \\ x_{m4}[n+1] &= T(nx_{m1}[n]) + x_{m4}[n] \end{aligned} \tag{11}$$

Discrete slave circuit:

$$\begin{aligned} x_{s1}[n+1] &= T(ax_{s3}[n] - ax_{s1}[n]m_0 - am_1 x_{s1}[n]x_{s4}[n]^2) + x_{s1}[n] \\ x_{s2}[n+1] &= T(b(dx_{s3}[n] - x_{s2}[n])) + x_{s2}[n] \\ x_{s3}[n+1] &= T(-c(x_{s1}[n] - x_{s2}[n])) + x_{s3}[n] \\ x_{s4}[n+1] &= T(nx_{s1}[n]) + x_{s4}[n] \end{aligned} \tag{12}$$

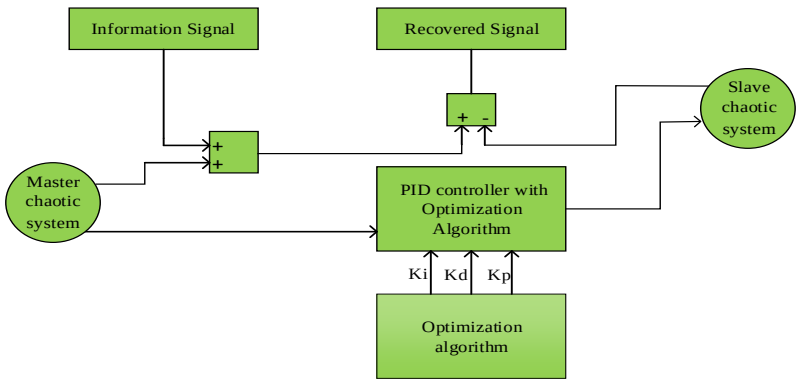


Figure 10. Blocks diagram of synchronization chaotic system

Table 2. Comparison of discretization methods

	Euler's Method	Taylor Series Method	Runge-Kutta Methods
Advantages	1. Simple and direct 2. This method can be used for nonlinear IVPs	1. One step, explicit 2. This method can be high order 3. Easy to show that global error is the same order as LTE.	1. One step method 2. Global error is of the same order as local error. 3. Don't need to know derivatives of *f*. 4. Easy for "Automatic Error Control".
Disadvantages	It is less accurate and numerically unstable. Usually applicable to explicit differential equations.	Needs the explicit form of derivatives of *f*. Truncation error tends to grow rapidly away from expansion point.	They require significantly more computer time than multi-step methods of comparable accuracy, and they do not easily yield good *global* estimates of the truncation error.

Error:

$$\begin{aligned} e_1[n] &= x_{m1}[n] - x_{s1}[n] \\ e_2[n] &= x_{m2}[n] - x_{s2}[n] \\ e_3[n] &= x_{m3}[n] - x_{s3}[n] \\ e_4[n] &= x_{m4}[n] - x_{s4}[n] \end{aligned} \tag{13}$$

The discrete PID control input is,

$$c[n+1] = K_p e + K_i (I_{n-1} + edt) + K_d \frac{e - e_{n-1}}{dt} \tag{14}$$

4.2 COOK modulation

In this part, memristor based hyperchaotic circuit is implemented to digital communication by using COOK modulation. There is no need for synchronization here, which allows the transmitter to spend less energy. COOK modulation is a special case of CSK that does not require a carrier based on bit energy estimation. This communication system requires only one chaotic signal. When the "+1" symbol is transmitted, "-1" symbol is displayed with zero transmission. The modulation process can be thought of as turning the chaotic generator on and off. Demodulation can be carried out using a simple bit energy estimator as in a carrier free structure [40]. The block diagram of COOK modulator and demodulator is shown in Figure 11.

$$s(t) = \begin{cases} c(t), & for \quad 1 \\ 0, & for \quad 0 \end{cases} \tag{15}$$

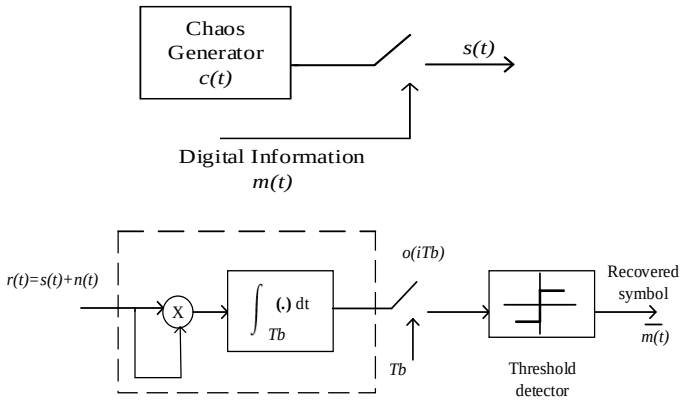


Figure 11. Block diagram of COOK modulator and demodulator

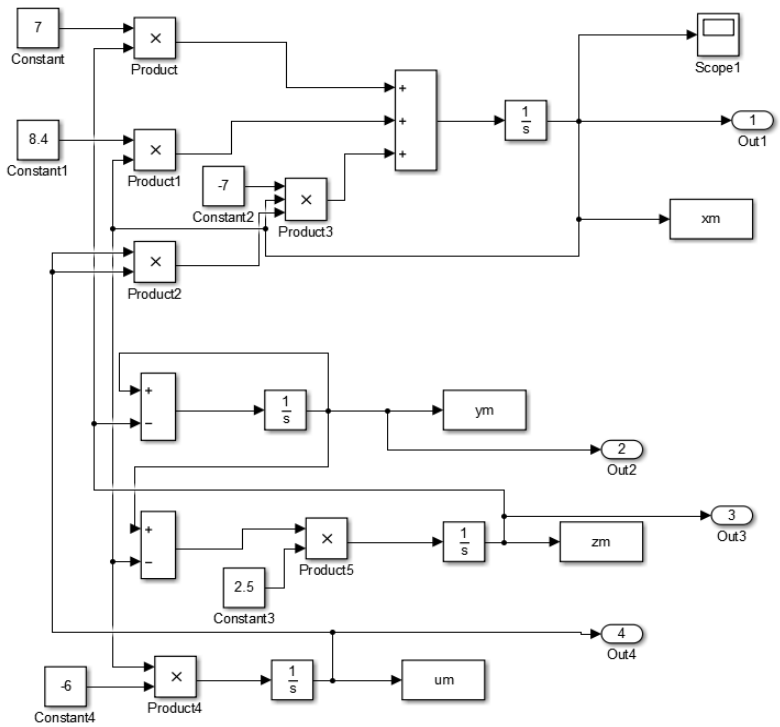


Figure 12. Block diagram of a memristor based hyperchaotic circuit

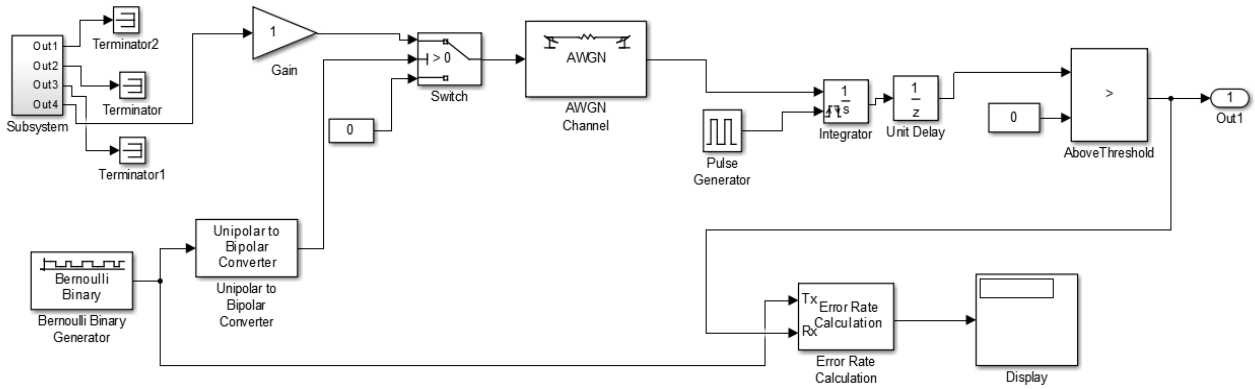


Figure 13. Block diagram of COOK modulation on MATLAB&Simulink for memristor based hyperchaotic circuit

The modulated signal from the COOK modulator circuit is transmitted via the communication channel $s(t)$ to the demodulator circuit on the receiving side as shown in Figure 11. In the demodulator circuit, the noise added to the modulated signal in the transmission channel is collected together with $n(t)$. This signal is then multiplied by $r(t)$ to be integrated (correlator unit) and transmitted to the threshold detector. The signal obtained from the correlation comes to the threshold detector and the information signal is obtained according to the threshold level determined in this part [41].

The signal from the correlator is transmitted to the threshold detector. Information is obtained according to the threshold level specified in this section. The threshold value in the decision circuit is important for the success of COOK modulation. This value changes depending on the noise. This is a disadvantage of COOK modulation [41, 42].

The signals, which are obtained from memristor based hyperchaotic circuit, are used in COOK modulation on MATLAB. Figure 12 shows a block diagram of a memristor based hyperchaotic circuit. In the COOK modulation of this signal, the communication block diagram under AWGN channel is given in Figure 13. In the communication application of the system designed in MATLAB environment 4000 bits are sent, the bit duration is selected as $T_b = 0.01$ and delay time as $T_b = 0.5$.

5. APPLICATIONS OF COMMUNICATION SYSTEMS ON FPGA PLATFORM

Due to the characteristics of FPGA, chips such as being numerical and reprogrammable, parameter changes of the system can be performed easily in chaotic system based FPGA applications. In addition, with the change of system parameters, the change in the dynamic behavior of the system can easily be seen. Compared to analog circuit oscillators, the fact that FPGA is fast, reliable and easy to design. This has made it possible to complete the work in the chaos area faster and to make it easier to develop new methods. Xilinx System Generator (XSG) is a high level MATLAB&Simulink based software platform that is used to quickly and easily design. Xilinx FPGA cards, perform hardware based simulation and perform real-time applications on the board [43]. XSG has a library based blocks in MATLAB&Simulink for arithmetic and logic applications, memory applications and Digital Signal Processing (DSP) applications. The only difference between XSG blocks and general Simulink blocks is that XSG blocks are used in discrete time and fixed point number format. The communication application of the designed chaotic systems is synthesized by using Xilinx Spartan-3E family XC3S500E board.

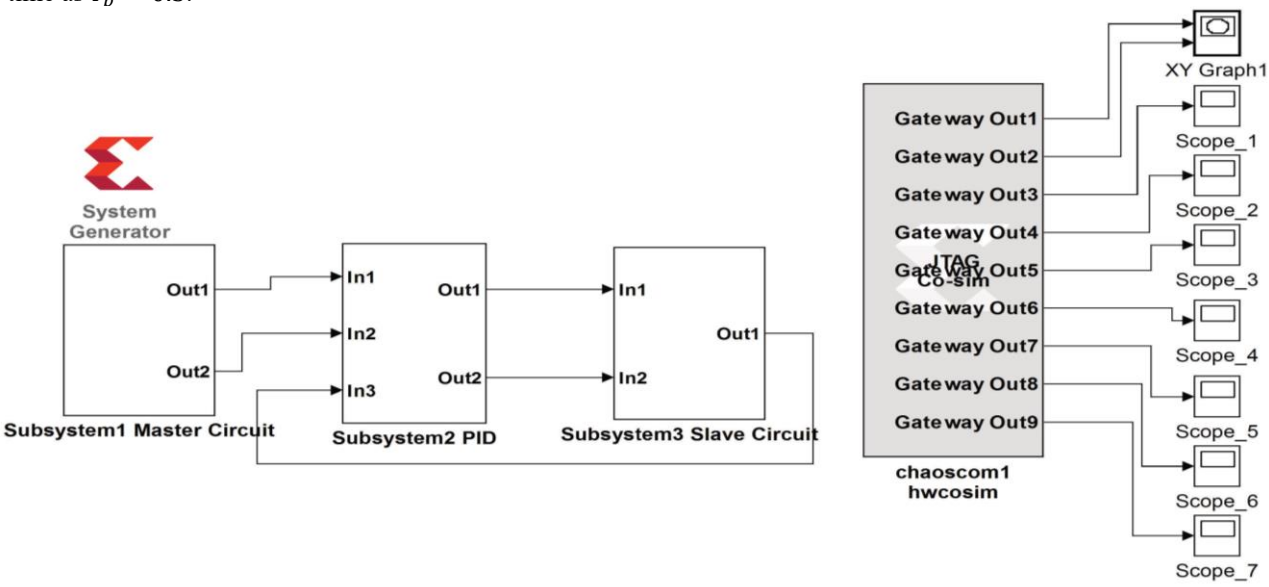


Figure 14. Block diagram of communication system on FPGA

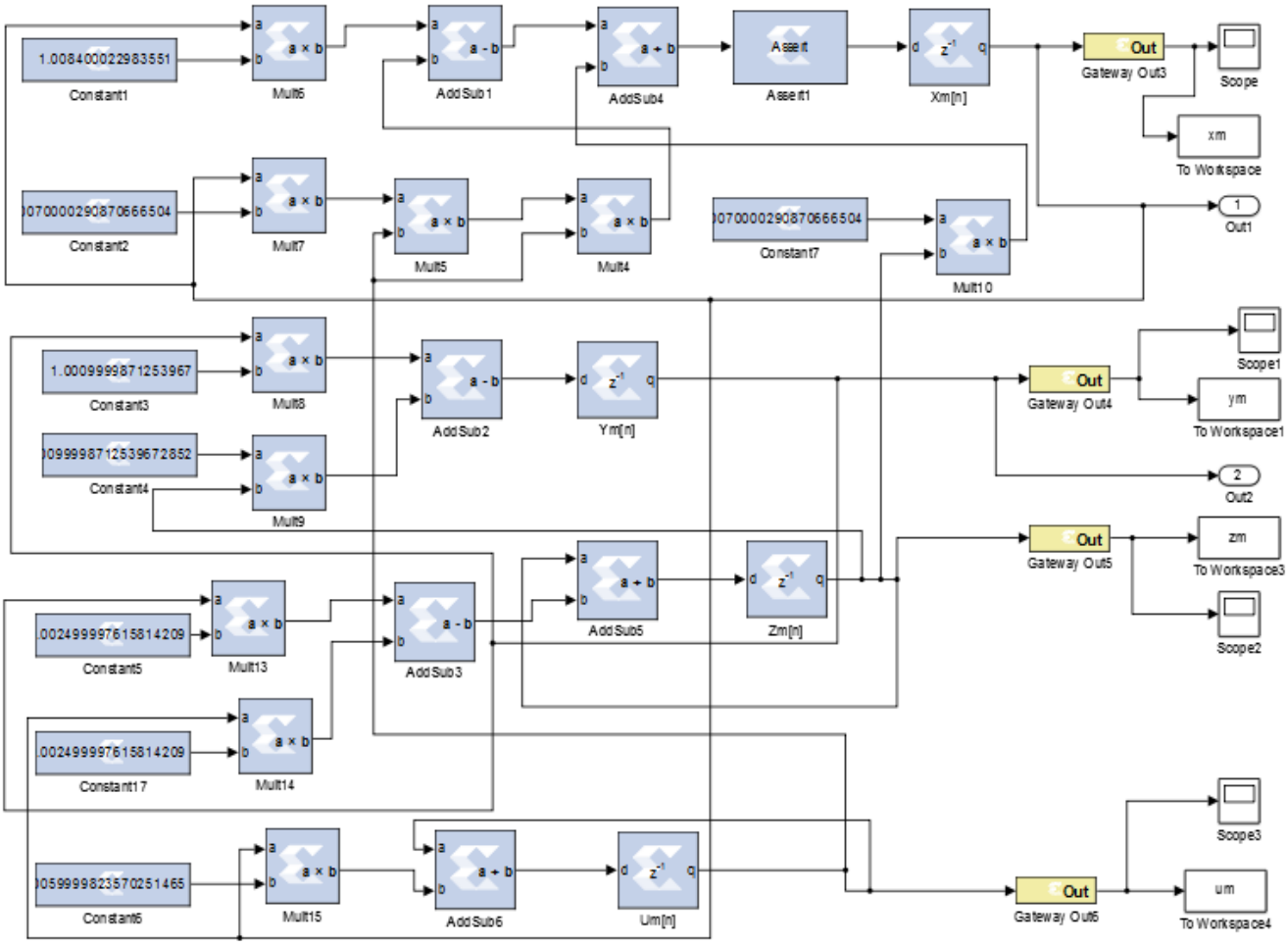


Figure 15. Block diagram of subsystem for memristor based hyperchaotic master circuit

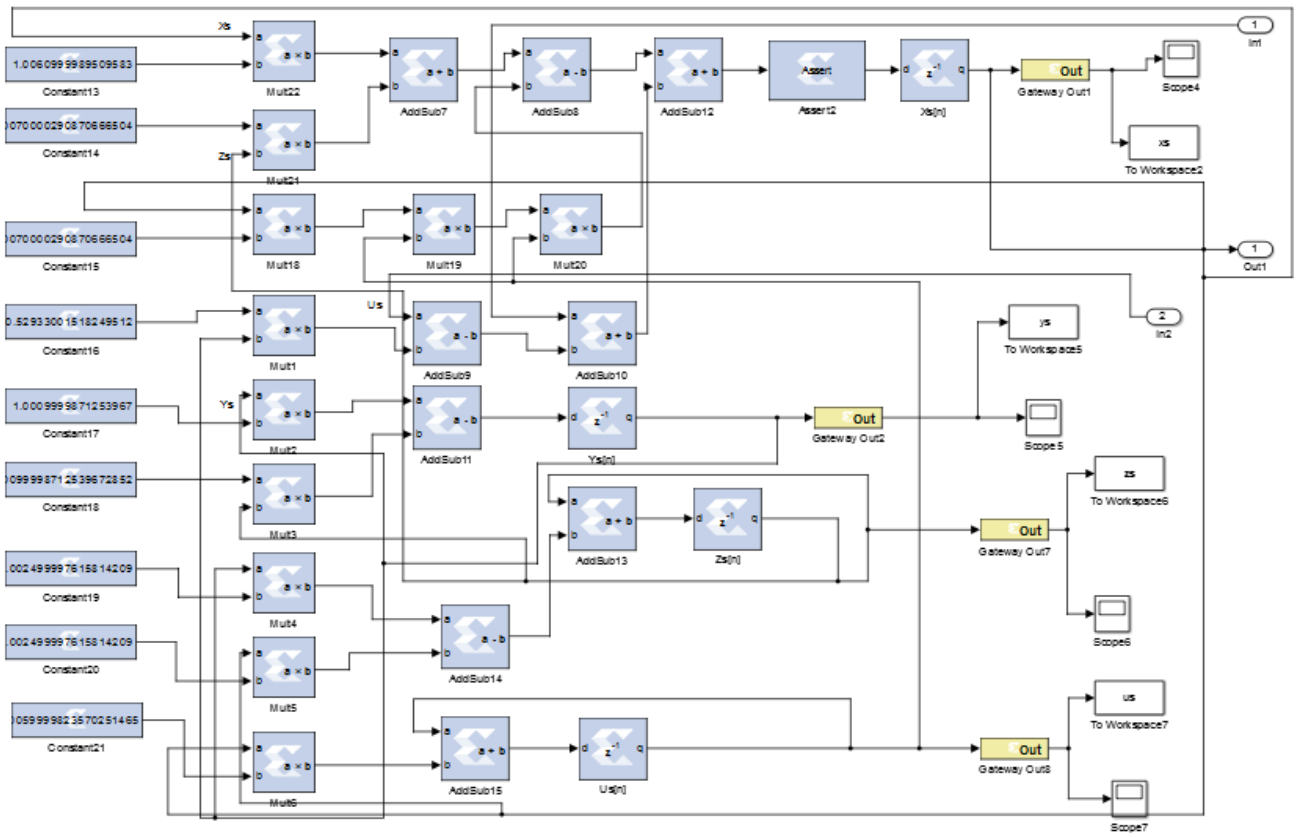


Figure 16. Block diagram of subsystem for memristor based hyperchaotic slave circuit

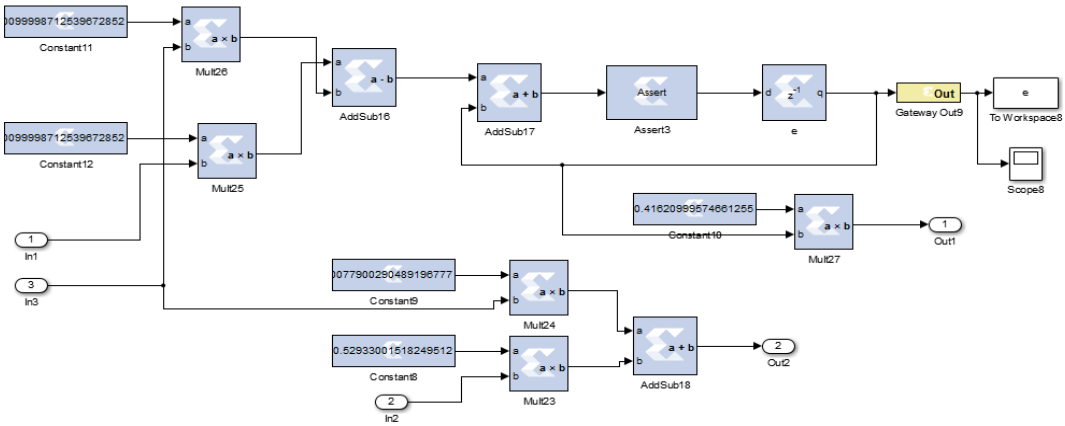
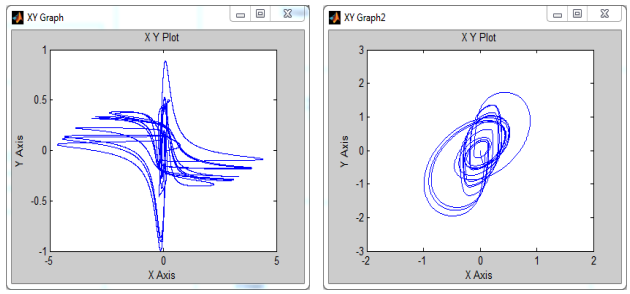


Figure 17. Block diagram of subsystem for PID controller

5.1 Chaotic masking

The application of the hyperchaotic circuit designed in this section to the communication systems is realized by using analog modulation technique. The discretized equations in the previous section are modeled in XSG in FPGA environment. The designed system is modeled using Xilinx ISE Design Tools 14.5 simulation program.

Figure 14 shows the design of the whole system on FPGA. As shown in Figure 14, the system consists of three subsystems, which include model of master, slave and PID controller circuits. The block diagram of master, slave circuits and PID control are given Figures 15, 16 and 17, respectively. The different initial conditions are master circuit [0.1, 0, 0, 0] and slave circuit [0, 0, 0, 0]. After the synchronized chaotic system is designed in MATLAB&Simulink environment, it will be sent to FPGA by the hardware cosimulation method and real time outputs will be observed in MATLAB&Simulink environment. The PID controller gain coefficients are obtained from the Firefly algorithm used for optimization, which are $K_p = 7.79, K_i = 416.21$ and $K_d = 529.3$ as obtained in the previous study [33]. The parameter values used in the Firefly algorithm are selected as 20 for iterations and 50 for the population number. The algorithm performs the simulation for 100 seconds. The sum of the absolute error is obtained from the samples in the last 4 seconds as 8.2e-28.



(*a*) (*b*)

Figure 18. Chaotic attractors of memristor based hyperchaotic circuit (*a*) *x*-*y* (*b*) *y*–*z* on FPGA

The phase portraits of the chaotic circuits designed on the FPGA platform are shown in Figure 18 in the form of *x*-*y* and *y*-*z*. Figure 19 shows the synchronization of the signal *u*[n] used as a carrier after it has been obtained under different initial conditions for the master and slave circuit. Chaotic signals of master circuit and slave circuit unsynchronized without PID controller is given in Figure 20. As shown in the figure, when synchronization is not performed, the master and slave signals are different from each other for different initial conditions. A good transmission of information cannot be achieved in this way.

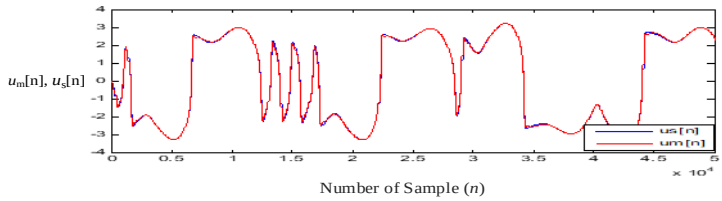


Figure 19. Chaotic signals of master circuit and slave circuit synchronized with PID controller (u_m[n], u_s[n]-Number of sample (n))

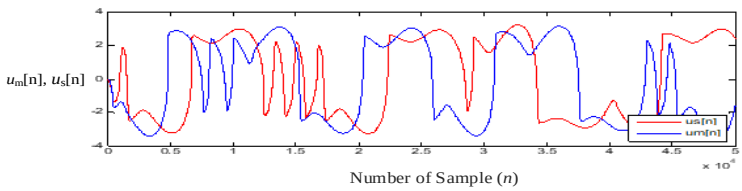


Figure 20. Hyperchaotic signals of master circuit and slave circuit unsynchronized without PID controller (u_s[n]-Number of sample (n))

The difference between the master and slave circuits synchronized with the help of PID controls shown in Figure 21 is equalized to zero in a short time. Error waveforms of the master and slave systems obtained after synchronizing using the algorithm are shown in Figure 21. When state errors of the synchronization system (e_1, e_2, e_3, e_4) are analyzed, it is observed that the hyperchaotic system is synchronized in a short time and the amount of exceedance is low.

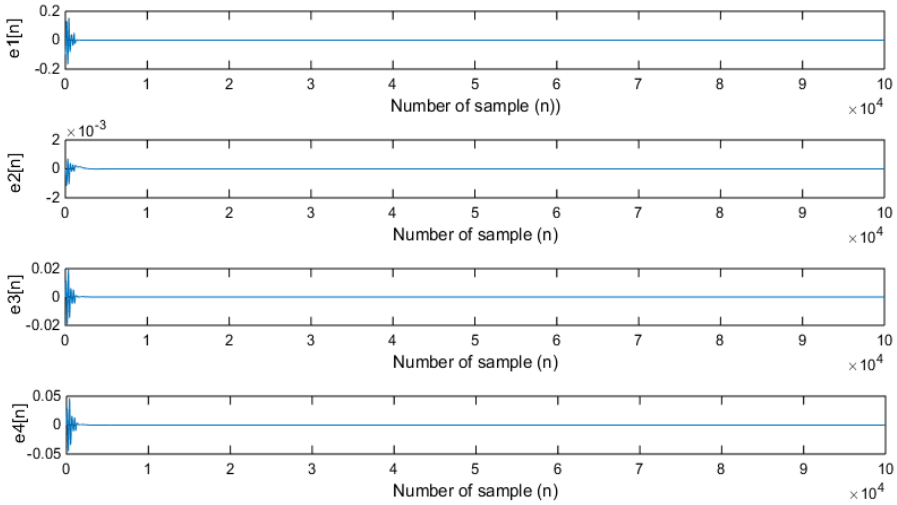


Figure 21. Error waveforms between synchronized master and slave system

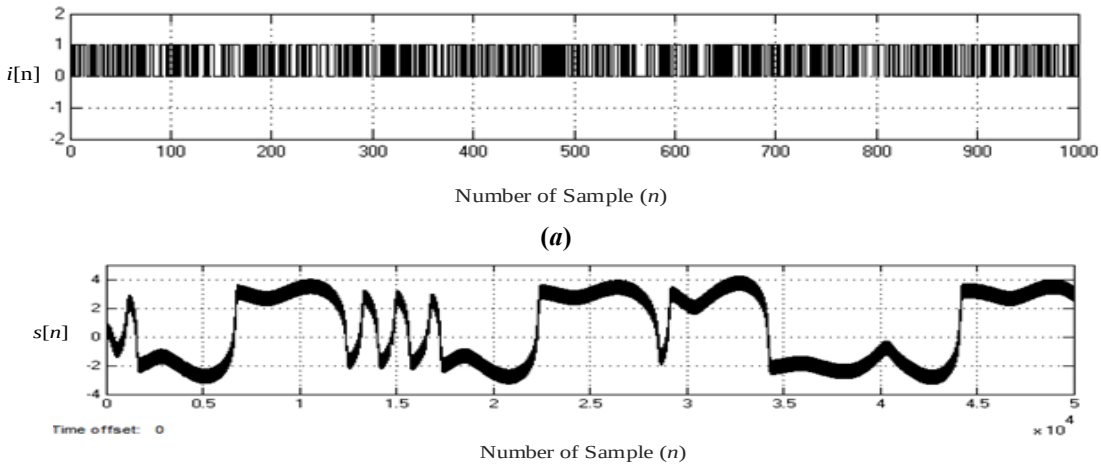


Figure 22. (*a*) The information signal *i*[n] (*b*) The transmitted signal *s*[n]

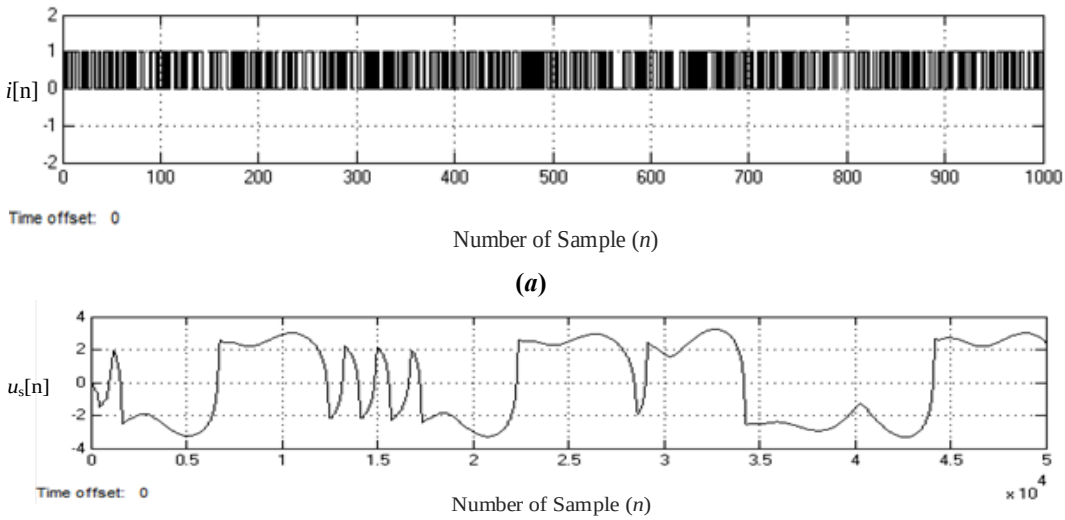


Figure 23. (*a*) The recovered signal *i*[n] (b) The hyperchaotic signal u_s[n]

Table 3. Final mapping report for memristor based hyperchaotic circuit with chaotic masking on FPGA

Resource	Utilization
Slice register	343
LUTs	640
Flip-Flop	287
Bonded IOBs	289
BUFG/BUFGCTRL/BUFHCEs	1
DSP4831s	68
Multiplier	26
Adder/Subtractor	18

A simple communication application is realized in FPGA environment by using the signal obtained from the synchronized circuit. In the chaotic masking technique, the information signal i[n] added to the carrier hyperchaotic signal u_m[n] is used in the communication system as s[n] signal on the receiving side. In Figure 22 (a) and (b), the information signal and the transmitted signal are shown, respectively. By subtracting the reproduced hyperchaotic signal from the incoming signal, the analog information signal is obtained and the transmitted information signal is obtained with very little error. The hyperchaotic signal u_s[n] and the recovered information signal i[n] used on the receiver side is shown in Figure 23. In order to achieve synchronization in chaotic masking, the power and amplitude of the information signal to be added must be considerably lower than the hyperchaotic carrier [44]. The number of processing blocks used in the design for the hyperchaotic circuit model and the resource utilization on the hardware are given in Table 3.

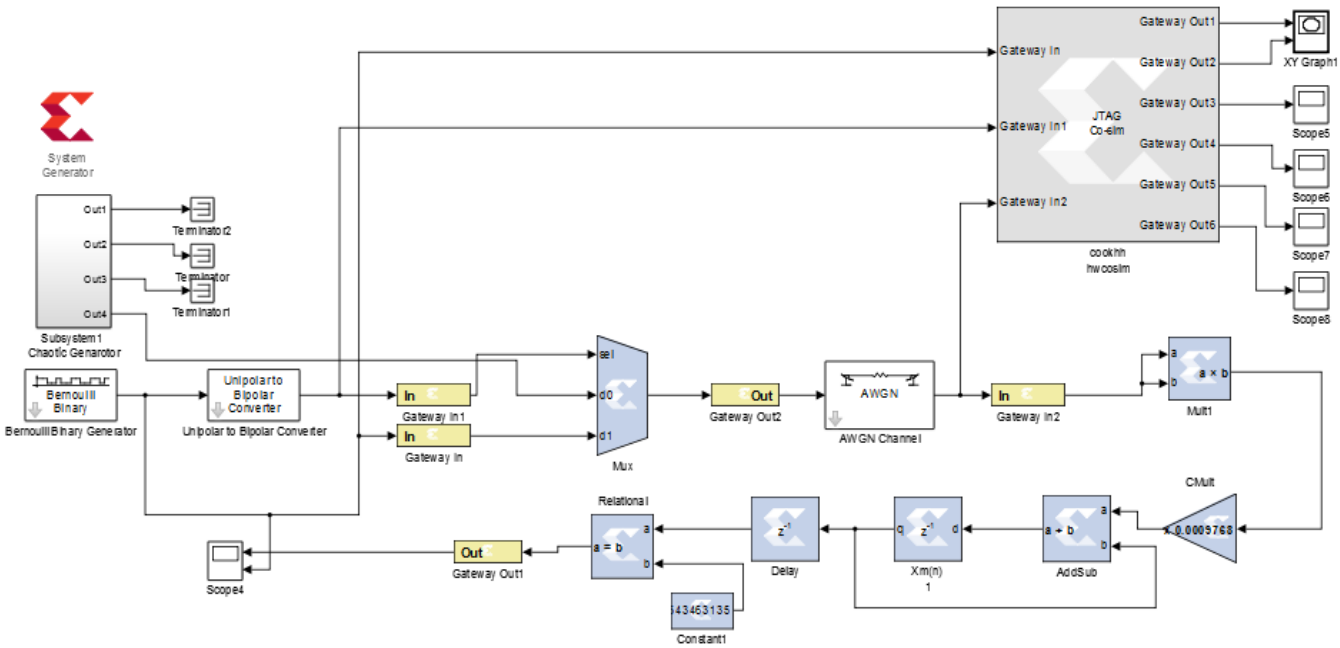


Figure 24. Block diagram of COOK modulation on FPGA

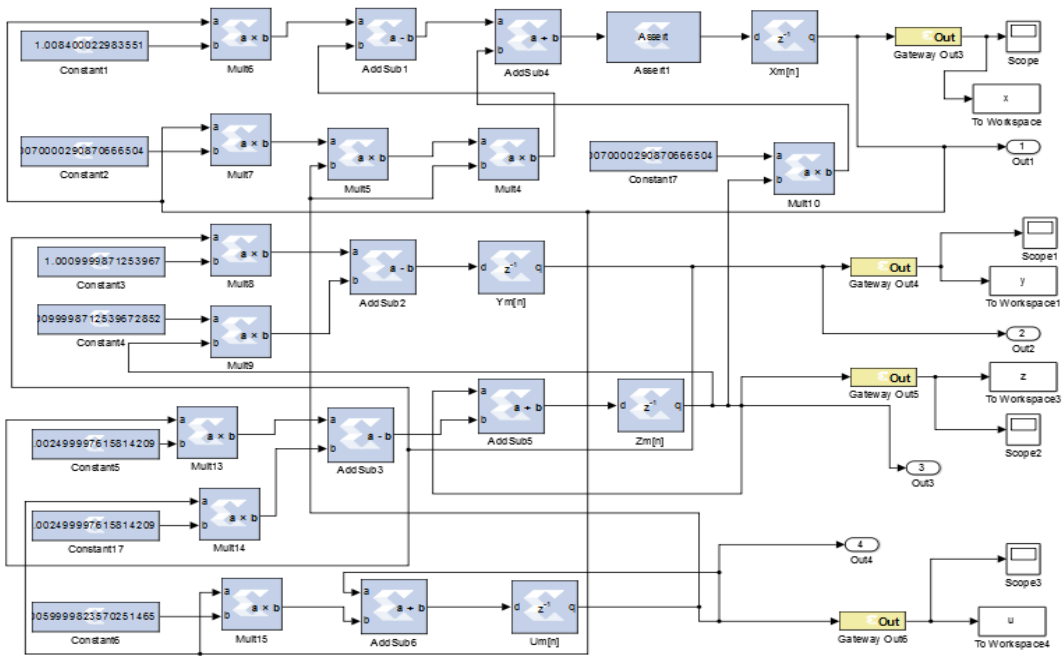


Figure 25. Block diagram of hyperchaotic circuit on FPGA

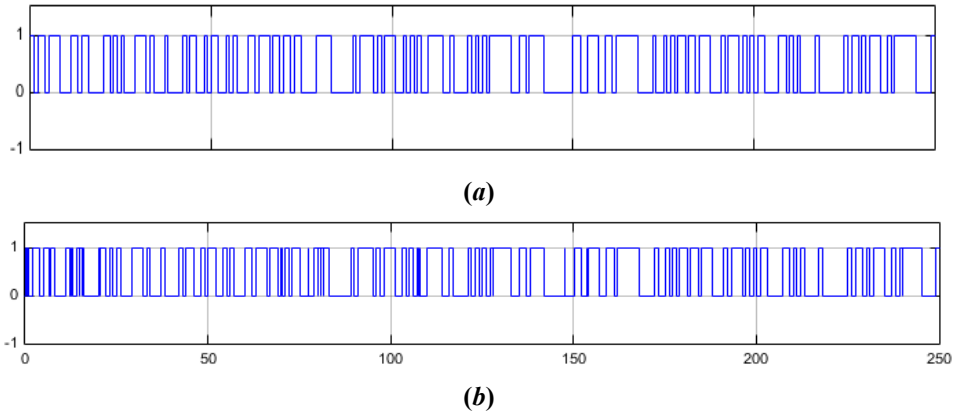


Figure 26. (a) Information signal (b) Recovered signal obtained from the COOK modulation

5.2 COOK modulation

Chaos based analog communication systems provide good performance in noise free environments, but are highly affected by noise in practice. Chaos based digital communication systems are less affected by noise than analog communication [26]. In this section, COOK modulation, one of the chaos based digital modulation techniques used in chaotic communication systems, is implemented.

In the previous section, the COOK model designed in MATLAB environment is remodeled on ISE XSG platform in order to realize it in FPGA environment. The blocks required for this system design are designed in COOK model using XSG and implemented in FPGA hardware.

Figures 24 and 25 show the COOK modulation model and the subsystem of the hyperchaotic signal used in the FPGA environment, respectively. The initial conditions are fixed for hyperchaotic circuit as [0.1, 0, 0, 0]. The design of the hyperchaotic system is designed using the required blocks in XSG in the form given in Eq. (11). In Figure 26(a) and (b) show the information signal and recovered signal obtained from the COOK modulation. The number of processing blocks used in the design for the hyperchaotic circuit model and the resource utilization on the hardware are given in Table 4.

Table 4. Final mapping report for memristor based hyperchaotic circuit with COOK modulation on FPGA

Resource	Utilization
Slice register	214
LUTs	294
Flip-Flop	175
Bonded IOBs	227
DSP4831s	34
BUFG/BUFGCTRL/BUFHCEs	1
Multiplier	11
Adder/Subtractor	7

The performance of the designed communication system is analyzed under AWGN (Additive White Gaussian Noise) channel model with E_b/N_0 (Bit energy level/noise power spectral density) values between 0 dB and 20 dB. As can be seen in Figure 27, the transmitted bits also depend on the noise of the AWGN, very few errors occur in the realized system. Figure 27 shows BER (Bit Error Rate) performance graph for different E_b/N_0 values obtained by MATLAB&Simulink, which is realized by using the FPGA based design method with memristor based hyperchaotic circuit.

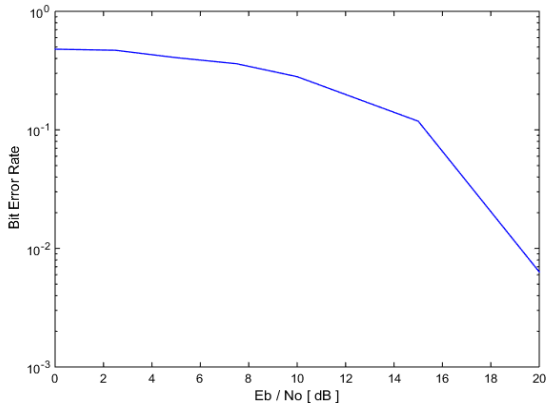


Figure 27. BER graph of memristor based hyperchaotic circuit

6. CONCLUSION

In this study, a hyperchaotic circuit model and its application to communication systems according to analog and digital modulation techniques are realized in hardware on FPGA platform. The chaotic analysis of the memristor based hyperchaotic circuit designed with the memristor emulator is performed and the results of the system are presented in real-time. As a result of the hyperchaotic analysis performed, it is confirmed by numerical results that the system is a hyperchaotic system. An electronic circuit model of the designed system is submitted. Thanks to the digital structure of the FPGA, it is observed that the real-time results confirm the simulation results. Furthermore, when using FPGA to produce chaotic signals, it is observed that FPGA is easy, fast, and reliable.

In order to use hyperchaotic circuits for communication systems, synchronization in analog modulation schemes is important. Based on the optimization algorithms, the PID control system is designed to synchronize the two hyperchaotic signals and its gain coefficients are obtained by using Firefly algorithms. A successful synchronization system design is confirmed by numerical results. Moreover, the application of the designed hyperchaotic system to digital communication systems is performed based on FPGA and BER analysis which has been realized for different E_b/N_0 values is submitted. The results of the study show that the memristor based hyperchaotic systems can be applied more

easily in FPGA applications and used for other chaotic communication systems due to their performance in chaotic communication systems.

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