

A low noise low power 45 nm technology based simultaneous switching noise (SSN) reduction model for mixed signal VLSI circuits

S. Seenuvasamurthi*, G. Nagarajan

Department of ECE, Pondicherry Engineering College, Pondicherry-605 014, India

Corresponding Author Email: seenu_er@yahoo.co.in

https://doi.org/10.18280/ama_d.230103

ABSTRACT

Received: 6 July 2018

Accepted: 15 November 2018

Keywords:

ALU, gate diffusion input (GDI), simultaneous switching noise (SSN)

Low noise, low power, minimum delay and smaller area are the prime factors in the current VLSI system design. There are many sources for noises that exhibit various types of noise. Noise in digital ICs can be credited to various sources such as PSN due to circuit switching transition, deviations in device parameters due to process changes, crosstalk noise caused by capacitive coupling among neighbouring circuit interconnects, noise due to charge sharing and charge leakage. Reducing noise is an important factor in VLSI design. This work involves the analysis and reduction of switching noise in the inverter based equivalent circuit model in 45 nm technology. Also, aims to minimize the power utilization, area and delay. Further the noise analysis is extended to half adder circuit and ALU. The noise value observed for the proposed circuit is 140 μ V whereas it is 33 mV for the existing circuit. The same circuit is implemented in GDI based half adder and 4 bit ALU. The simulation result show that the proposed model has reported low noise compared with the existing methods.

1. INTRODUCTION

In recent years, the number of devices on a chip has spectacularly increased because of technological scaling in size of the devices [1-2]. Today's VLSI technology allows complex circuits to be fabricated in a single semiconductor silicon die with high speed digital logic fitted along with high performance circuits. Though the clock signal frequencies continue to increase but the MOS device sizes will continue to shrivel to Very Deep Sub Micrometer (VDSM) dimensions [3-5]. Reducing the device size not only implies shorter channel length but also decreasing device threshold voltages and decreasing inter connects. Due to this scaling, the devices have become more sensitive to the noise. Noise is an important issue in both analog and digital circuits which determines the characteristics of the system. The problem of noise has increased the significance of on-chip noise and thus becomes the major research area for continuing the development in ICs performance, power, speed, density etc., [6-8].

The works in [9-10] focused on power supply noise and switching noise consideration, especially to enhance the performance of the mixed signal. In the mixed signal circuits, the switching noise is one of the limiting factors [11]. Digital section in the mixed signal circuits are performed with the same substrate for the overall performance [12]. Switching of the digital circuits leads the substrate noise to the other circuits. Analog devices are slowly degrading when the substrate noise is presented in the mixed signal circuits. Switching noise from the digital circuits started from the current peaks. That current peak generates the voltage fluctuations in the V_{DD} and Ground lines of the circuit. These voltage deviations are generally termed as "Switching Noise". Switching noise reduction is one of the challenging processes for the efficient System on Chip (SoC) [13].

Unless the area and power requirements are significantly minimized, the resulting heat dissipation and deviation of a signal from its nominal value in those sub-intervals of time will affect the packing density and performance of ICs. Thus the necessity of effective area and low power design becomes very important. Expansion of mobile technology and wireless network communication applications has large demands on signal processing. The aim of such approaches is to improve the performance of Arithmetic and Logic Unit (ALU) in terms of low power consumption, minimum area utilization and less propagation delay. Hence, high performance of adder and multiplier structure is necessary to improve the efficiency of ALU unit [14]. To handle this problem, various techniques have been proposed and the most commonly used techniques are modulation of the clock system [15], decoupling capacitors [16], separate power supplies for analog and digital circuits, use of guard rings, noise cancellation through sensing the noise [17], use of in-built self noise detection circuits [18], improving the mutual coupling between the paths by varying width and length [19]. Other techniques utilize the use of logic families which do not generate noise but they guzzle higher power than the regular MOS devices [20].

This work involves the analysis and reduction of switching noise in the inverter based equivalent circuit model and aims to minimize the power utilization, area and delay. Further the noise analysis is extended to half adder circuit and ALU. The rest of the paper is described as follows: The section II discusses about the previous works in this domain. Section III explains about the proposed circuit construction, working and the mathematical model for the small signal equivalent. Section IV discusses on the simulation results and their interpretation. Section V concludes the paper.

2. NOISE ANALYSIS USING EQUIVALENT CIRCUIT MODEL

There are many works which have been reported on Simultaneous Switching Noise (SSN). The switching noise is highly presented by the equivalent circuit model. In that circuit model, the parasitic impedance (R, L and C) values are varied to estimate the noise analysis in terms of the voltage. There is no decoupling capacitor is used in the equivalent circuit model [21]. The value of the peak noise voltage (dBV_{rms}) and peak noise are high. Also, in the earlier works of Arithmetic and Logic Unit (ALU) module, it is designed by using the Ripple Carry Adder (RCA) and Binary Multiplier (BM) and static CMOS based full adder is used. In that ALU stage, a large number of transistor are utilized due to the traditional nanometer technology. By using the Ripple Carry Adder (RCA), the computation delay of the ALU stage is highly occurred. Due to the high resources utilizations, the switching noise reduction is considered as the major problem in the traditional ALU unit.

The continuous switching activity is one of the major challenges and also the reduction of switching noise is one of the main processes in the mixed signal circuits. Two tier solution based clock scheduling is proposed for switching noise minimization. First, the management of switching noise at the basic frequency ranges and the clock delays are controlled to reduction of ripples in specified band of frequency. By using current shaping circuits, the spectral peak is reduced by using the lower frequencies and upper frequencies of the given supply current. Considerable research work has been carried out in the Parasitic impedance (R, L and C) based inverter and noise analysis in the combinational circuits like the design of efficient adder structures such as Gate Diffusion Input based Full Adder (FA), Carry Select Adders (CSA), Ripple Carry Adder (RCA), Vedic Multiplier, Binary Subtractor and Barrel Shifter for improving the architecture performances for Arithmetic and Logic Unit (ALU) in VLSI [22]. However, efforts are still required to reduce the complexity in adder architectures for the growth of wireless communication applications. However, this work aims to develop noise reduction circuit and to implement in the GDI technique half adder and ALU unit for meeting the goals mentioned.

3. PROPOSED METHOD

Earlier works in the field of exchanging commotion utilized MOS quadratic V-I trademark. This work aims for developing a circuit with low noise, low power and minimum transistors. In any case, the model that is presented broadly utilized for short channel devices is the α -power law which shows that records for speed immersion impacts. Based on the Sakurai and Newton's α power model [23], the drain current of the MOS in the saturation region is given as,

$$I_D = K(V_{GS} - V_T)^\alpha \quad (1)$$

where,

V_T is the threshold voltage

α is the fitting parameter

Due to the α^{th} power functions, the closed form formulae are not possible to be determined, where, I_d is the function of gate and source voltage.

Thus, the drain current (I_d) of the transistor can be written as,

$$I_D = f(V_G, V_S) \quad (2)$$

Due to the I_d characteristics, the drain current of the transistor can be formulated as below,

$$I_D = K(V_G - V_0 - \gamma V_S) \text{ when, } (V_G \geq V_0 + \gamma V_S) \quad (3)$$

where,

V_0 measures the voltage displacement and ' γ ' is the effect of the channel length.

The parasitic inductance is the only element connected among the current source and ground. The SSN due to the discharging current for N similar drivers through the inductor can be given as

$$V(t) = NL d I_D(t)/dt \quad (4)$$

Eq. (3) is substituted in the Eq. (4) and the v_g and v_s can be replaced by v_{in} and v , respectively to obtain Eq. (5)

$$V(t) = NLK \left(d \frac{v_{in}(t)}{dt} - \gamma \frac{dv(t)}{dt} \right) \text{ when, } v_{in}(t) \geq v_0 \quad (5)$$

The ground voltage $V(t)$ is zero before the $V_{in}(t)$ attains V_0 . The above Eq. (5) can be simplified by assuming the ramp input voltage,

$$\frac{dv(t)}{dt} + \frac{V(t)}{NLK\gamma} = \frac{s_r}{\gamma} \quad t \geq t_0 \quad (6)$$

Eq. (6) is the first order differential equation. At the time $t = t_0$, the ground voltage is zero for the initial conditions. Eq. (6) can be solved to determine the time independent equation for SSN at the ground.

$$V(t) = NL s_r \left(1 - \frac{e^{-s_r(t-t_0)}}{\gamma NL s_r k} \right); t_0 \leq t \leq t_r \quad (7)$$

where, t_r represents the rise time of the input signal. The at most noise voltage is achieved when the input signal reaches V_{DD} which after simplification reads,

$$V_m = NL s_r k \left(1 - e^{-\frac{V_{DD}-V_0}{\gamma NL s_r k}} \right) \quad (8)$$

The time dependent current through the MOS can then be measured utilizing Eq. (3) and Eq. (7)

$$I_D(t) = K \left(s_r t - v_0 - \gamma NL s_r k \left(1 - \frac{e^{-s_r(t-t_0)}}{\gamma NL s_r k} \right) \right); t_0 \leq t \leq t_r \quad (9)$$

Moreover being accurate, the mathematical formulation for the maximum SSN voltage is very simple. A further look into Eq. (8) which defines a circuit related figure H, where,

$$H = NL s_r \quad (10)$$

Then, the Eq. (8) can be rewritten as,

$$V_m = HK \left(1 - e^{-(V_{DD}-V_0)/\gamma HK} \right) \quad (11)$$

Initially, it is experimented that the peak SSN is a function of H, a circuit related figure and the process related parameters such as γ , K, V_0 and V_{DD} . The design observation is that a circuit related figure H is the only variable that can be used in circuit design to control the SSN. Next, the circuit related figure H is simply a multiplication of three factors of N (number of identical drivers), L (parasitic inductance) and s_r which represents that changes in each of those three factors will have the same result on simultaneous switching noise. This examination is supportive in optimizing the bonding pad driver design.

The switching noise is modelled using Resistance (R), Inductance (L) and Capacitance (C) which represents the parasitic impedances of the power supply network. The switching circuit is symbolized by CMOS gates and saturated ramp signal as input with transition time t_r . When the transition time of input signal is short, the switching noise can continue to rise after the transition is complete. Thus, analysis of noise only within the transition period can drastically undervalue the peak noise under specific damping conditions. The noise amplitude at the source node of the NMOS transistor in Figure 3 are generated by CMOS inverter in a 45 nm process technology is examined. The ramp signal is used as the input signal to the inverter.

4. SIMULATION RESULTS AND DISCUSSION

The performance of the proposed noise reduction circuit is realized and the simulations are carried out in the Tanner EDA (Version 14.1) and the synthesis results are estimated in the Spice simulation with 45 nm technology file from T Spice. The simulation parameters are listed in the Table 1. The SSN in the frequency domain is addressed by the spectral peak reduction. There are many numbers of clock buffers stages are introduced in the clock scheduling. The parasitic impedance (R, L and C) based noise reduction circuit is used to minimize the switching noise in the mixed signal ICs. The proposed Input/Output model is as shown in Figure 1. It can be used as buffer in the input port. With this circuit, the effect of V_{DD} and ground noise is analyzed along with the power variation due to V_{DD} . Figure 2 shows the schematic model of proposed noise reduction circuit.

Table 1. Simulation parameters for the proposed noise reduction circuit

Parameters	Specifications
Transistor Level Tool	Tanner EDA 14.1
Functional Simulator	Spice
Library File	45 nm Tech file from T-Spice
Wave Nature	Ramp
Frequency	8 MHz
Power Supply Voltage	5 V

To examine the consequence of number of switching gates on noise power, it is constructed with three inverter pairs along with pull up network. Proposed equivalent circuit model with noise reduction circuit is shown in Figure 3. For different values of R, L and C, the proposed circuit is simulated and the results are analyzed and compared with the existing circuit design. Figure 4 shows the transient response of the proposed circuit. For the betterment of analysis and measurement, the magnified view of Figure 4 is shown in Figure 5. The noise

does not attain the first local maximum within the transition when the transition time is shorter.

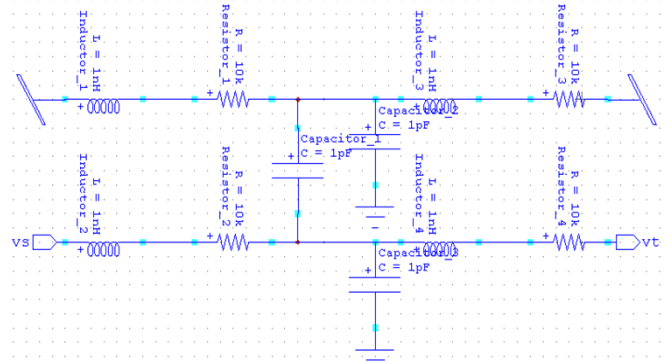


Figure 1. Schematic of input / output driver

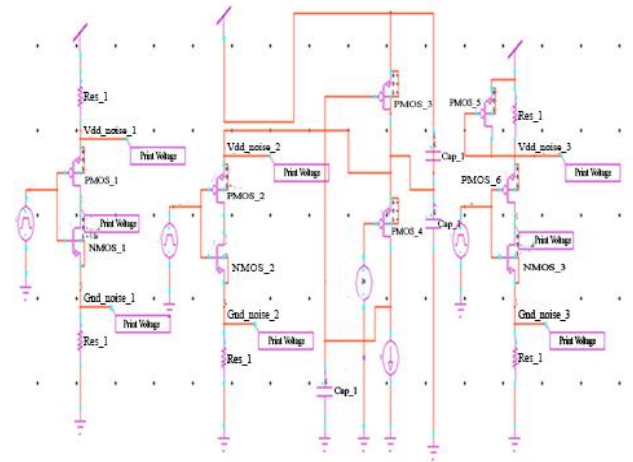


Figure 2. Schematic of noise reduction circuit

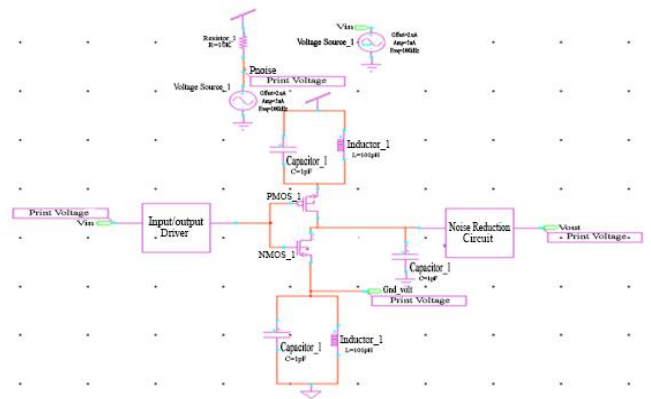


Figure 3. Proposed equivalent circuit model with noise reduction circuit

The peak noise would always happen after the transition period. Since the system reacts to the step function with natural response, when the input transition time is satisfactorily short, it is again accepted that the peak noise would occur after the transition period. The transition period is configured by using R, L and C parasitic impedances. Two important transient circuit characteristics need to be found from the transition period are noise at the end of transition and the current flowing through the capacitance. Since the current flowing through the PMOS transistor is very small, it is negligible. N is the parameter used to represent the effective number of

Input/Output gates when a large number of Input/Output drivers are in parallel, which switches simultaneously.

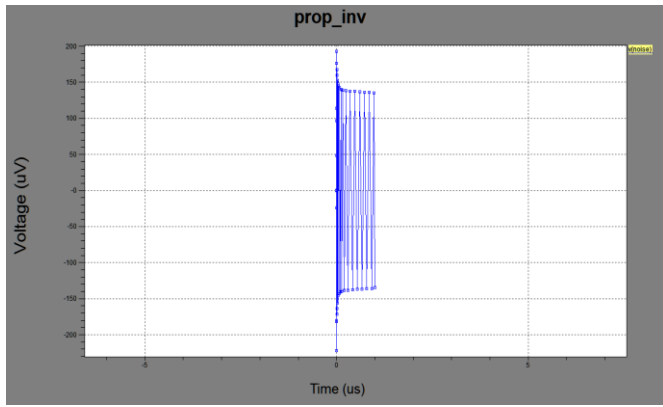


Figure 4. Transient response of proposed circuit

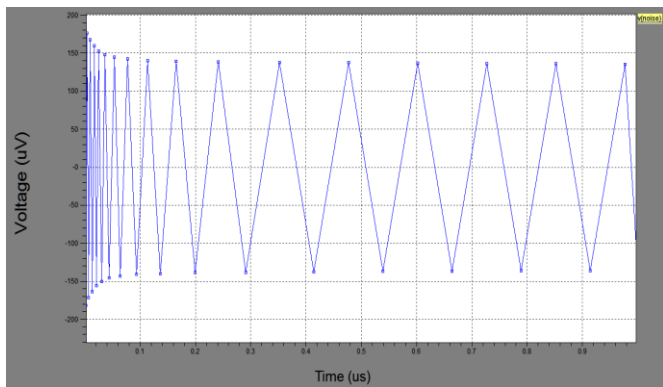


Figure 5. Transient response of proposed circuit-magnified

The result of signal transition time on the peak noise characteristics can be examined through the proposed circuit. For the value of $R=0.5 \text{ ohm}$, $L=100 \text{ pH}$ and $C=5 \text{ pF}$, transient response of proposed and existing circuit are compared and they are shown in Figure 6. For the value of $R=0.5 \text{ ohm}$, $L=100 \text{ pH}$ and $C=5 \text{ pF}$, the proposed circuit is simulated and noise value measured is $140 \text{ }\mu\text{V}$. Figure 7 shows the transient

response comparisons between existing and proposed circuit for another sample value of $R=1 \text{ ohm}$, $L=100 \text{ pH}$ and $C=5 \text{ pF}$. The noise value reported for the proposed circuit is $100 \text{ }\mu\text{V}$ where as it is 7.5 mV for the existing circuit. Table 2 shows the results comparisons between the existing and proposed works for two different values of R , L and C .

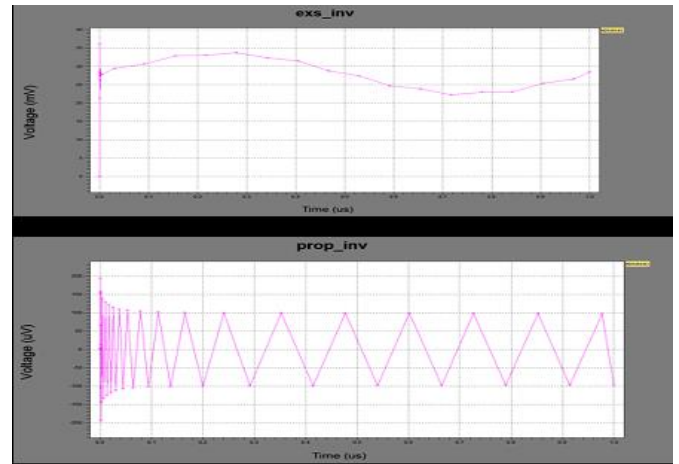


Figure 6. Transient response of existing vs proposed circuit for $R=0.5 \text{ }\Omega$, $L=100 \text{ pH}$ and $C=5 \text{ pF}$

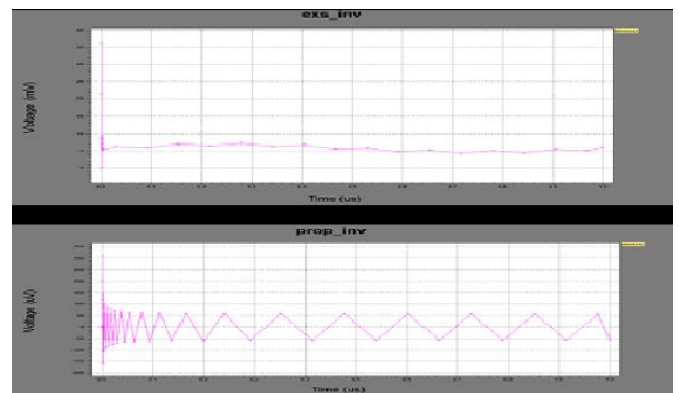


Figure 7. transient response of existing vs proposed circuit for $R=1 \text{ }\Omega$, $L=100 \text{ pH}$ and $C=5 \text{ pF}$

Table 2. Results comparison

Parasitic Impedances			Existing Work [21]			Proposed Work		
R (Ω)	L (pH)	C (pF)	Peak Noise (mV)	Frequency (MHz)	Max. Power Consumed (mW)	Peak Noise (μV)	Frequency (MHz)	Max. Power Consumed (mW)
0.5	100	5	33	8	0.07879455	140	8	10.23433
1	100	5	29	8	0.07879466	100	8	10.23430

As the proposed noise reduction circuit has reported minimum switching noise as compared with the existing circuit, it is deployed in adder circuit and ALU for noise, transistor count and power analysis. The GDI technique is implemented to reduce the number of transistor counts. This technique allows execution of wide range of complex logic functions using minimum number of transistors. Also, it is suitable for design of fast, low power circuits using minimum transistors, less delay and area.

The GDI cell consists of three inputs namely, G - Common gate input of NMOS and PMOS, P - Input to the source / drain of PMOS and N - Input to the source / drain of NMOS. The major advantages of GDI over Pass Transistor Logic (PTL) and other standard CMOS design are: 1) Due to the small node

capacitances high speed is achieved 2) As a result of the reduced number of transistors for implementing a function it requires low power, and 3) Lower interconnection effects, due to technology scaling.

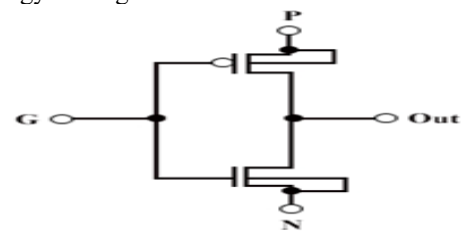


Figure 8. GDI basic cell

Figure 8 shows the GDI basic cell structure. Table 3 shows the different logic functions of GDI cell for various input configuration. A half adder performs addition of two input (A and B) bits and produces the Sum (S) and Carry (C). The input variables of a half adder are called the Augends and Addend bits. The output variables are designated as the Sum (S) and Carry (C).

Table 3. GDI logic table

N	Input P	G	Output	Function
0	B	A	A' B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Figure 9 and Figure 10 show the schematic of existing half adder circuit design and transistor count respectively.

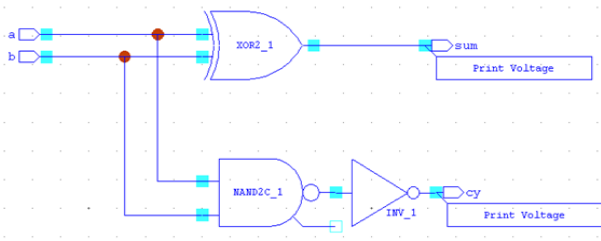


Figure 9. Schematic of existing half adder design

```

Device and node counts:
MOSFETs - 21
BJTs - 0
MESFETs - 0
Capacitors - 0
Inductors - 0
Transmission lines - 0
Voltage sources - 3
VCVS - 0
CCVS - 0
V-control switch - 0
Macro devices - 0
Subcircuits - 0
Model Definitions - 2
Independent nodes - 11
Total nodes - 15

MOSFET geometries - 2
JFETs - 0
Diodes - 0
Resistors - 0
Mutual inductors - 0
Coupled transmission lines - 0
Current sources - 0
VCCS - 0
CCCS - 0
I-control switch - 0
Verilog-A devices - 0
Subcircuit instances - 5
Computed Models - 2
Boundary nodes - 4

```

Figure 10. Transistor count of existing half adder design

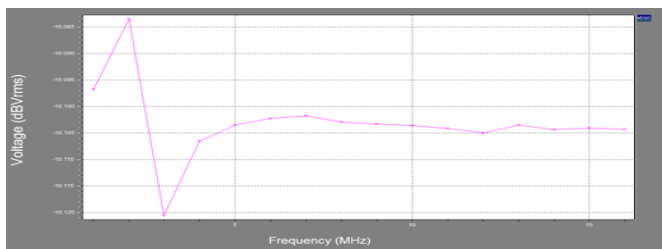


Figure 11. Noise waveform of existing half adder

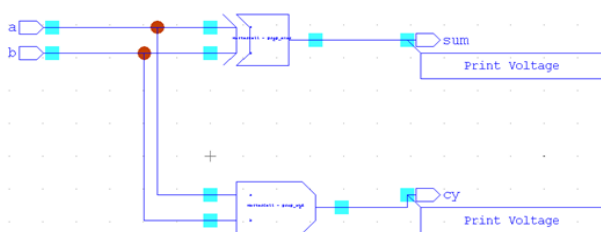


Figure 12. Schematic of proposed half adder design

```

Device and node counts:
MOSFETs - 11
BJTs - 0
MESFETs - 0
Capacitors - 0
Inductors - 0
Transmission lines - 0
Voltage sources - 3
VCVS - 0
CCVS - 0
V-control switch - 0
Macro devices - 0
Subcircuits - 0
Model Definitions - 2
Independent nodes - 5
Total nodes - 9

MOSFET geometries - 3
JFETs - 0
Diodes - 0
Resistors - 0
Mutual inductors - 0
Coupled transmission lines - 0
Current sources - 0
VCCS - 0
CCCS - 0
I-control switch - 0
Verilog-A devices - 0
Subcircuit instances - 5
Computed Models - 2
Boundary nodes - 4

```

Figure 13. Transistor count of proposed half adder design

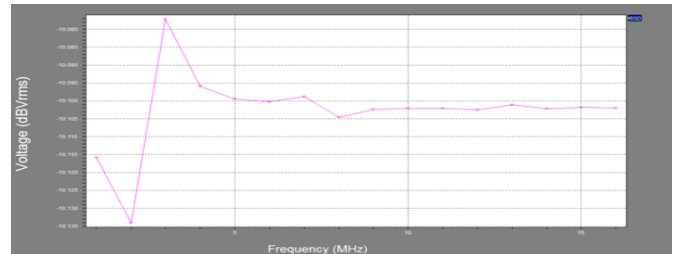


Figure 14. Noise waveform of proposed half adder

Figure 11 shows the noise waveform of the existing circuit design with peak noise of -10.083 dBV_{rms}. Similarly, Figure 12 and Figure 13 show the proposed half adder circuit design with GDI technique and the corresponding transistor count respectively. Figure 14 shows the noise waveform of the existing circuit design with peak noise of -10.077 dBV_{rms}. Table 4 shows the result comparisons between the existing and proposed GDI half adder design.

Table 4. Results comparison of existing and proposed half adder

Parameters	Existing Design [22]	Proposed Design
No. of Transistors	21	11
Maximum Power Utilizations (mW)	4.456427	2.951001
Peak Noise (dBV _{rms})	-10.083	-10.077
Frequency (MHz)	2	3
Input Voltage (V)	5	5
Temperature (°C)	25	25

ALU is the heart of all microprocessors/microcontrollers core of a CPU in a computer. It is a logic unit that performs its arithmetic, logic and shift operations. The adder cell is the basic unit of an ALU. The constraints the adder has to satisfy are power, speed and area requirements. Now-a-days the size of ALU is getting smaller and more complex to enable the development of more powerful but smaller smart computers. Though there are few limiting factors that slow down the advancement of smaller and more complex ICs and due to integrated circuit design, engineering cost, fabrication technology and productivity.

Figure 15 and Figure 16 show the noise amplitude and the transistor count of existing ALU design. The proposed noise reduction circuit is shown in Figure 2 has reported minimum switching noise as compared with the existing circuit and it is deployed in the 4 bit ALU for noise, transistor count and power analysis with GDI technique. Figure 17 shows the schematic of proposed GDI 4-bit ALU. Similarly, Figure 18 and Figure 19 show the noise amplitude and the transistor

count of proposed design. Table 5 shows the result comparisons of existing and proposed ALU Design.

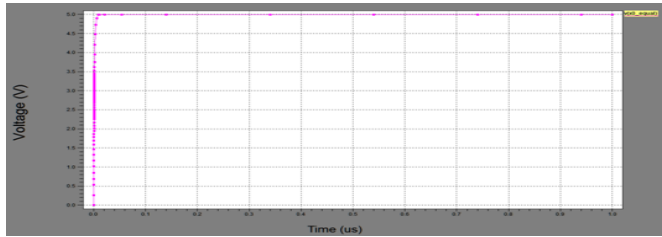


Figure 15. Noise amplitude of existing ALU design

Device and node counts:	
MOSFETs - 910	MOSFET geometries - 8
BJTs - 0	JFETs - 0
MESFETs - 0	Diodes - 0
Capacitors - 2	Resistors - 0
Inductors - 0	Mutual inductors - 0
Transmission lines - 0	Coupled transmission lines - 0
Voltage sources - 28	Current sources - 0
VCCS - 0	VCCS - 0
CCVS - 0	CCCS - 0
V-control switch - 0	I-control switch - 0
Macro devices - 0	Verilog-A devices - 0
Subcircuits - 0	Subcircuit instances - 167
Model Definitions - 2	Computed Models - 2
Independent nodes - 434	Boundary nodes - 29
Total nodes - 463	

Figure 16. Transistor count of existing ALU design

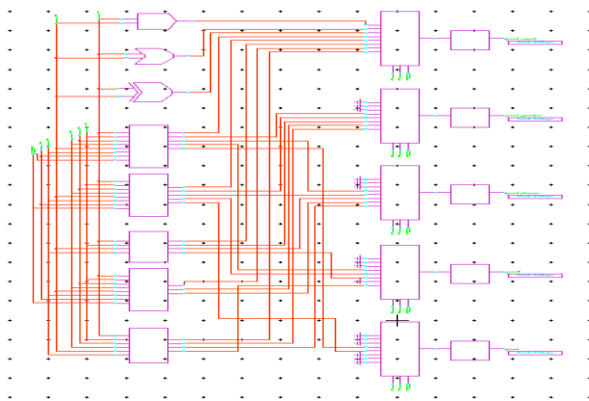


Figure 17. Schematic of proposed ALU design

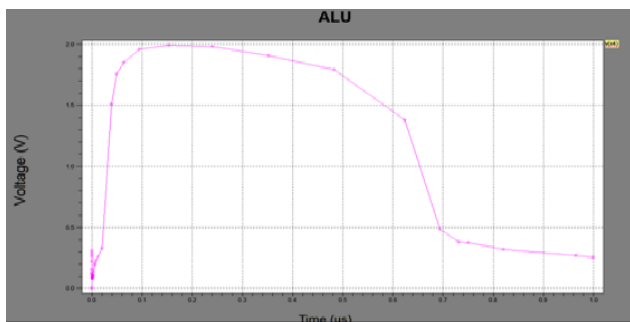


Figure 18. Noise amplitude of proposed ALU design

Device and node counts:	
MOSFETs - 657	MOSFET geometries - 8
BJTs - 0	JFETs - 0
MESFETs - 0	Diodes - 0
Capacitors - 15	Resistors - 25
Inductors - 0	Mutual inductors - 0
Transmission lines - 0	Coupled transmission lines - 0
Voltage sources - 17	Current sources - 5
VCCS - 0	VCCS - 0
CCVS - 0	CCCS - 0
V-control switch - 0	I-control switch - 0
Macro devices - 0	Verilog-A devices - 0
Subcircuits - 0	Subcircuit instances - 260
Model Definitions - 2	Computed Models - 2
Independent nodes - 2967	Boundary nodes - 18
Total nodes - 2985	

Figure 19. Transistor count of proposed ALU design

Table 5. Results comparison of existing and proposed ALU design

Parameters	ALU Design using CMOS Design	ALU Design using GDI Design
No. of Transistors	910	657
Maximum Power Utilizations (mW)	92.4	45.84
Peak Noise (V)	5	2

5. CONCLUSION

The noise reduction circuit is proposed, constructed and simulated. The simulated circuit's results are compared with the existing technique. For the value of $R=0.5$ ohm, $L=100$ pH and $C=5$ pF noise value measured for the proposed noise reduction circuit is $140 \mu\text{V}$ whereas it is 33 mV for the existing circuit. This noise reduction circuit is implemented in GDI based half adder circuit and simulated. The peak noise and the number of transistors required for the proposed half adder design is $-10.077 \text{ dBV}_{\text{rms}}$ and 11 transistors, whereas for the existing half adder design it is $-10.077 \text{ dBV}_{\text{rms}}$ and 21 transistors respectively. Similarly the power utilization of the proposed design is 2.95 mW whereas it is 4.45 mW for the existing design. Finally, the noise reduction circuit is implemented in GDI based 4 bit ALU and simulated. The proposed 4 bit ALU has reduced peak noise of 2 V whereas it is 5 V for the existing design. That is, 60 % reduction in peak noise is achieved by the proposed circuit. Similarly, number of transistors required for the proposed design is well reduced from 910 to 657 transistors compared to existing design. The power consumption for the proposed design is only 45.84 mW whereas it is 92.4 mW in existing method. Therefore, nearly 50% reduction of power consumption has been achieved by the proposed design.

6. LIST OF ACRONYMS

- ALU-Arithmetic Logic Unit
- BM-Binary Multiplier
- CMOS-Complementary Metal Oxide Semiconductor
- CPU-Central Processing Unit
- EDA-Electronic Design Automation
- GDI-Gate Diffusion Input
- IC-Integrated Circuit
- PSN-Power Supply Noise
- PTL-Pass Transistor Logic
- RCA-Ripple Carry Adder
- SoC-System on Chip
- SSN-Simultaneous Switching Noise
- VDSM-Very Deep Sub Micrometer
- VLSI-Very Large Scale Integration

REFERENCES

- [1] Mezhiba AV, Friedman EG. (2004). Scaling trends of on-chip power distribution noise. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 12(4): 386-394. <https://doi.org/10.1109/tvlsi.2004.825834>
- [2] Wang CL, Tao YG, Yang P, Liu ZJ. (2017). Dimension reduction and feedback stabilization for max-plus linear systems and applications in VLSI array processors. IEEE

- Transactions on Automatic Control 62(12): 6353-6368. <https://doi.org/10.1109/TAC.2017.2708508ss>
- [3] Scotti G, Bellizia D, Trifiletti A, Palumbo G. (2017). Design Of Low-Voltage High-Speed CML D-Latches In Nanometer CMOS technologies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25(12): 3509-3520. <https://doi.org/10.1109/TVLSI.2017.2750207>
- [4] Bait Suwailam MM, Ramahi OM. (2012). Ultrawide-band mitigation of simultaneous switching noise and EMI reduction in high speed PCBs using complementary split ring resonators. IEEE Transactions on Electromagnetic Compatibility 54(2): 389-396. <https://doi.org/10.1109/temc.2011.2163940>
- [5] Jia YT, Zhang DL, Zhang B. (2015). Slit-surface disturbance lattice ebg structure for simultaneously switching noise suppression in high speed data acquisition system. IEEE Transactions on Components, Packaging and Manufacturing Technology 5(1): 86-98. <https://doi.org/10.1109/TCPMT.2014.2376875>
- [6] Mandal JK, Mukhopadhyay S. (2012). A novel technique of filtering high random valued impulse noise and optimization through genetic algorithm (HRVINGA). AMSE Journals, France, Series: Advances B 55(1).
- [7] Barik RK, Pradhan M. (2015). Area-time efficient square architecture. AMSE Journals, France, Series Advances D 20(1): 21-34.
- [8] Bikshalu K, Reddy VSK, Reddy PCS, Rao KV. (2014). Electro deposition of nano crystalline La₂O₃ on p-type Si wafer and electrical characterization for CMOS applications. AMSE Journals, France, Series: Modelling A 87(3): 1-9.
- [9] Seenuvasamurthi S, Nagarajan G. (2017). Power supply noise reduction circuit for mixed signal VLSI systems. International Journal of Digital Signal Processing 9(2): 26-30.
- [10] Seenuvasamurthi S, Nagarajan G. (2017). Power supply noise reduction in mixed signal system on-chip with active decoupling inductor. International Journal of Digital Signal Processing 9(2): 17-25.
- [11] Tapari A, Banerjee B, Viswanathan TR. (2011). CS-CMOS: A low-noise logic family for mixed signal SoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 19(12): 2141-2148. <https://doi.org/10.17577/IJERTV5IS010510>
- [12] Seenuvasamurthi S, Nagarajan G. (2016). Highly stable power efficient, noise tolerant circuits for analog and digital systems. IEEE Sponsored, 10th International Conference on Intelligent Systems and Control (ISCO'16), Karpagam College of Engineering, Coimbatore, India (1): 134-139. <https://doi.org/10.1109/ISCO.2016.7727040>
- [13] Mohammad BS, Saleh H, Ismail M. (2015). Design methodologies for yield enhancement and power efficiency in SRAM based SoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 23(10): 2054-2064. <https://doi.org/10.1109/TVLSI.2014.2360319>
- [14] Bhattacharyya P, Kundu B, Ghosh S, Kumar V, Dandapat A. (2015). Performance analysis of a low power, high speed hybrid 1-bit full adder circuit. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 23(10): 2001-2008. <https://doi.org/10.1109/TVLSI.2014.2357057>
- [15] Badaroglu M, Wambacq P, Van der Plas G, Donnay S, Gielen GGE, De Man HJ. (2005). Digital ground bounce reduction by supply current shaping and clock frequency modulation. IEEE Transaction on Computer Aided Design of Integrated Circuits Systems 24(1): 65-76. <https://doi.org/10.1109/tcad.2004.839471>
- [16] Wang HL, Salman E. (2015). Decoupling capacitor topologies for TSV-based 3-D ICs with power gating. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 23(12): 2983-2991. <https://doi.org/10.1109/TVLSI.2014.2386253>
- [17] Chang NCJ, Hurst PJ, Levy BC, Lewis SH. (2014). Background adaptive cancellation of digital switching noise in a pipelined analog-to-digital converter without noise sensors. IEEE Journal of Solid-State Circuits 49(6): 1397-1407. <https://doi.org/10.1109/JSSC.2014.2314446>
- [18] Li CF, Chou SC, Ke GH, Huang PC. (2012). A power efficient noise suppression technique using signal-nulled feedback for low-noise wideband amplifiers. IEEE Transactions on Circuits and Systems 59(1): 1-5. <https://doi.org/10.1109/tcsii.2011.2177695>
- [19] Zhao SY, Roy K, Koh CK. (2002). Decoupling capacitance allocation and its application to power-supply noise-aware floor planning. IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems 21(1): 81-92. <https://doi.org/10.1109/43.974140>
- [20] Seenuvasamurthi S, Nagarajan G. (2017). A low noise and power efficient 45nm GPDK technology based highly stable current balancing logic (HCBL) and dynamic logic circuits for mixed signal systems. Association for the Advancement of Modelling and Simulation Techniques in Enterprises (AMSE), France, Series: Advances C 72(1): 11-24, Feb. 2017
- [21] Wang HL, Salman E. (2016). Closed-form expressions for I/O simultaneous switching noise revisited. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25(2): 769-773. <https://doi.org/10.1109/TVLSI.2016.2584387>
- [22] Morgenshtein A, Fish A, Wagner IA. (2002). Gate-diffusion input (GDI): A power efficient method for digital combinatorial circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 10(5): 566-581. <https://doi.org/10.1109/TVLSI.2002.801578>
- [23] Chandra N, Yati AK, Bhattacharyya AB. (2009). Extended-sakurai-newton MOSFET model for ultra-deep-submicrometer CMOS digital design. 22nd International Conference on VLSI Design, New Delhi, India: 247-252. <https://doi.org/10.1109/VLSI.Design.2009.48>