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A High Gain, Low Power and Low Noise down Conversion Mixer Using 0.18 µm CMOS Process

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Abstract

This paper presents a down conversion mixer design with high gain, low power and low noise. Here, a combination of bulk injection technique, switched biasing technique and current bleeding technique is used for this mixer design. This is simulated in cadence tool using 0.18 µm CMOS process. The bulk injection technique enhances the conversion gain of the mixer with a noisy drain current. This noise is reduced by the use of switched biasing technique with a dc level shifter. The current bleeding technique is used to reduce the effect of parasitic capacitance, which results in progress of conversion gain and also improves the mixer noise. The proposed mixer produces a simulated conversion gain of 11 dB with a noise figure (NF) of about 8.1 dB and the third order input intercept point (IIP3) of 10.8 dBm. The power consumed by the circuit is 0.5 mW from 1.8 V supply voltage.

Key words

Bulk injection, Current bleeding, DC level shifter, Gilbert mixer, Noise figure.

1. Introduction

In recent deep-submicron process, digital and analog design faces several new challenges. The design of analog and radio frequency (RF) circuits are more demanding due to the reducing

supply voltages. The CMOS technology grades an enhancement in operation speed, power consumption and area of the integrated circuit. The integration of the RF front end and base band digital function in a single chip depends upon the CMOS technology. The RF front end consists of all the components in the receiver, which processes the signal at the incoming RF, before it is changed into a lower intermediate frequency (IF). The linearity of transmitter is dominated by the mixer [1] due to the cascade structure of RF front end. Therefore, a mixer with good linearity is required to further improve the lively range of the RF front end. A mixer translates one frequency to another frequency by maintaining phase information and signal amplitude [2]. Either a sum or a difference frequency (IF signal) at a single output terminal is obtained, when two different signal frequencies (RF signal and local oscillator (LO) signal) are inserted into other two terminals. The Fig.1 shows the down conversion system, where the input frequency is higher than the output frequency by the process of mixing. In radio frequency integrated circuit (RFIC) design, the more popular active double balanced mixer is Gilbert type mixer [3]. It is widely used in CMOS transceiver system for its compact layout, high linearity, high conversion gains and good port to port isolation. However, this has also certain drawbacks like high supply voltage and high power consumption requirements. So different techniques including folded technique, bulk injection technique, current bleeding technique, charge injection technique and switched biasing technique are applied for operation in low supply voltage and to consume less power.

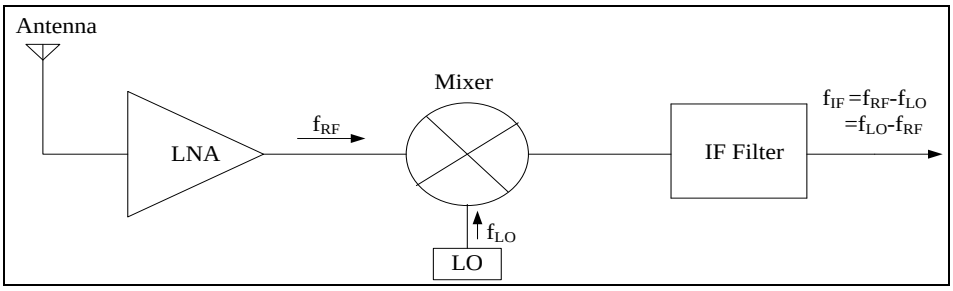

Fig.1. Down Conversion System

The folded technique [4] reduces the supply voltage, due to the use of less stacked layers of transistors, and dc power consumption. But due to the use of inductor in the matching network, the chip area is more and the bandwidth is less. The switched biasing technique [5] lowers noise originating at tail current transistors. But it needs high supply voltages due to the more number of stacked transistors tending to high power consumption. In bulk driven concept [6] the supply voltage is low as the number of stacked transistor are less, producing less power consumption. Here, RF signal is inserted directly through the body terminal providing more noise current. A low power and high gain mixer [7] is obtained when transistors operate in subthreshold region

with an active load. But, more noise is added to the system due to the large aspect ratio of transistors. In bulk injection technique [8], PMOS transistor acts as an active load which provides high output impedance. Hence, the current flow through the mixer core is less resulting low supply voltage operation. But it results low conversion gain and relatively high noise figure. The bulk pumped mixer [9] achieves low supply voltage and low power consumption due to the use of less number of stacked transistors, where the conversion gain is poor. Both bulk injection and switched biasing techniques [10] achieve flat conversion gain, low supply voltage, low power consumption and improvement in noise figure, but result low isolation and high LO power requirement. The current bleeding technique [11-13] improves the noise figure, linearity [14] and power conversion gain of the mixer. However, in this case the chip area is more due to the use of inductor in the matching network.

In this work, the design of the proposed mixer is followed by bulk injection technique, switched biasing technique and current bleeding technique to achieve high gain, low power and low noise figure in 0.18 µm CMOS technology. The mixer circuit operates at a 1.8 V supply voltage with a power consumption of 0.5 mW. The conversion gain for this mixer is 11 dB and it achieves the noise figure of 8.1 dB. The layout design of the proposed mixer is also presented in this work.

2. CMOS Mixer Design and Performance Analysis

2.1 Bulk Injection, Switched Biasing and Current Bleeding Technique Based Mixers

In bulk injection technique based mixer, the bulk voltage is smaller than the threshold voltage of the device. Hence, the circuit operates at low voltage and consumes less power [9]. The LO signal modulates the threshold voltage as a function of voltage between bulk and source (VBS) [8] as expressed in equation (1).

$$V_{TH(LO)} = V_{T0} + \gamma\sqrt{2\varphi_F - V_{BS(LO)}} - \gamma\sqrt{2\varphi_F} \quad (1)$$

where, V_{T0} is the zero substrate bias threshold voltage, γ is the body effect factor and φ_F is the surface potential. This technique eliminates the parasitic capacitance of the Gilbert type mixer to achieve a higher conversion gain, which is expressed in equation (2) and (3), respectively [10].

$$A_{V,Gilbert} \approx \frac{2}{\pi} g_m \frac{g_{mLO}}{g_{mLO} + J\omega C_P} \tag{2}$$

$$A_{V,\ Bulk\ injection} \approx \frac{2}{\Pi} g_m Z_L \tag{3}$$

where, g_{mLO} and g_m are the transconductance of the LO and RF stage respectively, and Z_L is the load impedance and C_P denotes the shunt parasitic capacitance.

In switched biasing technique based mixer, the tail current source is divided into two half size transistors to operate in between accumulation and strong inversion region. By this act, releasing of trapped charge carriers lowers the flicker noise [15]. There is a reduction in flicker noise and LO switching noise in current bleeding technique based mixer [16-18].

2.2 Proposed CMOS Mixer Description

The proposed mixer which incorporates bulk injection technique, switched biasing technique and current bleeding technique is displayed in Fig.2. The mixer consists of four major parts: bulk injection core stage (M3-M6), switched biasing stage (M1-M2), the active load stage (M7-M8) and current bleeding stage (M9-M10). The bulk injection core stage is an integration of conventional RF transconductance stage and LO switching stage.

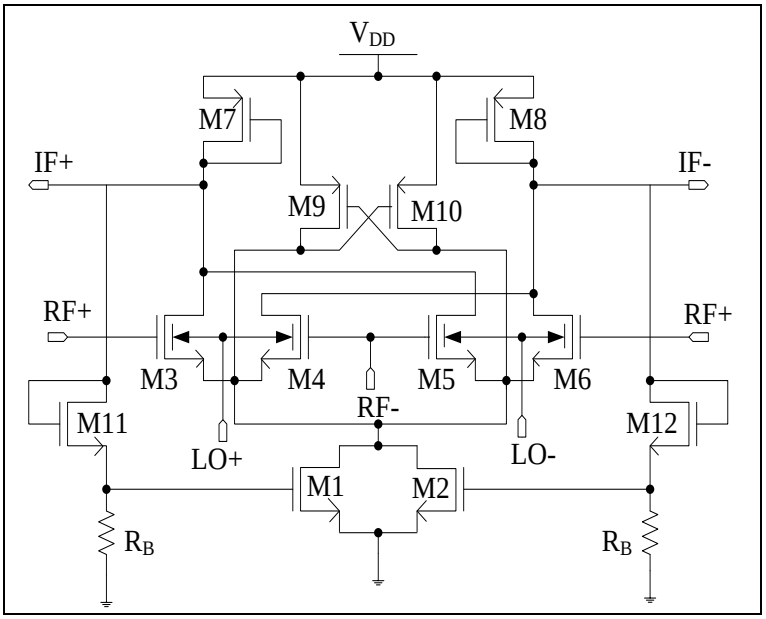

Fig.2. The Proposed Mixer

The integration of two stages into one reduces the number of stacked transistors from six to four. So that the circuit operates at reduced supply voltage. Here, RF and LO inputs are inserted

to the core transistors (M3-M6). The voltage to current conversion takes place by the RF stage where all transistors operate in sub-threshold region. This results in low noise figure and high conversion gain. In 0.18 μm CMOS process, the gate voltage of the core transistors is taken as less than 0.5 V, which is the typical value of threshold voltage (VTH). As the threshold voltage is modulated by the LO signal as per equation (1), no dc current flow through the transistors (M3-M6) due to the turn off condition of the switching stage. As a result, core transistors consume less power.

The switched biasing stage acts as a tail current source which is used to solve the nosier drain current problem as observed in bulk injection technique. Here, the tail current source divides into two half size transistors (M1-M2) which are alternately switched by IF output signals through the dc level shifter (M11, M12 and RB). This switching makes transistors (M1-M2) to operate between strong inversion and accumulation regions and randomly trapped charge carriers are released. This lowers the flicker noise. The dc level shifter provides proper gate to source voltage of (M1-M2) transistors to make the overdrive voltage very small. Therefore, the symmetric switch operation is obtained with small output swing. To reduce the noise figure, (M1-M2) transistors are suitably selected with a small overdrive voltage.

The current to voltage conversion for the IF output signal takes place due to the high output impedance of the active load stage consists of PMOS transistors (M7-M8). Though the noise performance of mixer is poor due to active load, there is an improvement in power consumption.

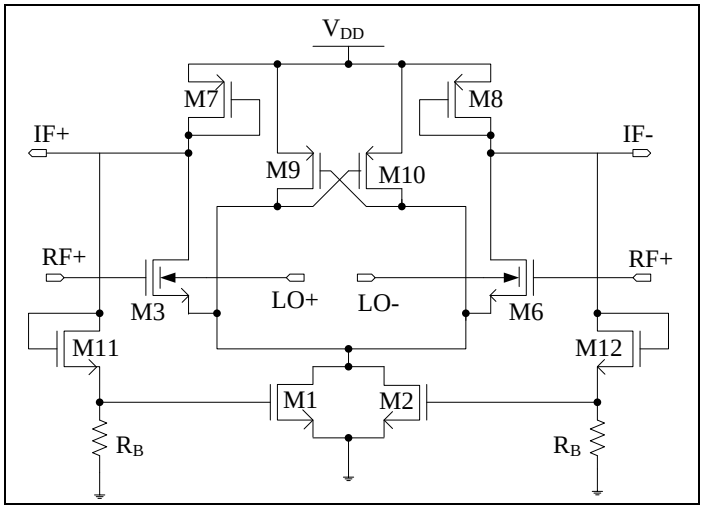

Fig.3(a). The Proposed Mixer when M3 and M6 are ON

The current bleeding stage (M9-M10) is used to maintain the total current of the mixer but reduces the LO current and professionally lowers the switching noise. But indirectly the noise figure is degraded due to the larger value of parasitic capacitance present at the source of the LO

stage. So the appropriate size of transistors in the switching stage and current bleeding stage are selected to diminish this effect. The proposed mixer works on a switched current principle so that the switches change their position in every clock cycle. The transistors M3 and M6 are on and M4 and M5 are off, which is shown in Fig.3(a) during the first cycle.

The Fig.3(b) shows the transistors M4 and M5 are on and M3 and M6 are off during the second cycle. In order to specify the circuit design principle, the analysis is focused on conversion gain and noise figure.

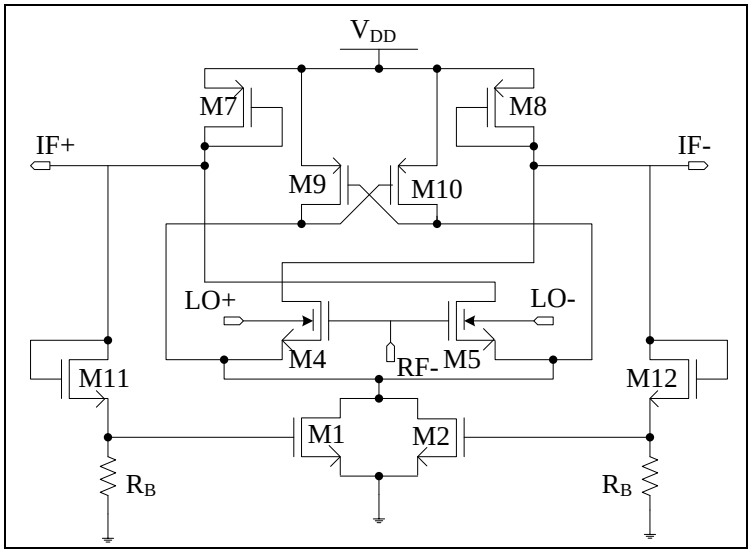

Fig.3(b). The Proposed Mixer when M4 and M5 are ON

2.2.1 Conversion Gain

The conversion gain is the ratio between the desired IF signal (IF = RF - LO) and the RF signal. The equivalent small signal model [19-20] of the proposed mixer is shown in Fig.4(a-c). Here, all PMOS and NMOS transistors are identical to each other.

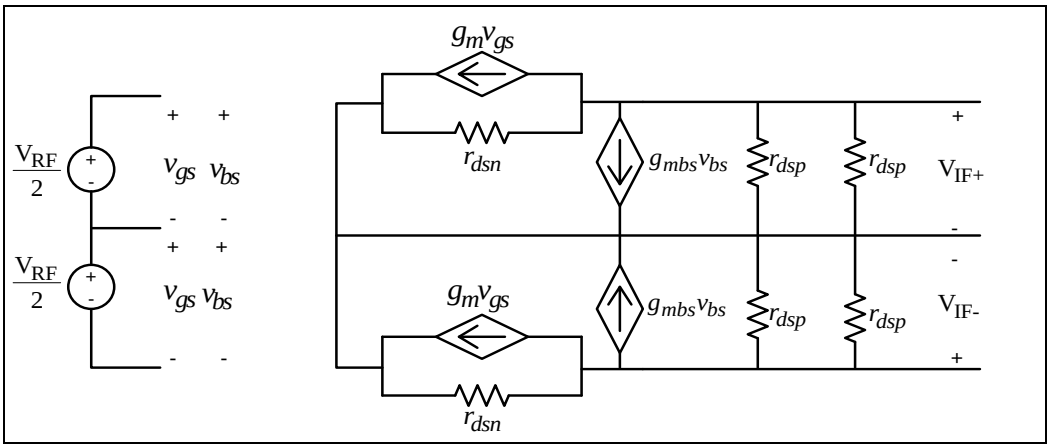

Fig.4(a). Small Signal Model of Proposed Mixer

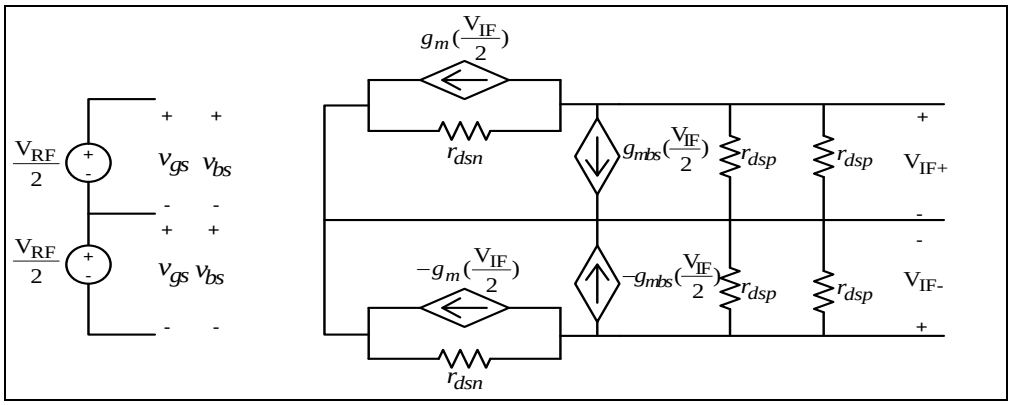

Fig.4(b). Equivalent Small Signal Model of Proposed Mixer

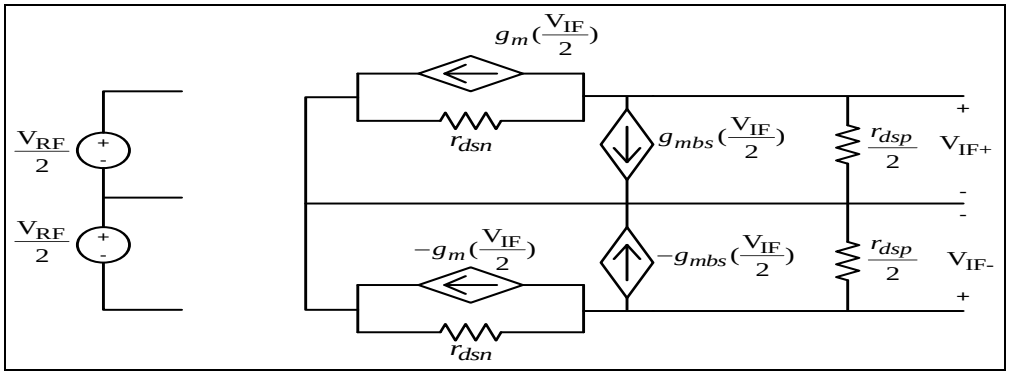

Fig.4(c). More Equivalent Small Signal Model of Proposed Mixer

Further, simplified equivalent small signal model as shown in Fig.4(d) is derived and the conversion gain is calculated as follows.

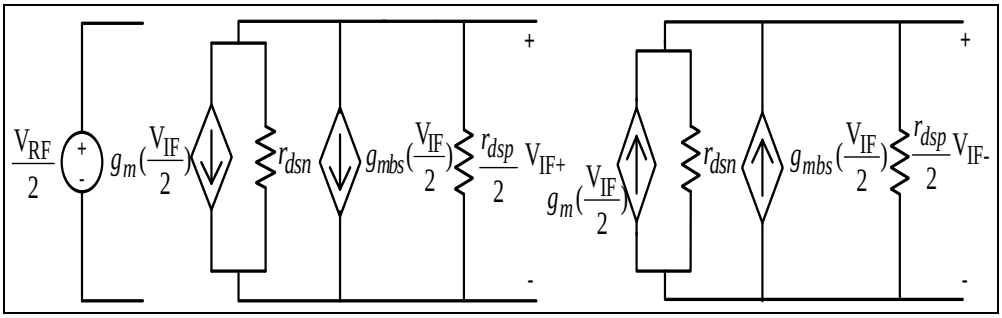

Fig.4(d). Simplified Small Signal Model of Proposed Mixer

$$V_{IF+} = -\left(g_m + g_{mbs}\right)\frac{V_{IF}}{2}\left(r_{dsn} \parallel \frac{r_{dsp}}{2}\right)$$

$$\Rightarrow V_{IF+} = -\left(g_m + g_{mbs}\right)\frac{V_{IF}}{2}\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)$$

$$\Rightarrow \frac{V_{IF+}}{V_{IF}} = -\frac{1}{2}\left(g_m + g_{mbs}\right)\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right) \quad (4)$$

Similarly

$$\frac{V_{IF-}}{V_{IF}} = \frac{1}{2}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right) \quad (5)$$

So the voltage gain (AV) or (G) of the proposed mixer is given as

$$A_V = \frac{V_{OUT}}{V_{IF}} = \frac{(V_{IF-})-(V_{IF+})}{V_{IF}} \quad (6)$$

By putting the value of equation (4) and equation (5) in above equation (6), it results

$$A_V = \frac{1}{2}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right) - \left(-\frac{1}{2}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)\right)$$

$$\Rightarrow A_V = \frac{1}{2}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right) + \frac{1}{2}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)$$

Finally the voltage gain (G) is as follows:

$$A_V = (g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right) \quad (7)$$

The conversion gain (CG) of the proposed mixer is given as

$$CG = \frac{2}{\pi}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)$$

$$CG = 20\log\left(\frac{2}{\pi}(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)\right) \text{ dB} \quad (8)$$

where, g_m, g_{mbs} and r_{dsn} are the transconductance, the body to substrate transconductance and the drain to source resistance of the bulk injection core stage respectively and the r_{dsp} is the resistance of active load stage.

The conversion gain of the proposed mixer is calculated as per equation (8) and found to be 11.66 dB.

2.2.2 Noise Figure

Noise figure is defined as the ratio of SNR at IF port to the SNR at the RF port and is expressed as:

$$\text{NF} = \frac{\text{Noise output of actual receiver}}{\text{Noise output of ideal receiver}}$$

$$NF = \frac{N_o}{GN_i} = \frac{N_o}{GKT_oB}$$

$$NF = \frac{GKT_oB + N_R}{GKT_oB} \quad (9)$$

By putting the value of gain of equation (7) in equation (9), we get

$$NF = \frac{(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)KT_oB + N_R}{(g_m + g_{mbs})\left(\frac{r_{dsn}r_{dsp}}{2r_{dsn}+r_{dsp}}\right)KT_oB}$$

$$NF = \frac{(g_m + g_{mbs})r_{dsn}r_{dsp}KT_oB + N_R(2r_{dsn}+r_{dsp})}{(g_m + g_{mbs})r_{dsn}r_{dsp}KT_oB} \quad (10)$$

Finally the expression for Noise Figure is expressed as

$$NF = \frac{(g_m + g_{mbs})r_{dsn}r_{dsp} + \frac{N_R}{Ni}(2r_{dsn}+r_{dsp})}{(g_m + g_{mbs})r_{dsn}r_{dsp}} \quad (11)$$

where, N_i = Available noise power at input and N_o = Available noise power at output

3. Simulation Results

The proposed down conversion mixer is implemented in cadence tool using 0.18 µm CMOS process. The schematic of the proposed design is shown in Fig. 5.

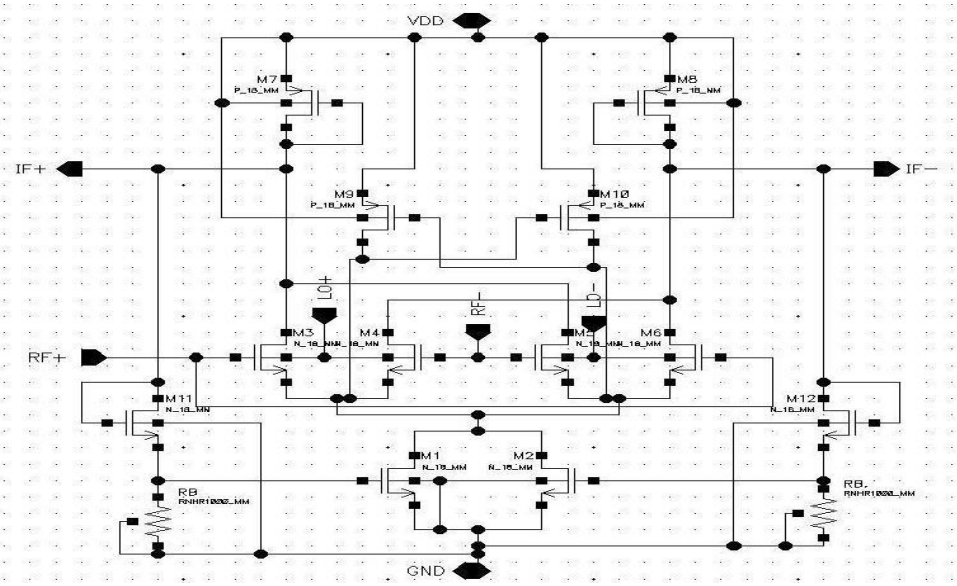

Fig.5. Schematic of Proposed Mixer

The design parameters such as conversion gain, noise figure and IIP3 are simulated at LO power of 5 dBm with the RF frequency of (1-10) GHz. The transient analysis of the proposed circuit is shown in Fig.6, in which the IF frequency is 100 MHz.

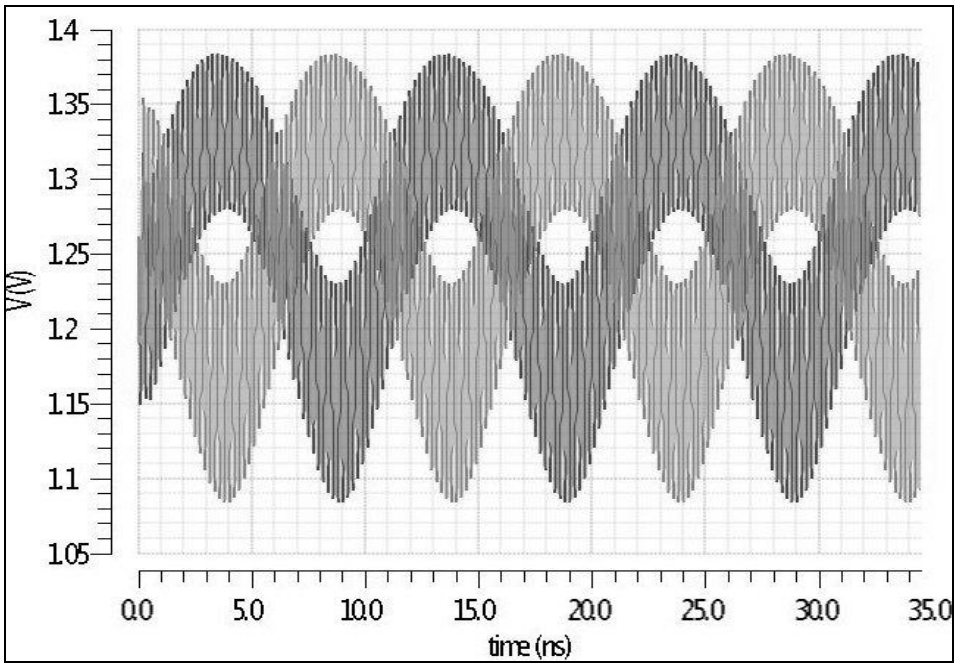

Fig.6.Transient Analysis of Proposed Mixer Circuit

Fig.7 represents the graph between conversion gain and LO power, in which maximum conversion gain is 11 dB at a LO power of 5 dBm.

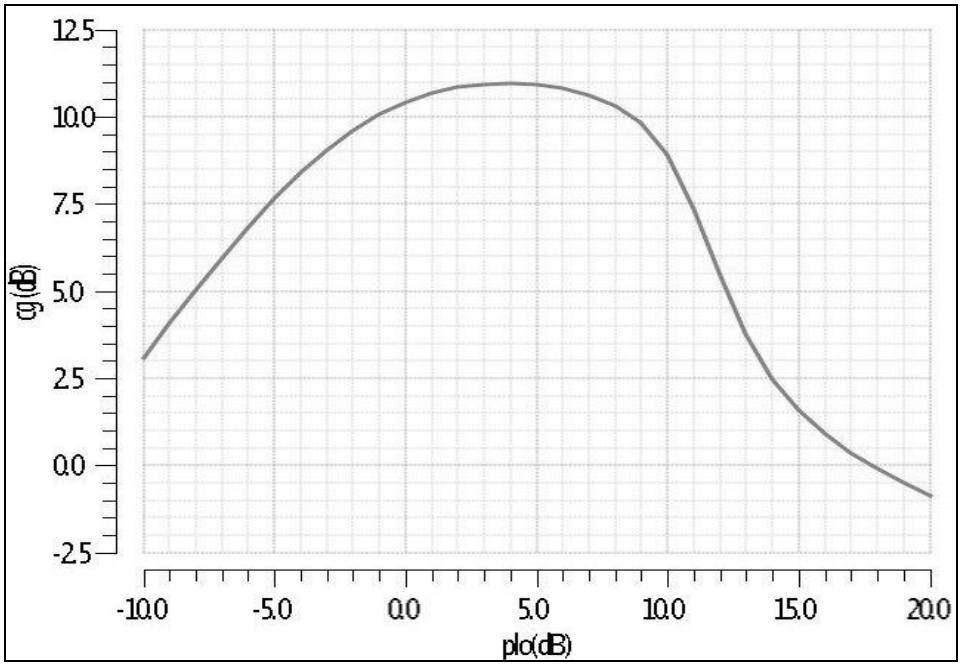

Fig.7. Conversion Gain Versus LO Power

The graph between the conversion gain and frequency of proposed mixer is shown in the Fig.8. From the simulation result the conversion gain of the proposed mixer obtained is 11 dB (approximately) and the analysis provides a flat response over a wide range of frequency.

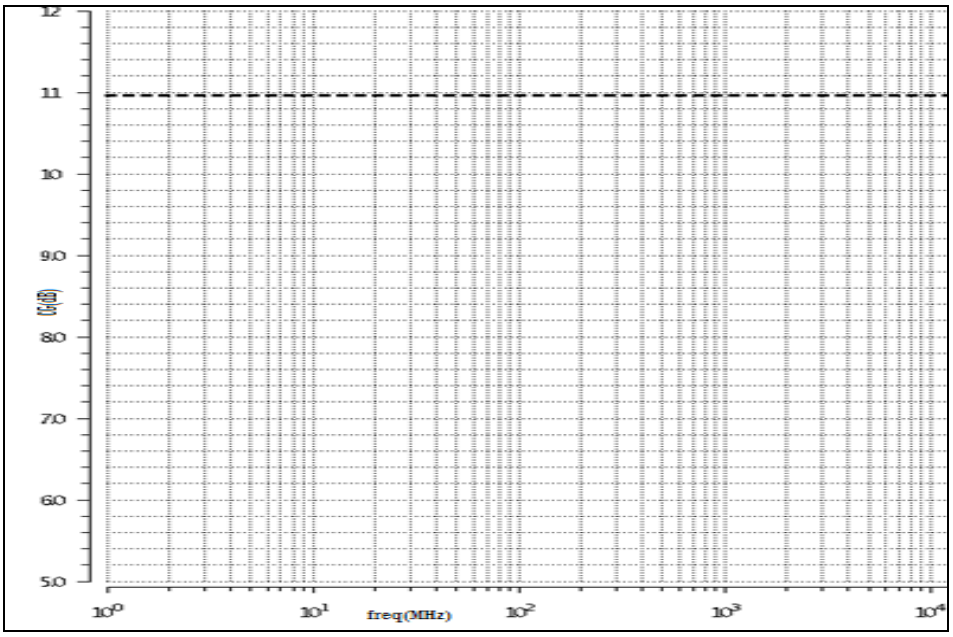

Fig.8. Conversion Gain Versus Frequency

The noise figure versus RF frequency plot is shown in the Fig.9. From the plot the noise figure of the proposed mixer obtained is 8.1 dB (approximately) over the entire frequency range from 0.7 GHz to 10 GHz.

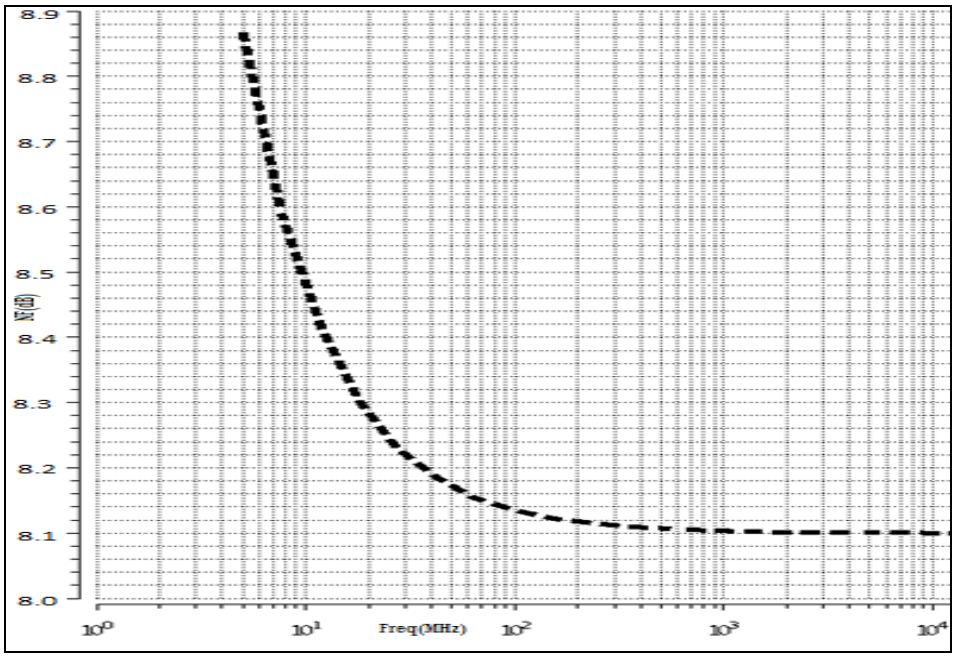

Fig.9. Noise Figure Versus Frequency

The IIP3 (third order input intercept point) plot of the proposed mixer is shown in the Fig.10. From the plot, it is observed that the third order intercept point is 10.8 dBm. The layout design of

the proposed schematic is shown in the Fig.11.

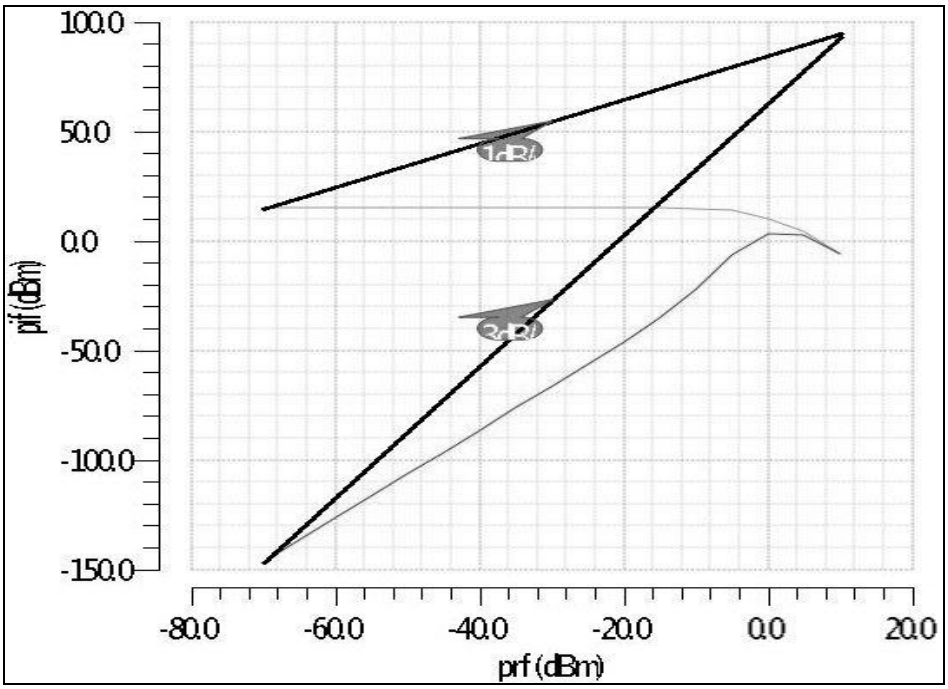

Fig.10. IIP3 (RF Power Versus IF Power) of Proposed Mixer

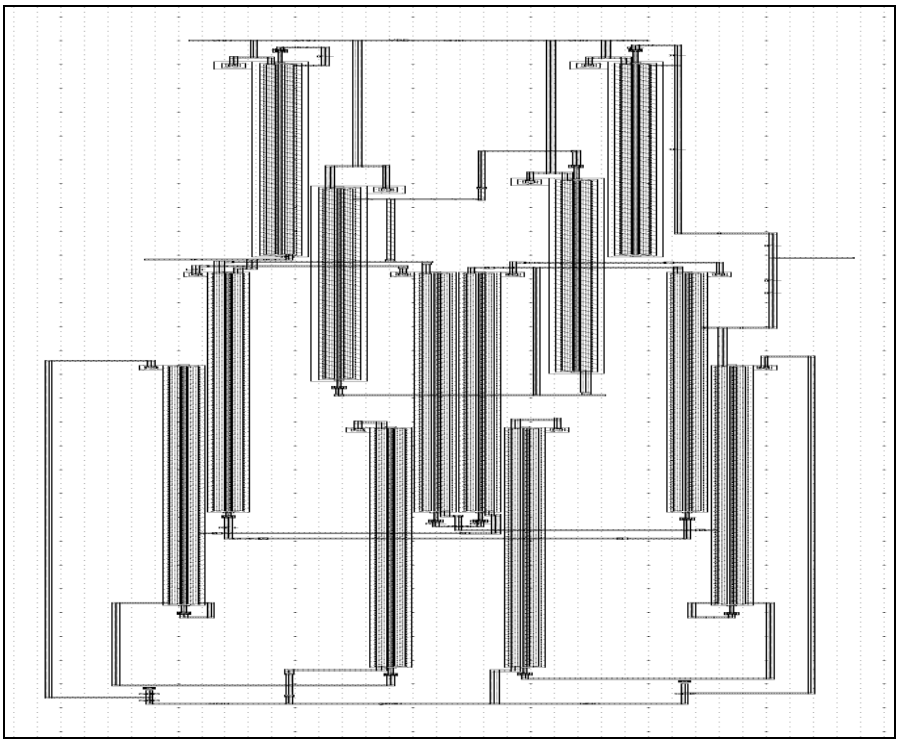

Fig.11. Layout Design of the Proposed Mixer

4. Discussion

As per the simulation results obtained, the proposed mixer design operates at a supply voltage of 1.8 V with power consumption of 0.5 mW. The third order input intercept point (IIP3)

is 10.8 dBm while the conversion gain and the noise figure are 11 dB and 8.1 dB respectively. It is observed that, the calculated conversion gain (11.66 dB) is nearly equal to the simulated conversion gain (11 dB). By comparison to CMOS mixers reported in the literature [4-12], the proposed mixer using the combination of bulk injection technique, switched biasing technique and current bleeding technique provides high conversion gain, low noise and low power performance. The comparison is shown in the Table-1.

Tab. 1. Performance Summery of CMOS Mixers

Ref.	CMOS Process (µm)	Frequency (GHz)	IF (MHz)	Conversion Gain (dB)	NF (dB)	IIP3 (dBm)	Supply Voltage (V)	Power (mW)	Technique
4	0.18	0.2-16	528	5.3	-	-	1.8	15	Folded
5	0.18	2.4	100	7.6	10.9	-5	1.8	8.1	Switched Biasing
6	0.18	0.9-1	100	1.27	19.8	-16.65	1	1.6	Bulk Injection
7	0.13	3.1-10.6	264	9.8	14.5	-11	1.2	1.85	Folded
8	0.18	0.5-7.5	100	5.7	15	-5.7	0.5	0.8	Bulk Injection
9	0.13	10-35	100	1	-	-	1	6	Bulk Pumped
10	0.18	0.2-13	264	9.9	11.7	-10	0.8	0.88	Bulk Injection and Switched Biasing
11	0.18	24	50	8.376	11.6	-8.4	1.8	5.65	Current Bleeding
12	0.13	2.4	100	7.5	15	1	0.45	0.572	Current Bleeding
This Work	**0.18**	**1-10**	**100**	**11**	**8.1**	**10.8**	**1.8**	**0.5**	**Bulk Injection, Switched Biasing and Current Bleeding**

Conclusion

In this paper, a low noise, low power consumption and high gain mixer is presented using 0.18 µm CMOS process. The bulk injection technique enables the proposed mixer to achieve low

power consumption with superior gain flatness characteristic resulting from the reduction of parasitic capacitances with the help of current bleeding technique. Low noise performance is accomplished with the help of switched biasing technique. The simulation results of the proposed mixer show that, the maximum conversion gain of 11 dB, a minimum noise figure of 8.1 dB and third order input intercept point of 10.8 dBm, while consuming only 0.5 mW from 1.8 V supply voltage. So, the RF mixer is suitable for a building block in low voltage and low power RF receiver front end design in recent high level wireless system.

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