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An Improved Single Phase Self-balancing Switched Capacitor Based Step-up Nine Level Inverter

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ABSTRACT

The improved single phase switched capacitor based nine level inverter is presented in this article. A low DC input voltage is transformed into AC and boost up to the high output voltage without any Boost converter, inductors, transformers. The self-balancing process is involved in the states of charging and discharging of the capacitors. The presented topology does not have any H-bridge configurations which result in the low Total Standing Voltage (TSV). The Phase Disposition Carrier based PWM (PDCPWM) control technique is applied to the presented nine level inverter. The conduction loss, switching loss, efficiency and capacitor ratings are analyzed mathematically. The comparative analysis of the number of semiconductor switches, Total Standing Voltage, Peak Inverse Voltage between the presented topology and existing topology is explained in detail. Finally, using MATLAB/SIMULINK the proposed nine level inverter is simulated to realize the performance of the presented topology.

1. INTRODUCTION

Nowadays, Multilevel Inverters (MI's) have become very popular in usage for the applications in renewable energy systems, industries, electric vehicles, HVDC transmission systems [1]. The Multilevel Inverters have low dv/dt, high efficiency, improves the quality of output [2]. The three classical topologies NPC [3, 4], FC [5, 6], CHB [7, 8] are widely using in many applications. For more levels of output, the CHB, NPC, and FC requires more gate driver circuits, semiconductor devices, and facing problems in balancing the capacitor voltages [9]. In many industrial applications, the high output AC voltage is required from the low input DC voltage [10]. For this purpose, the transformer or boost converter based topologies are preferred. But, these inductor or transformer topologies have high volumes of cores, require more filtering circuits which leads to expensive, complexity and bulky in size [11]. The power electronics researchers and industrialists of all over the world are inventing the Transformer-less inverter topologies to obtain the more levels of DC-AC output voltage with less number of semiconductor devices, low Total Standing Voltage (TSV) and Peak Inverse Voltage (PIV) [12].

The switched diode-based cascaded H-Bridge Multilevel inverter of two-stage configuration with several numbers of DC sources has been proposed by Wang et al. [13]. The modules of switched diode produce the number of levels in the first stage, the H-bridge inverter generates the polarity in the second stage with less number of switches. The switched capacitor based H-bridge Inverter with self-balancing capability is proposed by Hinago and Koizumi [14]. For more levels of output voltage, the switches voltage stress is very

high, leads to high TSV and PIV. The alternate connected switched DC sources [15] are placed in opposite polarities through the semiconductor switches with boosting capability that will produce an output voltage. For high levels of output, the number of DC sources is required which causes the high voltage stress between the semiconductor switches. The Packed U-Cells (PUC) inverter [16] has a single DC source, with self-balancing capacitors generates the high levels of the DC-AC output voltage. The system will become very complex, increases the voltage stress of switches for the high number of levels. The Switched capacitor boost inverter [17] has a single DC source, four capacitors with the self-balancing capability to produce a nine-level inverter. The requirement of capacitors is high for increasing the number of levels. The self-balanced based switched capacitor boost multilevel inverter [18] is shown in Figure 1, voltage stress of each switch is the same which is equal to input DC voltage, which results in low TSV and PIV. The requirement of semiconductor switches, gate drivers is more in this topology which leads to system bulky and expensive.

An improved switched-capacitor based nine-level inverter without H-bridge configuration is presented in this article. It has a single DC source, less number of semiconductor switches and capacitor compared to the earlier topologies. The self-balancing process is utilized for charging and discharging of the capacitors. The level shift PWM technique is preferred to this topology to provide gate pulses to the switches. The novelty in this topology is maintaining a low Total Standing Voltage and Peak Inverse voltage with less number of switches which reduces the losses and cost of the system. The performance of topology is analyzed by THD analysis with a modulation index of 0.9. Due to having boosting voltage

ability, this inverter is offered to applications such as Renewable Energy Systems (RES), Electric Vehicles (EVs), Uninterruptible Power Supplies (UPS).
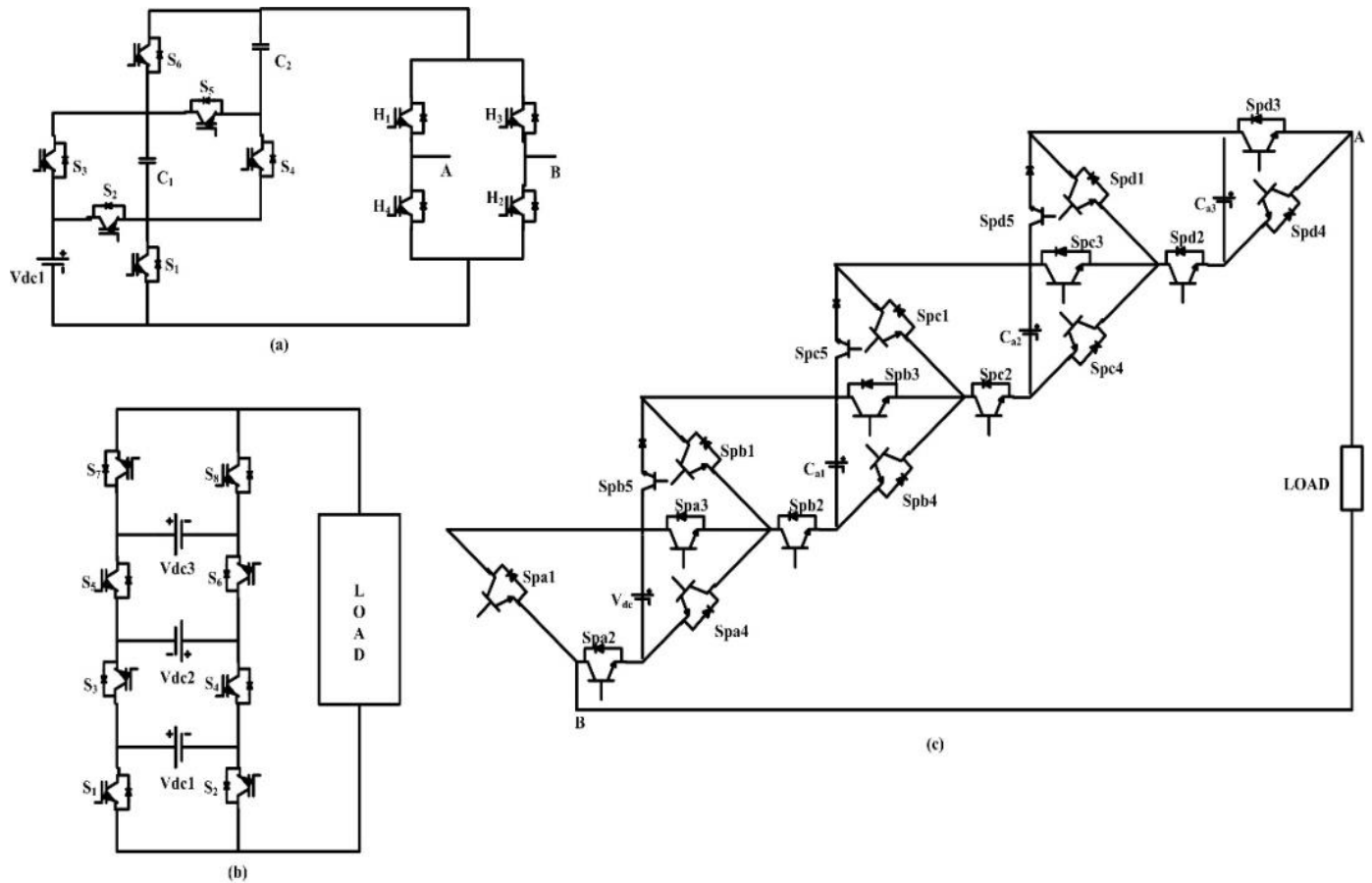

Figure 1. Existing topologies (a)[14] (b) [15] (c) [18]

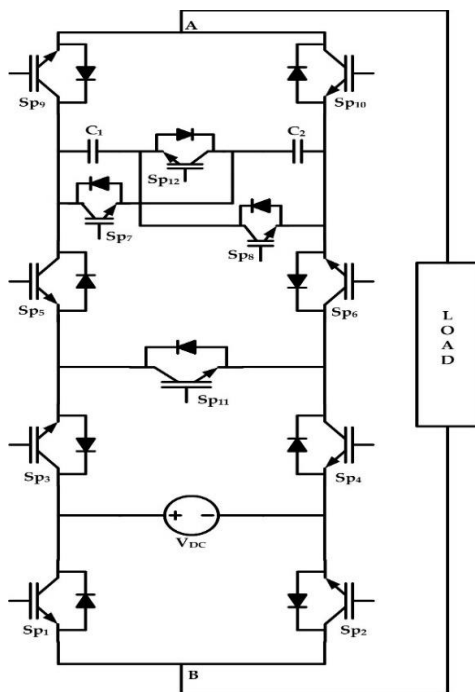## 2. ANALYSIS OF IMPROVED NINE LEVEL INVERTER

Figure 2. Improved switched-capacitor based nine-level inverter

The improved switched-capacitor based nine-level inverter is given in Figure 2. This topology requires a single DC source, twelve semiconductor switches, and two capacitors. The switches pair Sp_1 & Sp_2, Sp_3 & Sp_4, Sp_5 & Sp_6, Sp_9 & Sp_{10} are operated complementary. For the charging and the discharging of capacitors, the self-balancing process is utilized. This topology will boost the voltage of $2V_{in}$ from the application of input voltage V_{DC} with the nine-level output. The standing voltage of switches Sp_1, Sp_2, Sp_3, Sp_4, Sp_5, Sp_6, Sp_9, Sp_{10}, Sp_{11} are equal to the input voltage V_{DC}, whereas the switches Sp_7, Sp_8, Sp_{12} are equal to half of the input voltage $\frac{V_{DC}}{2}$. The two capacitors are charging during the Zero voltage level and $\pm 1 V_{DC}$ voltage level and discharges during $\pm\frac{V_{DC}}{2}$, $\pm\frac{3V_{DC}}{2}$, $\pm 2V_{DC}$ voltage levels. Therefore, the capacitor voltages are balanced without using any balancer circuit.

2.1 Modes of operation

Initially, the two capacitors C_1, C_2 are connected in series through the switch Sp_{12} and charged to $\frac{V_{DC}}{2}$ during the zero voltage level by conducting the switches Sp_3 and Sp_4. For the $+2V_{DC}$ output voltage level, the input voltage V_{DC} provides the current to the load through the switches Sp_3, Sp_{11}, Sp_6, Sp_{12}, Sp_9, Sp_2 as shown in Figure 3(a). The two charged capacitors are starts to discharge through the switch Sp_{12} and added with input voltage V_{DC} to produce the $+2V_{DC}$ as output voltage.

$$V_o = V_{in} + V_{C1} + V_{C2} = V_{DC} + \frac{V_{DC}}{2} + \frac{V_{DC}}{2} = 2V_{DC} \qquad (1)$$

$$V_o = V_{in} + V_{C2} = V_{DC} + \frac{V_{DC}}{2} = \frac{3V_{DC}}{2} \qquad (2)$$

The switches Sp_3, Sp_{11}, Sp_6, Sp_7, Sp_9, & Sp_2 will conduct from the input voltage V_{DC} toward the load to obtain $\frac{+3V_{DC}}{2}$ output voltage level as presented in Figure 3(b). During this process, the two capacitors are connected in parallel, the capacitor C_1 will charge to $\frac{V_{DC}}{2}$ through the switch Sp_8, capacitor C_2 will discharge through the switch SP_7 and is added to the input voltage V_{DC} to obtain the output voltage $\frac{+3V_{DC}}{2}$.

For the $+1V_{DC}$ voltage level, the input voltage V_{DC} is directly connected to the load through the switches SP_3, Sp_5, Sp_9, & Sp_2 as shown in Figure 3(c). At this instant, the two capacitors C_1 and C_2 are charged to a voltage of $\frac{V_{DC}}{2}$ through the SP_{12}. The input voltage source V_{DC} is not connected to the circuit, the Capacitor C_2 is acting as a source and starts to discharge the voltage through the switches Sp_7, Sp_9, Sp_2, Sp_4, Sp_6 to produce the $\frac{+V_{DC}}{2}$ output voltage level as shown in Figure 3(d).
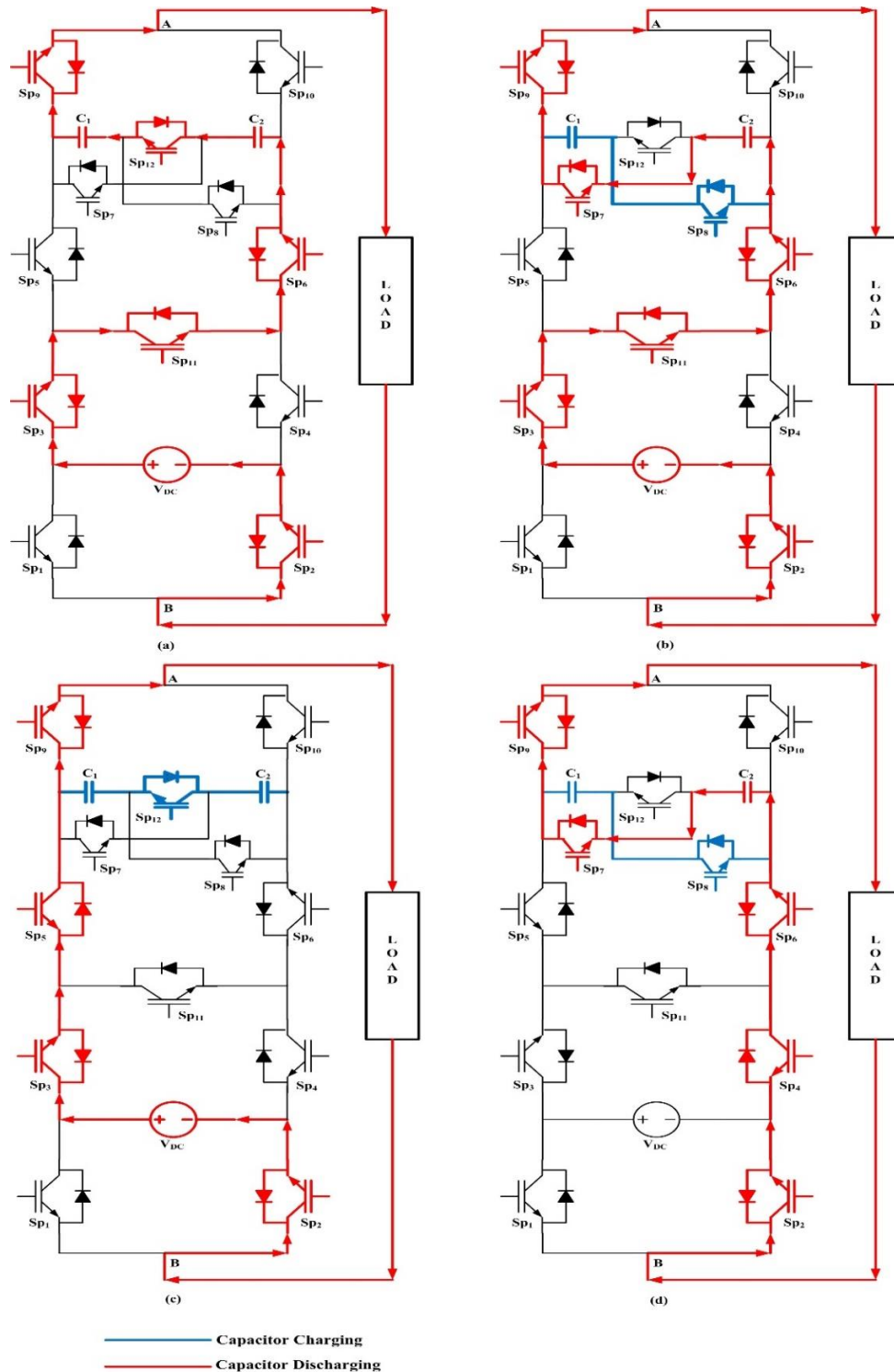

Figure 3. Switching modes for positive output voltages (a) $+2V_{DC}$ (b) $\frac{+3V_{DC}}{2}$ (c) $+1V_{DC}$ (d) $\frac{+V_{DC}}{2}$

The negative voltage levels of the proposed topology are obtained by the complementary operation of the switches. For $\frac{-V_{DC}}{2}$ voltage level, the capacitor C_1 is connected to the load and starts to discharge through the switches Sp_5, Sp_3, Sp_1, Sp_{10}, & Sp_8 as shown in Figure 4(a). At this, the capacitor C_2 is charging simultaneously by using the switch Sp_7. The $-1V_{DC}$ voltage level is shown in Figure 4(b), the input voltage V_{DC} is passing the current directly to the load through the switches Sp_1, Sp_{10}, Sp_6, & Sp_4, and the two capacitors are charging by using the switch Sp_{12}. The input voltage V_{DC} is added to the capacitor C_1 to provide the current to the load through the switches Sp_1, Sp_{10}, Sp_8, Sp_5, Sp_{11}, & Sp_4 to produce $\frac{-3V_{DC}}{2}$ voltage level as shown in Figure 4(c). The two capacitors C_1, C_2 are discharged through the switches Sp_1, Sp_{10}, Sp_{12}, Sp_5, Sp_{11}, & Sp_4 and is added to the input voltage V_{DC} to obtain the $+2V_{DC}$ voltage level as shown in Figure 4(d).
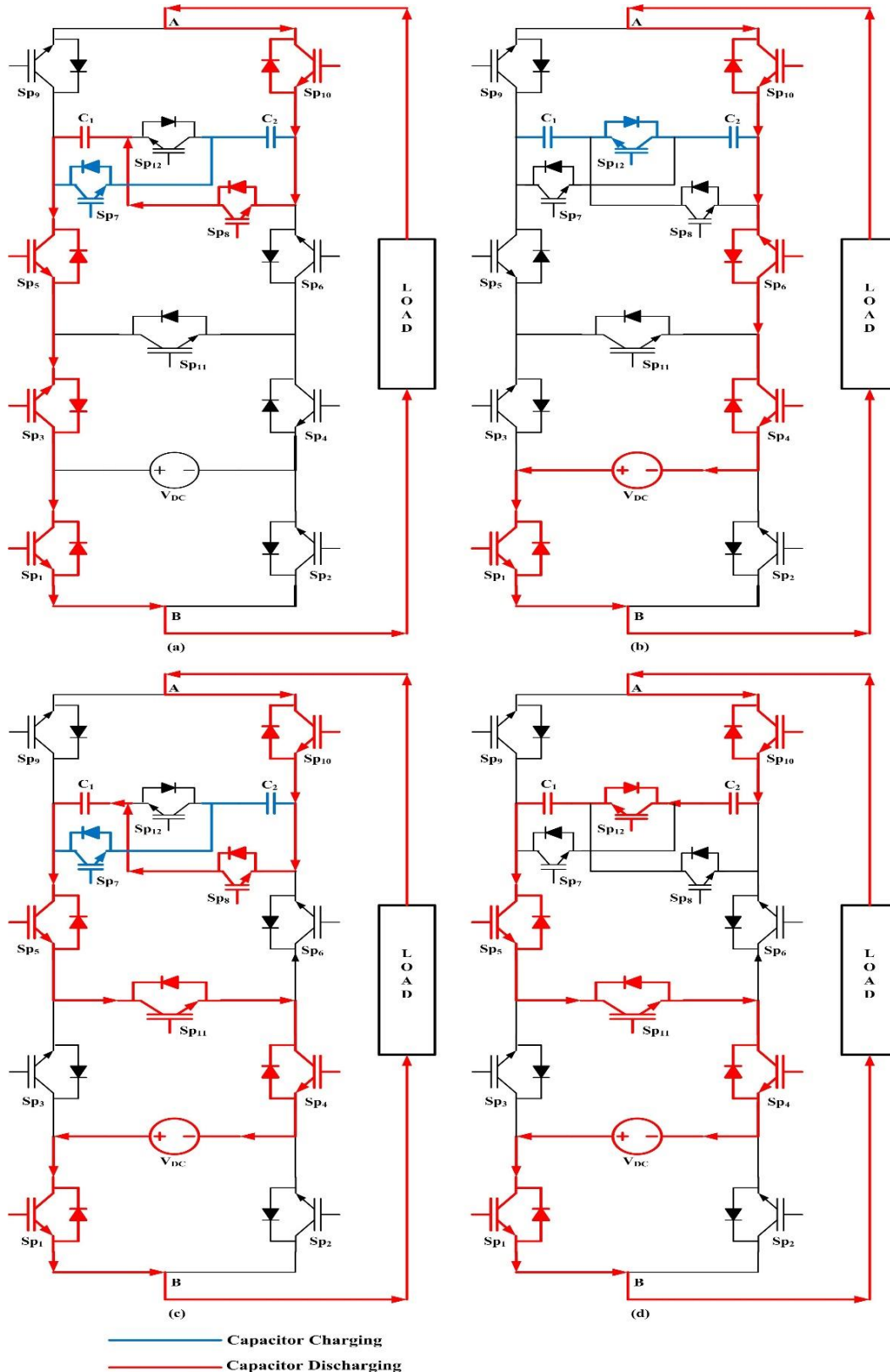

Figure 4. Switching modes for negative output voltages (a) $\frac{-V_{DC}}{2}$ (b) $-1V_{DC}$ (c) $\frac{-3V_{DC}}{2}$ (d) $-2V_{DC}$

Table 1. Switching scheme and positions of Switches, Diodes, and Capacitors

Timing instants	Switching Condition	Conducting Diodes	Conducting IGBT Switches	Position of Capacitors		Voltage Level
				C_1	C_2	
$0 - t_a$	$V_{C4} < V_{ref} < V_{C3}$	Sp4, Sp7	Sp2, Sp6, Sp9	↑	↓	$\frac{+V_{DC}}{2}$
$t_a - t_b$	$V_{C3} < V_{ref} < V_{C2}$	Sp5	Sp2, Sp3, Sp9	↑	↑	$+1V_{DC}$
$t_b - t_c$	$V_{C2} < V_{ref} < V_{C1}$	Sp7	Sp2, Sp3, Sp6, Sp9, Sp11	↑	↓	$\frac{+3V_{DC}}{2}$
$t_c - t_d$	$V_{ref} > V_{c1}$	----	Sp2, Sp3, Sp6, Sp9, Sp11, Sp12	↓	↓	$+2V_{DC}$
$t_f - t_a^*$	$V_{C5} < V_{ref} < V_{C4}$	Sp2, Sp3	Sp5, Sp10, Sp12	↑	↑	0
$t_a^* - t_b^*$	$V_{ref} < V_{c8}$	----	Sp1, Sp4, Sp5, Sp10, Sp11, Sp12	↓	↓	$-2V_{DC}$
$t_b^* - t_c^*$	$V_{C8} < V_{ref} < V_{C7}$	Sp8	Sp1, Sp4, Sp5, Sp10, Sp11	↓	↑	$\frac{-3V_{DC}}{2}$
$t_c^* - t_d^*$	$V_{C7} < V_{ref} < V_{C6}$	Sp6	Sp1, Sp4, Sp10	↑	↑	$-1V_{DC}$
$t_d^* - t_e^*$	$V_{C6} < V_{ref} < V_{C5}$	Sp3, Sp8	Sp1, Sp5, Sp10	↓	↑	$\frac{-V_{DC}}{2}$
↑ = Charging ; ↓ = Discharging						

3. PHASE DISPOSITION CARRIER BASED PWM

The Phase Disposition Carrier-based Pulse Width Modulation (PDCPWM) control scheme is used for the presented topology shown in Figure 5. The sinusoidal reference signal V_{ref} is comparing with the eight triangular carrier signals V_{C1} -V_{C8} to produce the gate pulses to the switches of the nine-level inverter. The eight carrier signals have the same amplitude A_C, frequency f_C and phase is arranged one by one based on their amplitudes. For high levels of output, the switches Sp11 & Sp12 are conducting at $V_{ref} > V_{C1}$ and $V_{ref} < V_{C8}$. The switches Sp7 & Sp8 will be turned ON, when the switch Sp12 is turned OFF i.e., at $V_{C2} < V_{ref} < V_{C1}$, $V_{C4} < V_{ref} < V_{C3}$, $V_{C6} < V_{ref} < V_{C5}$, $V_{C8} < V_{ref} < V_{C7}$. The switching scheme and states of the capacitors are given in Table 1.
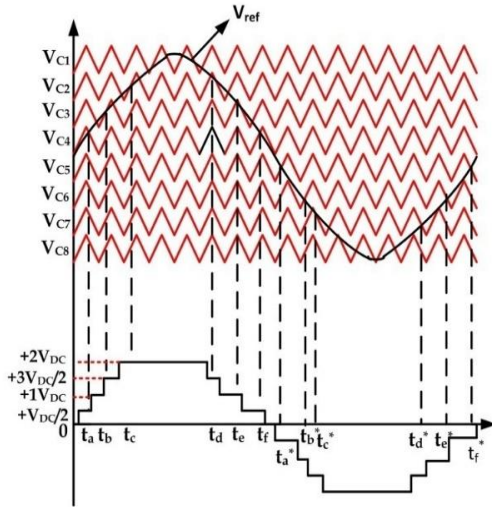

Figure 5. Phase Disposition Carrier-based Pulse Width Modulation (PDCPWM) control scheme

From Figure 5, the carrier signals $V_{C1} - V_{C4}$ is compared with the positive half cycle of reference sinusoidal signal to produce positive voltage levels. Similarly, the carrier signals $V_{C5} - V_{C8}$ are compared with the negative half cycle of reference sinusoidal signal to obtain the negative voltage levels. The positive voltage levels are obtained at time instants $t_a - t_d$ and are given as

$$t_a = \frac{\sin^{-1}\left(\frac{A_{C4}}{A_{ref}}\right)}{2\pi f_r} \qquad (3)$$

$$t_b = \frac{\sin^{-1}\left(\frac{A_{C3}}{A_{ref}}\right)}{2\pi f_r} \qquad (4)$$

$$t_c = \frac{\sin^{-1}\left(\frac{A_{C2}}{A_{ref}}\right)}{2\pi f_r} \qquad (5)$$

$$t_d = \pi - \frac{\sin^{-1}\left(\frac{A_{C2}}{A_{ref}}\right)}{2\pi f_r} \qquad (6)$$

When $f_r = 50Hz$; $A_{ref} = 3.8$ the time instants of the output voltage are calculated. When the timing instant $t_a - t_b$ the two capacitors are charging up to the nominal voltage of $\frac{V_{DC}}{2}$. At timing instant $t_c - t_d$ the two capacitors are discharging and the maximum discharging of the capacitor [19] is given as:

$$\Delta Q_{Ci} = \int_{t_c}^{t_d} i_L \sin(\omega_r t)\, dt \qquad (7)$$

where, t_c, t_d are charging and discharging time instants; i = number of capacitors; $\omega_r = 2\pi f_r$.

A ripple factor $k_r = 0.1$, the rating of the capacitor is given as:

$$C_i = \frac{\Delta Q_{Ci}}{k_r \left(\frac{V_{DC}}{2}\right)} \qquad (8)$$

4. CALCULATION OF LOSSES

The calculation of power loss for a switched capacitor based Multilevel Inverter depends on the Conduction Loss and Switching Loss.

4.1 Conduction loss (P_CL)

The reason for occurring the conduction losses are ON state switching resistance R_SW,ON, ON state diode resistance R_D,ON,

and internal resistance of the capacitor R_C. At time $0 < t < t_a$, the voltage level is changing from 0 to $\frac{+V_{DC}}{2}$ with three switches, two diodes at zero level and three switches, two diodes, and one capacitor at $\frac{+V_{DC}}{2}$ level. The equivalent resistances of ON state switches, diodes, and capacitors at different voltage levels are given in Table 2.

Table 2. Equivalent resistance of diodes, switches, and capacitors

Voltage Levels	Number of ON State devices			Equivalent Resistances
	Switches	Diodes	Capacitors	
0	3	2	-	$3R_{sw,ON} + 2R_{D,ON}$
$\frac{+V_{DC}}{2}$	3	2	1	$3R_{sw,ON} + 2R_{D,ON} + R_C$
$+1V_{DC}$	3	1	-	$3R_{sw,ON} + R_{D,ON}$
$\frac{+3V_{DC}}{2}$	5	1	1	$5R_{sw,ON} + R_{D,ON} + R_C$
$+2V_{DC}$	6	-	2	$6R_{sw,ON} + 2R_C$

The conduction loss at $0 < t < t_a$ is given as:

$$P_{CL1} = P_{0\&\frac{V_{DC}}{2}} = \int_0^{t_a} \left[I_{Load,RMS}\right]^2 \left[\left[3R_{sw,ON} + 2R_{D,ON} + R_C\right]\left[\frac{A_{ref}\sin\omega_r t}{A_C}\right] + \left[3R_{sw,ON} + 2R_{D,ON}\right]\left[1 - \frac{A_{ref}\sin\omega_r t}{A_C}\right]\right] dt$$

where, $\omega_r = 2\pi f_r$;

$$I_{Load,RMS} = I_L \sin\omega_r t \qquad (9)$$

Similarly, the conduction loss at time instants $t_a < t < t_b$, $t_b < t < t_c$, $t_c < t < t_d$ are calculated as follows.

$$P_{CL2} = P_{\frac{V_{DC}}{2}\&V_{DC}} = \int_{t_a}^{t_b} \left[I_{Load,RMS}\right]^2 \left[\left[3R_{sw,ON} + R_{D,ON}\right]\left[\frac{A_{ref}\sin\omega_r t - A_C}{A_C}\right] + \left[3R_{sw,ON} + 2R_{D,ON} + R_C\right]\left[1 - \frac{A_{ref}\sin\omega_r t - A_C}{A_C}\right]\right] dt \qquad (10)$$

$$P_{CL3} = P_{V_{DC}\&\frac{3V_{DC}}{2}} = \int_{t_b}^{t_c} \left[I_{Load,RMS}\right]^2 \left[\left[5R_{sw,ON} + R_{D,ON} + R_C\right]\left[\frac{A_{ref}\sin\omega_r t - 2A_C}{A_C}\right] + \left[3R_{sw,ON} + R_{D,ON}\right]\left[1 - \frac{A_{ref}\sin\omega_r t - 2A_C}{A_C}\right]\right] dt \qquad (11)$$

$$P_{CL4} = P_{\frac{3V_{DC}}{2}\&2V_{DC}} = \int_{t_c}^{t_d} \left[I_{Load,RMS}\right]^2 \left[\left[6R_{sw,ON} + 2R_C\right]\left[\frac{A_{ref}\sin\omega_r t - 3A_C}{A_C}\right] + \left[5R_{sw,ON} + R_{D,ON} + R_C\right]\left[1 - \frac{A_{ref}\sin\omega_r t - 3A_C}{A_C}\right]\right] dt \qquad (12)$$

The output voltage has quarter-wave symmetry, therefore, the total conduction loss is given as:

$$P_{CL} = 4P_{CL1} + 4P_{CL2} + 4P_{CL3} + 2P_{CL4} \qquad (13)$$

4.2 Switching loss (P_{SwL})

The main source of occurring the power losses is switching losses which are occurred due to the switching actions of the semiconductor devices. The switches Sp_1, Sp_2, Sp_7, Sp_8, Sp_9, Sp_{10}, Sp_{11}, & Sp_{12} are operated at the low switching frequency $\left(\frac{f_{sw}}{2}\right)$ and Sp_3, Sp_4, Sp_5, Sp_6 switches are operated at the high switching frequency f_{sw}. At ON-state of the switches, the power loss is given as:

$$P_{sw,on} = f_{sw} \int_0^{t_{on}} V_s(t)I_s(t)dt = \frac{1}{6}f_{sw}V_sI_{s,on}t_{on} \qquad (14)$$

At OFF-state, the power loss is given as:

$$P_{sw,off} = f_{sw} \int_0^{t_{off}} V_s(t)I_s(t)dt = \frac{1}{6}f_{sw}V_sI_{s,off}t_{off} \qquad (15)$$

Therefore, the total switching losses is given as:

$$P_{swl} = \sum_{i=1}^{N_{sw}} \left(P_{swi,on} + P_{swi,off}\right) \qquad (16)$$

where, N_{sw} is a number of switches.

5. RESULTS AND DISCUSSION

The self-balanced switched-capacitor based nine-level inverter is simulated in MATLAB/SIMULINK software. The switching pulses to the inverter are obtained by comparing the carrier signals of switching frequency $f_s = 5KHz$ with the sinusoidal reference signal of frequency $f_r = 50Hz$ is given in Figure 6.

At load, R = 50Ω and L = 50mH, the input current is passed through the inverter and produces the output voltage of 400V and load current of 7.3A from the input DC voltage of 200V is shown in Figure 7 and Figure 8.

A ripple factor of 10%, the voltage across the capacitors for the values of $C_1 = C_2 = 2100\mu F$ is given in Figure 9. The capacitors are charged to $\frac{V_{DC}}{2}$ i.e 100V and discharged by the self-balanced process.
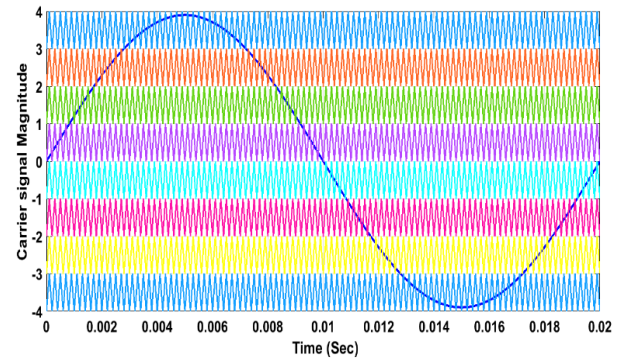

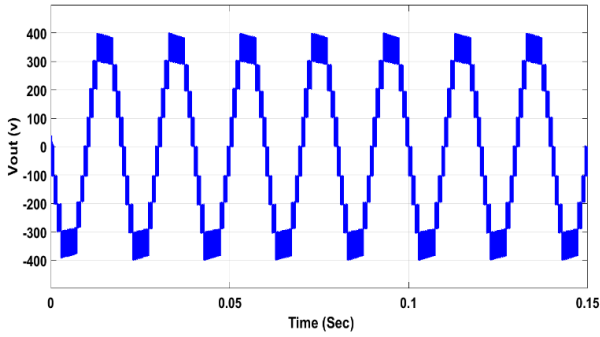**Figure 6.** Phase disposition carrier based PWM control scheme

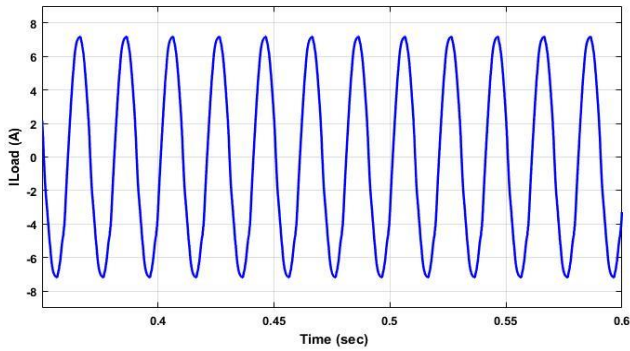**Figure 7.** Load voltage of the inverter
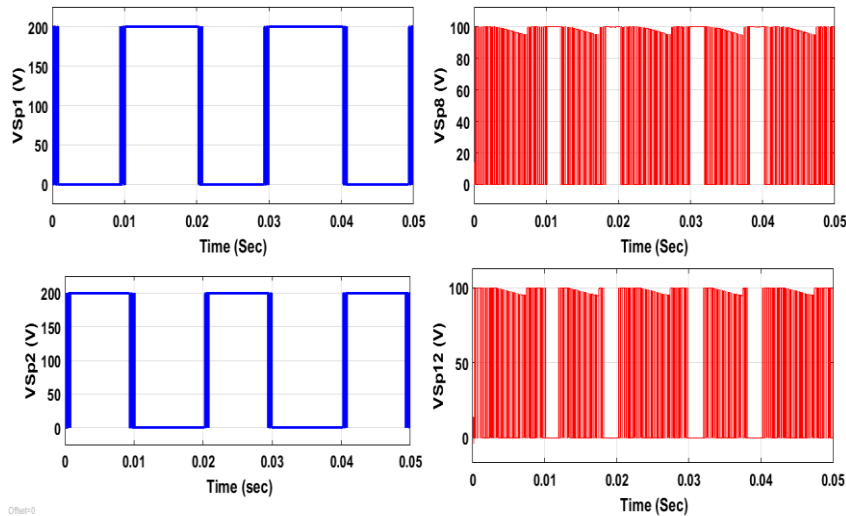

Figure 8. Load current of the inverter

The blocking voltages of the semiconductor switches employed in the inverter given in Figure 10. It shows that the switches SP_1, Sp_2 (also SP_3, Sp_4, Sp_5, Sp_6, Sp_9, Sp_{10}, Sp_{11}) must hold up the voltage which is equal to input DC voltage of 200V, and other switches Sp_7, Sp_8, Sp_{12} have the blocking voltages of half of input DC voltage i.e. 100V.

At modulation index 0.9, the switched capacitor based nine-level inverter have the Total Harmonic Distortion(THD) is 19.20% at switching frequency $f_{SW} = 5KHz$ is given in Figure 11.
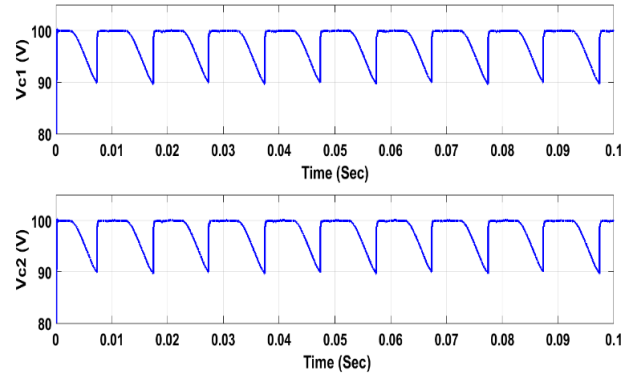

Figure 9. Capacitor voltages V_{C1} and V_{C2}

Figure 10. Blocking voltages of switches Sp_1, Sp_2, Sp_8, Sp_{12}
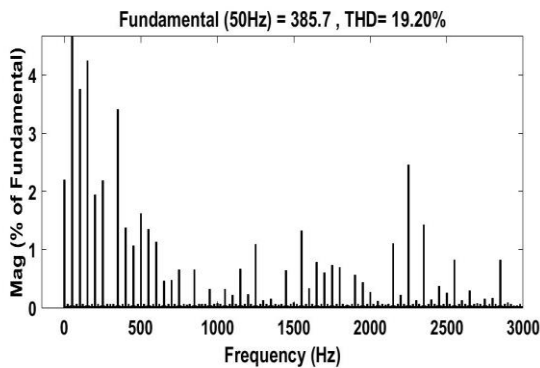
Figure 11. THD analysis at Modulation Index 0.9

6. COMPARATIVE ANALYSIS

The comparison analysis between previous topologies and present topology in terms of semiconductor switches, capacitors, and input sources is given in Table 3. From the observation of the table, the topology [14] used the less number of switches and DC sources. But it has an H-bridge configuration which leads to high PIV and TSV. The four DC sources are connected alternatively in topology [15] which leads to system expensive and required high ratings of semiconductor switches. In the topology [18], there is no H-bridge configuration, but it requires a high number of semiconductor switches leads to high TSV and increases the system cost.

https://doi.org/10.3390/en12040615

Table 3. Comparison of present topology with existing topologies

Elements	Ref. [14]	Ref. [15]	Ref. [18]	Present Topology
Swicthes	13	10	19	12
Capacitors	3	0	3	2
DC Sources	1	4	1	1
H-bridges	Yes	No	No	No
Capacitor Control	No	No	Self-balancing	Self-balancing
THD	16.40	26.89	28.07	19.20
PIV	$6 * 1V_{DC}$ $3 * 2V_{DC}$ $4 * 4V_{DC}$	$2 * 1V_{DC}$ $4 * 2V_{DC}$ $4 * 3V_{DC}$	$19 * 1V_{DC}$	$9 * V_{dc}$ $3 * \dfrac{V_{DC}}{2}$
TSV	`$28V_{DC}$	$22V_{DC}$	$19V_{DC}$	$9V_{dc} + \dfrac{3V_{DC}}{2}$

In spite of all these topologies, the present topology has many advantages such as it requires only one DC source, two capacitors, twelve semiconductor switches, and no H-bridge configuration. The present nine-level inverter is operating with low PIV i.e., nine switches are operating with $1V_{DC}$ and three switches are operating with $\frac{V_{DC}}{2}$. Therefore, the blocking voltage across the switches is low and required low rating semiconductor switches which lead to implementation cost is low compared to others.

7. CONCLUSION

The improved self-balancing switched-capacitor based step up nine-level inverter is simulated in this article. The operating modes of the inverter, charging and discharging states of the capacitors is discussed in detail. The step-up output AC voltage is obtained from the low input DC voltage without using boost converter, transformers. The Phase Disposition Carrier-based PWM (PDCPWM) control scheme is involved for the generation of switching pulses to the inverter. The ratings of the capacitors, switching and conduction losses are obtained mathematically. The comparative analysis between the existing topologies and presented topology depicts the requirement of semiconductor switches is less, operating the switches with low PIV and TSV which leads to cost-effective and improves the performance of the inverter.

ACKNOWLEDGMENT

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