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Design of New Asymmetrical Cascaded Multilevel Inverter with Reduced Number of Switches

Chettiar Ramachandra Bharathi

Department of ECE, Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science & Technology, Avadi, Chennai 600054, Tamil Nadu, India

Corresponding Author Email: crbharathi@veltechuniv.edu.in

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ABSTRACT

This paper designs an advanced circuit for multilevel inverter. The topology of the design is an asymmetric cascaded multilevel inverter based on switched capacitor. The technique of switch-capacitor inverter using series/parallel conversion (SCISPC) was developed to reduce the number of switches. In the design, the three different DC voltage sources and the capacitor connected to the circuit could be adjusted to increase the output voltage, eliminating the need for additional DC source, and, work with the diode-clamped switch arrangement, to reduce the voltage stress on each switch. To verify its performance, the proposed design was subjected to a Matlab simulation, and a fast Fourier transform analysis on the percentage of total harmonic distortion produced by the design. In addition, a hardware prototype of our design was prepared, and its operations were studied in details. The results show that our design has an edge over the other multilevel inverter topology, as it produced lower harmonics and made better use of lower circuit components.

INTRODUCTION

Renewable energy based power generation methods are gaining considerable popularity in recent year. Due to the fact of degradation of non-renewable fossil fuels which were the main source of power production for decades, the most popular renewable energy sources for power generation application are wind and solar energy as these sources are in exhaustible and produces low level of pollution [1]. Though they are renewable source of energy they also have some drawbacks. One of them is this sources are subjected to change that is the output produces by a renewable energy system is not constant as it depends on natural sources like solar energy which varies from time to time but on the other hand all our utilities and distribution system are designed to operate at a constant level especially in terms of frequency.

To overcome this problem most of the system uses certain conversion devices that can produce the desired and constant output [2]. For example, a solar based power generation system produces power by converting the sun's heat and radiation into DC voltage by using a PV panel. This DC voltage cannot be utilized by the consumers because most of the electrical appliances are designed for alternating AC voltage [3]. So this demands conversion of DC power to AC this is done by using an inverter circuit also known as DC/AC converter which consist of power electronic switches. Many researches are being done in order to achieve a more efficient inverter design which produces lower harmonics and power quality issues [4]. The most popular inverter topology proposed is a MULTILEVEL INVERTER shortly known as MLI's. This is an efficient topology especially for solar based power generation system as they can support variable DC inputs to produce the desired AC output whose waveform structure is stepped in nature compared to the conventional square wave inverters this eliminates the need for bulky filter circuits to archive pure sinusoidal waveforms which is preferred by the grid [5].

This paper proposes an MLI topology which is designed in such a way to reduce the total number of components used in the MLI circuit compared to other existing multilevel topologies and it can produce higher peak voltage. The proposed multilevel inverter can produce a 31 level stepped output voltage waveform with reduces number of switches. The proposed system comes under the cascaded H-bridge topology [6] where two types of circuit combination is used to obtain the multilevel output one of this circuits is used to produce the stepped multilevel output in positive direction and the other circuit is an H bridge inverter which helps in obtaining an alternating wave out of the unidirectional multilevel waveform. Other commonly used topologies are the diode clamped [7] and capacitor clamped methods [8]. In diode clamped method switches used are combined with a freewheeling diode for voltage sharing this method reduces the voltage stress on the switches during high frequency voltage switching. Our system uses a diode clamped power switch assembly [9]. The capacitor clamped circuit is also an advantages device configuration which reduces the unbalances in DC link capacitor [10]. Mostly multilevel inverters fall under two categories based on the level of voltage sources used. They are asymmetric and symmetric configuration [11]. If all the dc sources used in a multilevel inverter are of equal voltage level then the system is called Symmetric and if the voltage sources of different voltage levels are used then the topology is called an asymmetric. The asymmetric model is the most preferred as it can produce higher output steps [12].

Another multilevel inverter topology which is used widely is the switched capacitor based MLI. This is a modified version of a flying capacitor multilevel inverter (FCMLI) despite of their advantage the FCMLI suffer certain disadvantages [13]. FCMLI requires a greater number of

capacitors for provide different voltage levels. These capacitors are subjected to un-necessary discharge when operated at higher switching frequency. To overcome this problem special capacitor voltage balancing control scheme and circuits are needed this increases the total number of components thus making it bulky. In case of a switched capacitor topology it is capable of producing higher number of voltage level output with lesser DC sources. The switched capacitor topology is more effective when it is operated using a series parallel switching technique (SCISPC) [14]. Here the capacitor can be either charged to a certain level by connecting it in parallel to the available DC sources or be used as a DC voltage source by connecting it in series with a help of a proper switching pattern thus eliminating the need for additional voltage sources this helps in archiving higher amplitude using lesser number of DC sources [15].

The proposed multilevel topology follows this strategy in addition to the above discussed topologies to reduce the need for additional DC source and components to obtain higher stepped waveform with greater amplitude [16].

2. OPERATION OF THE PROPOSED SCMLI TOPOLOGY

The proposed switched capacitor multilevel inverter circuit is shown in Figure 1.

It is a cascaded MLI setup that is the whole circuit can be divided into two sections the level generating section and the inverter section.

The level generation circuit has a set of three voltage switching unit each unit is made up of a circuit which uses a diode, a switch and a DC source to attain a diode clamped switching arrangement [17]. N number of units can be added to the circuit to attain higher levels. The three sources used in the given system are Vdc1, Vdc2 and Vdc3. These sources are in asymmetrical patterns as each source has different voltage level [18]. Along with this three switches S1, S2, and S3 with 3 coupling diodes namely D1, D2, D3 are used who's switching controls the level formation. Also three other switches S4, S5 and S6 and a diode D4 are seen this circuit elements are used to obtain the SCISPC technique by using a single capacitor. Apart from this a H-bridge inverter with four switches H1, H2, H3 and H4 form the second section which performs the inversion of the positive directional stepped waveform to produce an alternating output [19].

The switches used in the level producing circuit should be capable of withstanding high switching frequency. But on the other hand, the switches in the polarity generating H-bridge circuit don't need high frequency capability as they operate at the fundamental frequency [20]. The overall operation of the proposed system falls under two modes of operation which is discussed in Table 1.

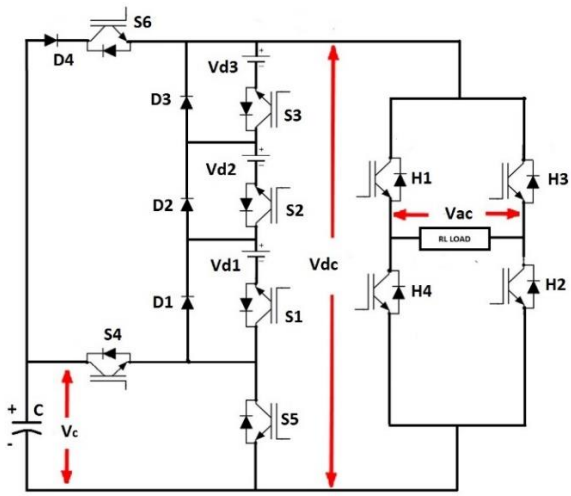


Figure 1. Circuit structure of the proposed switched capacitor multilevel inverter

Table 1. Switching states of the proposed system

SWITCHES										VOLTAGE	LEVEL
1	0	0	1	0	1	0	1	1	0	84	14
0	1	1	0	0	1	1	0	0	1	72	13
1	1	1	0	0	1	0	1	0	1	66	10
0	0	1	1	0	1	1	0	1	1	42	6
0	1	1	0	1	1	1	0	0	0	18	5
1	1	0	0	1	1	0	0	1	1	-6	-2
1	0	0	1	1	1	1	0	0	0	-12	-3
0	0	1	0	0	1	0	0	1	0	-30	-5
1	1	1	1	0	0	0	0	1	1	-36	-7
0	1	0	1	0	1	0	1	0	1	-42	-9

The overall operation of the proposed system can be divided into two modes. These modes are discussed below.

2.1 Mode I (capacitor in parallel connection)

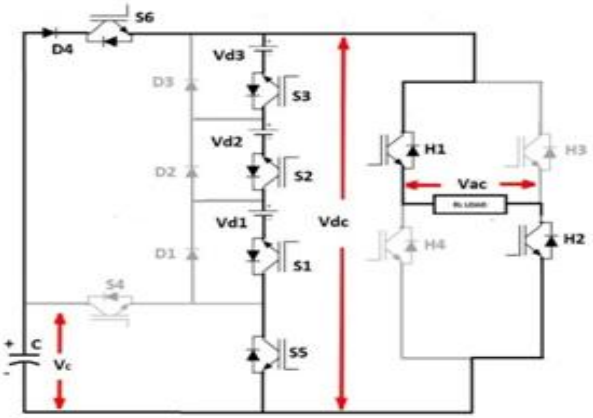
During mode I the diode D4 and switches S5 and S6 are ON while S4 is kept in OFF position this connects the capacitor in parallel configuration as discussed earlier. Now the remaining three S1, S2, and S3 are switched based on the switching patters given in table I. This operation can produce a maximum of 15 level output. Seven in the positive cycle when H1 and H2 are ON in the H-bridge circuit shown in Figure 2(a). Seven levels in the negative cycle when H3 and H4 are in ON shown in Figure 2(b). And the zero level was also taken in account thus making a total of 15 levels. The operation of the circuit in this mode and its current direction is shown in below Figure 2. The level generator's output is given by the Eq. (1)

$$V_{dc} = (V_{d1} * S_1) + (V_{d2} * S_2) + (V_{d3} * S_3) \quad (1)$$

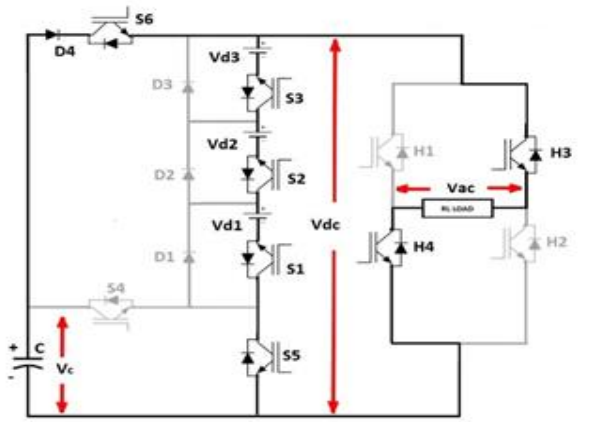
2.2 Mode II (capacitor in series connection)

During Mode II the diode D4 and switches S5 and S6 are turned OFF leaving the switch S4 in ON state. This switching pattern connects the capacitor in series with other sources. Now by following the same switching pattern another set of

15 voltage steps can be formed at even higher voltage level as the capacitor voltage gets added to the already available voltage sources.



(a) Circuit operation for positive half cycle at max DC output level in Mode I



(b) Circuit operation for positive half cycle at max DC output level in Mode I

Figure 2. Circuit operation modes

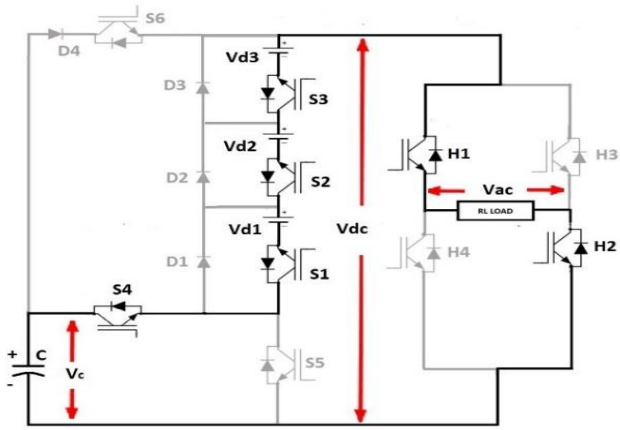


Figure 3. Circuit operation for positive half cycle at max DC output level in Mode II

This produces 7 levels above the previous 7 levels in positive half cycle when H1 and H2 are ON and 7 levels below the previous 7 levels in the negative half cycle when H3 and H4 are in ON state. Thus a total of 31 level output waveform can be produced without the use of any additional DC sources are components. The operation of the circuit in mode II in both positive cycle and negative half cycle is shown in Figure 3.

Level voltage output at mode II is given by Eq. (2)

$$V_{dc} = (V_{d1} * S_1) + (V_{d2} * S_2) + (V_{d3} * S_3) + (V_c * S_4) \quad (2)$$

The number of switches used in the level generation circuit is denoted by the variable 'Ls' and the number of voltage level produced is denoted by 'Lv'. The switches and the levels can be related by the below Eq. (3).

$$L_s = L_v = (2n+1)2 \quad (3)$$

where, n = 3, 'n' is the number of switches used in the level generation circuit

The total number of levels at the output load is denoted by 'Lf' given by Eq. (4).

$$L_f = 2L_s + 1 \quad (4)$$

The final voltage steps after the inverter can be calculated using Eq. (5)

$$V_{ac} = V_{dc}(H_1 - H_3) \quad (5)$$

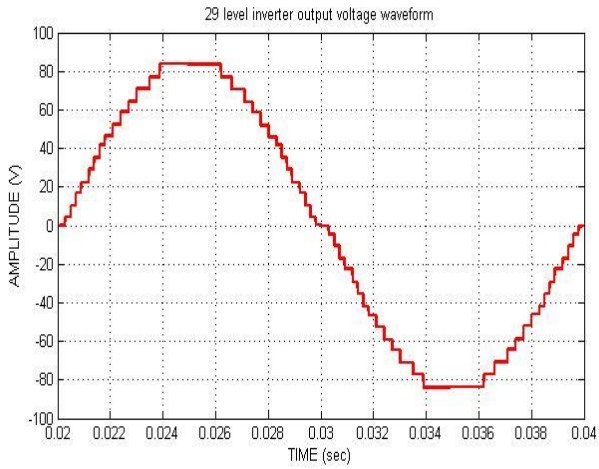
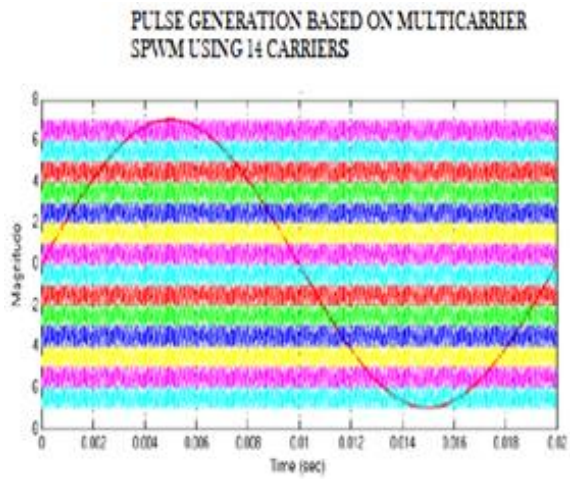


Figure 4. Output waveform of proposed system

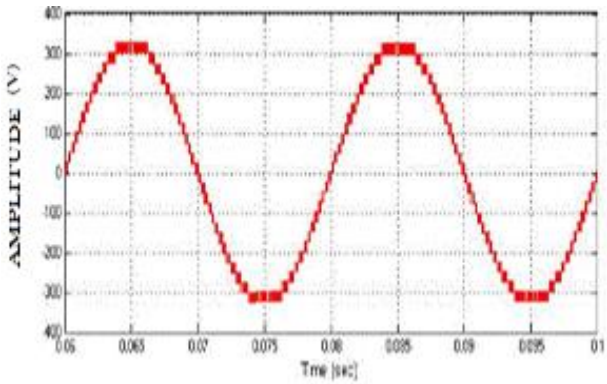
3. MULTI CARRIER SPWM TECHNIQUE

In multi carrier SPWM based pulse generation method multiple number of triangle carrier waves are compared with a single sinusoidal reference waveform to produce the require pulse [21]. Here the amplitude and the frequency of all carrier are same but the positions are manipulated based on the width of the final PWM signal. This method produces a pulse whenever the amplitude reference waveform which oscillates at fundamental frequency ie.50Hz and its zero reference placed at the middle of this carriers is greater than the carrier amplitude. For an MLI circuit with 'n' levels we need n-1 number of triangular carriers [22]. The output waveform of the proposed system is depicted in Figure 4. The resultant pulse is summed up and given to the inverter to obtain the desired steps in the output waveform. Though it is a simple method the output levels produced by applying this pulse to the inverter has internal chopping this causes higher switching losses any may reduce the life time of the inverter. This drawback has been rectified by the application of Selective Harmonics Elimination as discussed in III (a). The below Figures 5(a) and 5(b) shows output wave form of a 29 level inverter which uses

Multicarrier SPWM based control technique.



(a) carrier and reference comparison plot with 14 carrier



(b) output waveform of a 31 level inverter which uses multicarrier SPWM

Figure 5. Reference comparison and output waveforms

4. RESULTS AND DISCUSSION

The procedure of the proposed work has been verified through MATLAB/ SIMULINK software platform. The same is also experimentally verified by using DSPIC30F2010 controller.

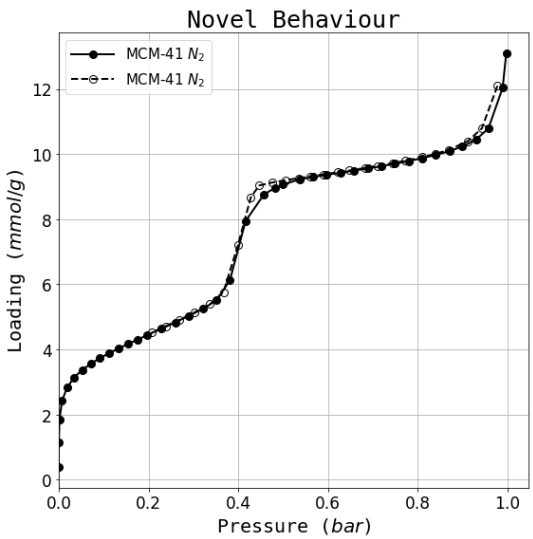


Figure 6. Proposed system MCM comparison

Figure 6 shows the shows the Multi carrier signal for controlling the proposed thirty one level inverter, fifteen carrier signal and one reference signal.

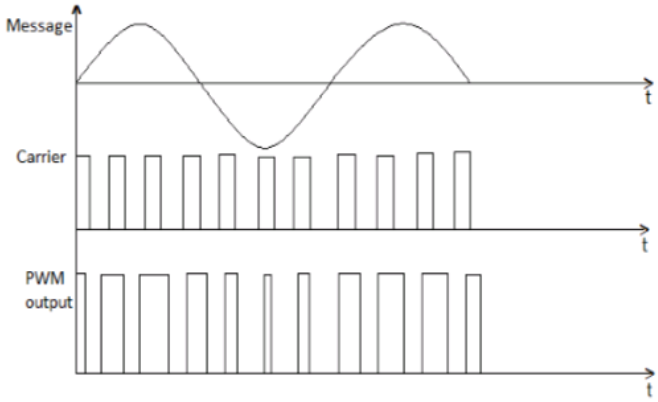


Figure 7. Proposed system PWM pulse to the H bridge inverter

Figure 7 shows PWM pulses for controlling the H bridge inverter with 180 degree mode of conduction.

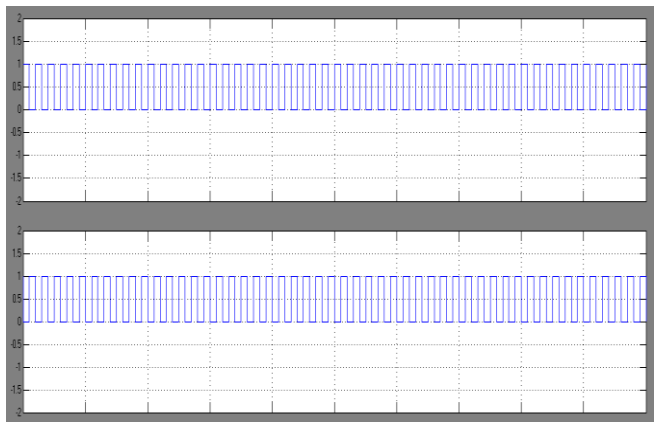


Figure 8. Proposed system PWM pulse to the H bridge inverter

Figure 8 represents the PWM pulse rate to the H Bridge inverter clearly.

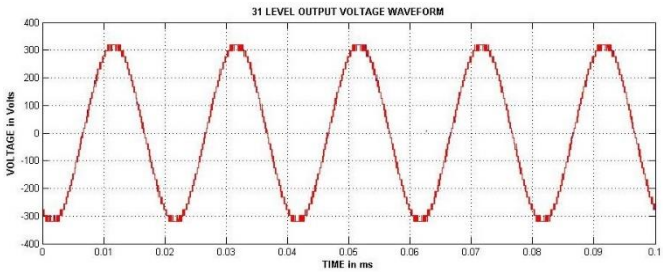


Figure 9. Proposed system thirty one level inverter output voltage

The proposed method system thirty one level inverter output voltage is represented in Figure 9.

Figure 10 Represents proposed system thirty one level inverter output current levels.

The Proposed system thirty one level inverter THD levels are illustrated in Figure 11.

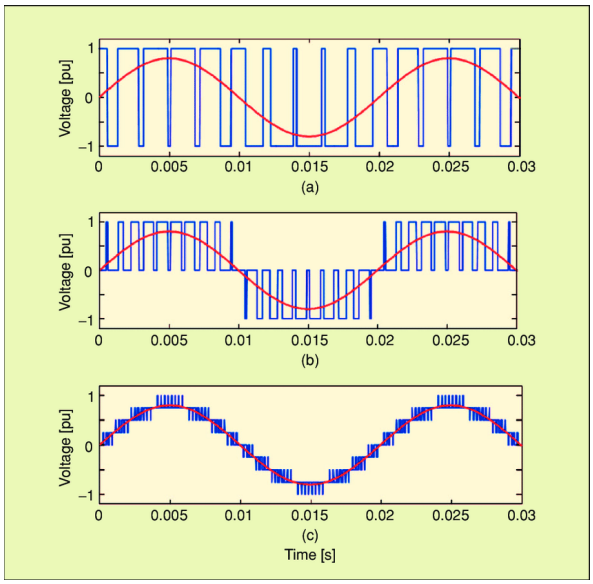


Figure 10. Proposed system thirty one level inverter output current

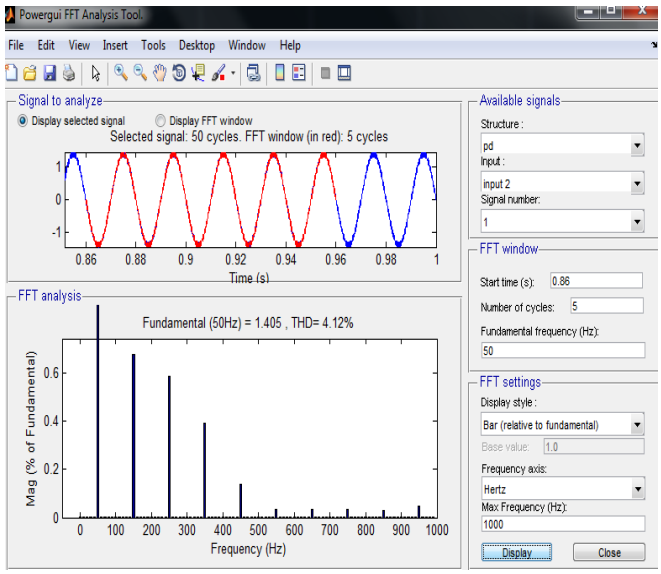


Figure 11. Proposed system thirty one level inverter THD

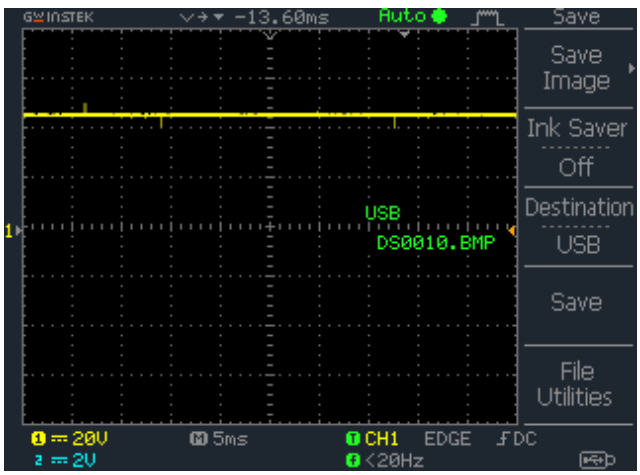


Figure 12. Hardware result of DC voltage to the multilevel inverter

The Hardware result of DC voltage compared to multilevel inverter is depicted in Figure 12.

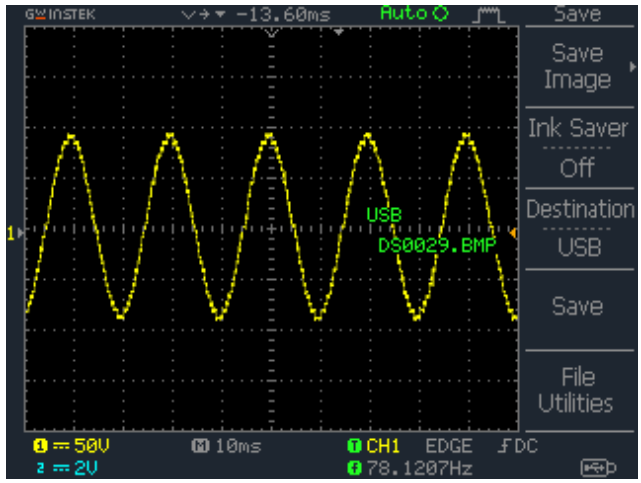


Figure 13. Hardware result of thirty one level inverter output voltage waveform

The Figure 13 indicates the hardware result of thirty one level inverter output voltage waveform.

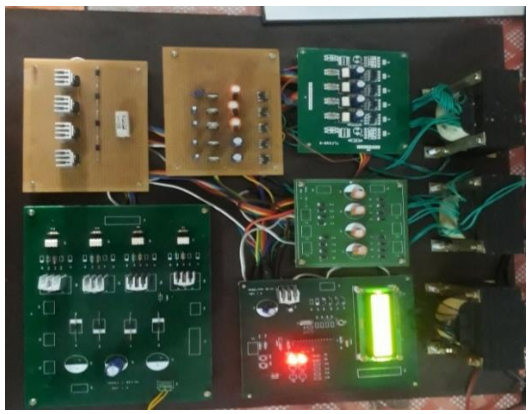


Figure 14. Experimental setup

The above figure 14 shows the experimental setup for proposed reduced switch thirty one level inverter developed using DSPIC30F2010 controller.

5. CONCLUSIONS

A novel single phase asymmetrical multilevel inverter topology which uses SCISPC method is proposed. The inverter has two set of circuits the level generator and H bridge inverter arranged in a cascaded set up. A multi carrier PWM studied and applied to obtain the desired results with lower harmonics and switching losses. A switched capacitor based series parallel control was also used to obtain higher voltage levels with reduces DC sources. The simulation and experimental results were discussed elaborately in this paper. To test the feasibility of this system a hardware prototype was developed which uses DSPIC controller to generate the switching pulse's at desired angles.

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