



Voltage Regulation at the Point of Common Coupling Using a Single-Phase Static Synchronous Compensator

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<https://doi.org/10.18280/jesa.590820>

ABSTRACT

Received: 21 June 2026

Revised: 13 August 2026

Accepted: 22 August 2026

Available online: 31 August 2026

Keywords:

single-phase static synchronous compensator, field-programmable gate array control, voltage regulation at the point of common coupling, reactive-power compensation, proportional-integral control, sinusoidal pulse-width modulation

This paper presents the design, simulation, and laboratory implementation of a single-phase static synchronous compensator (STATCOM) controlled by a field-programmable gate array (FPGA) for voltage regulation at the point of common coupling (PCC) under inductive and capacitive loading conditions. The proposed system employs a single-phase full-bridge voltage-source inverter and an Intel MAX 10 FPGA implemented on a DE10-Lite development board. A proportional-integral (PI) controller processes the PCC-voltage error and adjusts the sinusoidal pulse-width-modulation index, while a zero-crossing detector (ZCD) provides the grid timing reference. The inverter switching frequency is 4 kHz, and its output is connected to the PCC through a step-up transformer followed by an inductor-capacitor-inductor (LCL) filter. The photovoltaic/LiFePO₄ subsystem supports the inverter direct-current (DC) link through a maximum power point tracking charge controller but remains independent of the PCC-voltage control loop. Voltage regulation is achieved through reactive-current injection and absorption. The simulation and laboratory results demonstrated consistent voltage-restoration behavior under both loading conditions. Under inductive loading, the PCC voltage decreased to approximately 212 V root mean square (RMS) and was restored to the 215 V RMS reference through reactive-power injection. Under capacitive loading, it increased to approximately 219 V RMS and was reduced to 215 V RMS through reactive-power absorption. The simulated DC-link voltage was approximately 53 V, compared with the measured value of 52.3 V. These results demonstrate the feasibility of the proposed FPGA-controlled STATCOM for PCC-voltage regulation under the tested laboratory conditions.

1. INTRODUCTION

Maintaining an acceptable voltage level at the point of common coupling (PCC) is essential for the reliable operation of electrical distribution systems. Variations in load demand, feeder impedance, and reactive power flow can cause voltage deviations at the PCC. Inductive loads may produce a voltage drop because of increased reactive power demand, whereas capacitive loads may cause a voltage rise. These deviations can reduce power quality and adversely affect voltage-sensitive equipment [1, 2].

Reactive-power compensation is widely used to improve voltage regulation. Among the available compensating devices, the static synchronous compensator (STATCOM) provides controllable reactive-power injection and absorption through a voltage-source inverter (VSI) [3]. By regulating the inverter output voltage relative to the PCC voltage, the STATCOM can inject reactive power during voltage-drop conditions or absorb reactive power during voltage-rise conditions [4].

The performance of a STATCOM depends on the converter topology, control strategy, synchronization method, and switching-signal generation. Field-programmable gate arrays

(FPGAs) are suitable for power-electronic control because they provide deterministic timing and parallel execution of measurement, synchronization, control, and pulse-generation functions [5]. A proportional-integral (PI) controller offers a practical solution for real-time implementation because of its simple structure and low computational requirements [6].

In addition to the real-time control platform, the STATCOM inverter requires a suitable direct-current (DC) source for its DC link. In the proposed system, the photovoltaic (PV) array supplies renewable DC energy, while the LiFePO₄ battery supports the DC-link voltage during variations in PV output [7, 8]. This subsystem supports inverter operation, whereas PCC-voltage regulation is performed by the FPGA-controlled VSI through reactive-current injection or absorption. Previous studies have investigated PI, neuro-fuzzy, and artificial-intelligence-based STATCOM systems for voltage regulation and power-quality improvement. The main objectives of previous works on the FPGA-controlled distribution static synchronous compensator (DSTATCOM) are the reduction of harmonics, load balancing, power factor correction, and the compensation of reactive current [9, 10]. Concurrently, PV- and battery-supported compensators have been mostly explored for the management

of renewables and DC-link support [11, 12]. Yet, minimal experimental studies have focused on direct PCC-voltage regulation with inductive and capacitive loads for a low-voltage single-phase system with a low-complexity FPGA control structure, and clearly distinguished the PCC-voltage-regulation function from the energy-support function of the PV/battery subsystem.

To address this application-oriented gap, reliable synchronization between the inverter and the utility grid is incorporated into the FPGA-based control architecture. A zero-crossing-based synchronization stage provides the grid timing reference, allowing the inverter sinusoidal pulse-width-modulation (SPWM) signals to maintain frequency synchronization and close phase alignment with the grid voltage under the tested operating conditions. Based on this synchronized operation, a single closed-loop PI voltage controller directly adjusts the SPWM modulation index according to the PCC-voltage error, without employing multi-axis transformations or a closed-loop reference-current extraction stage. The STATCOM consequently injects reactive current when the PCC voltage falls below its reference and absorbs reactive current when the voltage rises above it.

The proposed system was evaluated in simulation under inductive, capacitive, and dynamic load-switching conditions, while laboratory validation covered steady-state inductive and capacitive loading. The contribution of this work lies in the reduced-complexity FPGA control architecture and the experimental validation of grid-synchronized PCC-voltage regulation under inductive and capacitive loading, while clearly separating the voltage-regulation function from the PV/battery DC-link support.

1.1 Static synchronous compensator operation and control

A STATCOM is a shunt-connected flexible alternating current transmission system (FACTS) device based on a voltage-source inverter, a DC-link, a coupling transformer, and a control system [13]. The basic configuration of a STATCOM connected to an AC power system is shown in Figure 1. The converter generates a controllable compensating voltage, which is coupled to the network through the transformer. By controlling the inverter output voltage relative to the PCC voltage, the STATCOM regulates the reactive power exchanged with the network [14].

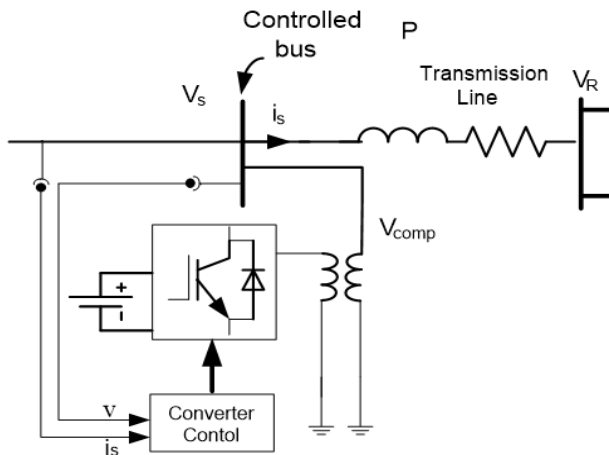


Figure 1. Basic configuration of a static synchronous compensator (STATCOM) [15]

When the inverter voltage is higher than the PCC voltage, $V_{inv} > V_{PCC}$, the STATCOM operates in capacitive mode and injects reactive power into the network. This mode is used to compensate for the voltage drop produced by inductive loads. Conversely, when $V_{inv} < V_{PCC}$, the STATCOM operates in inductive mode and absorbs reactive power to reduce the voltage rise caused by capacitive loads. When both voltages are approximately equal, the reactive power exchange becomes minimal.

The reactive power exchanged between the STATCOM and the PCC is expressed by Eq. (1) [16]:

$$Q = \frac{V_{inv}V_{PCC}}{X} \cos \phi - \frac{V_{PCC}^2}{X} \quad (1)$$

where, V_{inv} is the inverter output voltage, V_{PCC} is the PCC voltage, X is the coupling reactance, and ϕ is the phase difference between the inverter and grid voltages. Since both voltages are synchronized, the direction of reactive power exchange is primarily determined by their relative magnitudes.

In the proposed system, the inverter voltage is controlled by adjusting the SPWM modulation index through a PI voltage controller implemented on an FPGA. A zero-crossing detector (ZCD) provides the grid synchronization signal, while the inductor–capacitor–inductor (LCL) filter reduces the switching harmonics before the inverter output is connected to the PCC [17].

2. METHODOLOGY

2.1 Design of the proposed static synchronous compensator

The proposed system consists of a single-phase utility grid, a variable inductive–capacitive load, a shunt-connected STATCOM, a step-up transformer, an LCL filter and an isolation transformer and it was developed in MATLAB/Simulink software. The voltage in the utility grid is 220 V, 50 Hz, with a voltage reference of 215 V RMS in the PCC. The STATCOM is placed in parallel with the load to inject or absorb reactive current to match the PCC voltage. The main electrical, control, hardware, and load parameters of the proposed STATCOM system are summarized in Table 1.

The STATCOM power stage employs a single-phase full-bridge VSI connected to a DC link of approximately 53 V. The inverter output voltage is first increased to the PCC level by a 1:4 step-up transformer and then passed through an LCL filter composed of ($L_1 = 2.22$) mH, ($C_f = 25$) μ F, ($L_2 = 1.906$) mH, and a damping resistor of 5 Ω before being connected to the PCC. A 1:1 isolation transformer separates the experimental system from the utility grid.

The complete MATLAB/Simulink configuration of the proposed system is shown in Figure 2. The model includes the STATCOM inverter, coupling transformers, LCL filter, variable load, control subsystem, and measurement blocks required to evaluate PCC voltage regulation under inductive and capacitive loading conditions.

2.2 Photovoltaic and battery-supported DC-link configuration

It has two PV modules, a maximum power point tracking (MPPT) charge controller and a LiFePO₄ battery to support the DC link. The PV-side energy transfer is regulated by the

MPPT controller and the battery supplies energy stored on its side for the inverter-side DC supply [11, 12]. This subsystem is not related to the FPGA-based PCC-voltage control loop and is not directly responsible for deciding the direction of

reactive-current compensation. The PV/battery-supported DC-link configuration and single-phase full-bridge inverter are represented in Figure 3. The main electrical specifications of the PV module are summarized in Table 2.

Table 1. Main electrical, control, hardware, and load parameters of the proposed static synchronous compensator (STATCOM) system

Parameter	Symbol	Value
Grid voltage	V_{grid}	220 V RMS
PCC reference voltage	V_{ref}	215 V RMS
Grid frequency	f_{grid}	50 Hz
Switching frequency	f_{sw}	4000 Hz
Proportional gain	K_p	0.03
Integral gain	K_i	0.002
Inverter-side inductance	L_1	2.22 mH
Filter capacitance	C_f	25 μ F
Grid-side inductance	L_2	1.906 mH
Damping resistance	R_d	5 Ω
Power-switch model	—	IRFP4668 N-channel power MOSFET
Approximate maximum inverter rating	$P_{inv, max}$	1 kW
Voltage-sensor model	—	ZMPT101B
Current-sensor model	—	ZMCT103C
Field-programmable gate array (FPGA) development software	—	Quartus Prime 23.1 Standard Edition
Inductive-load configuration	—	R-L Series Load
Inductive-load resistance	R_L	100 Ω
Inductive-load inductance	L_{load}	0.55 H
Capacitive-load configuration	—	R-C Series Load
Capacitive-load resistance	R_C	16 Ω
Capacitive-load capacitance	C_{load}	0.000022 F

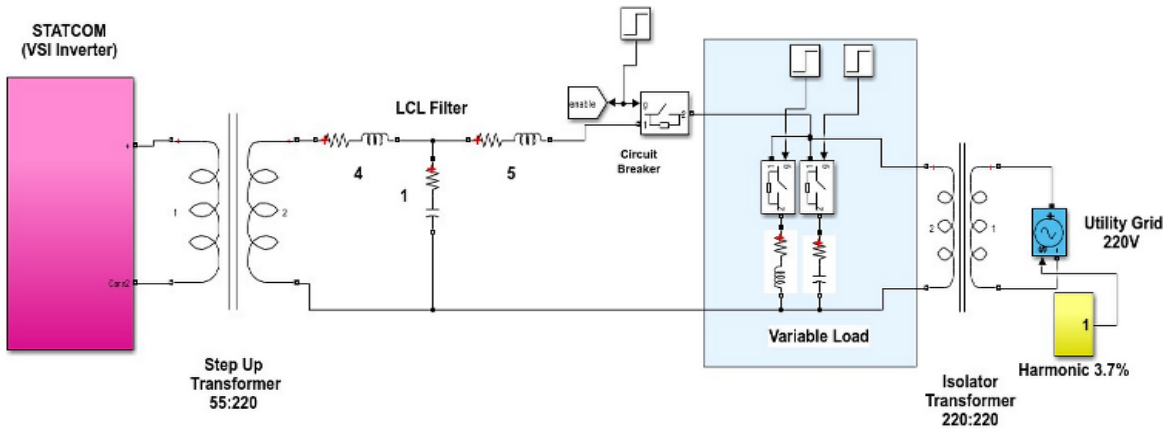


Figure 2. MATLAB/Simulink model of the proposed single-phase static synchronous compensator (STATCOM) system

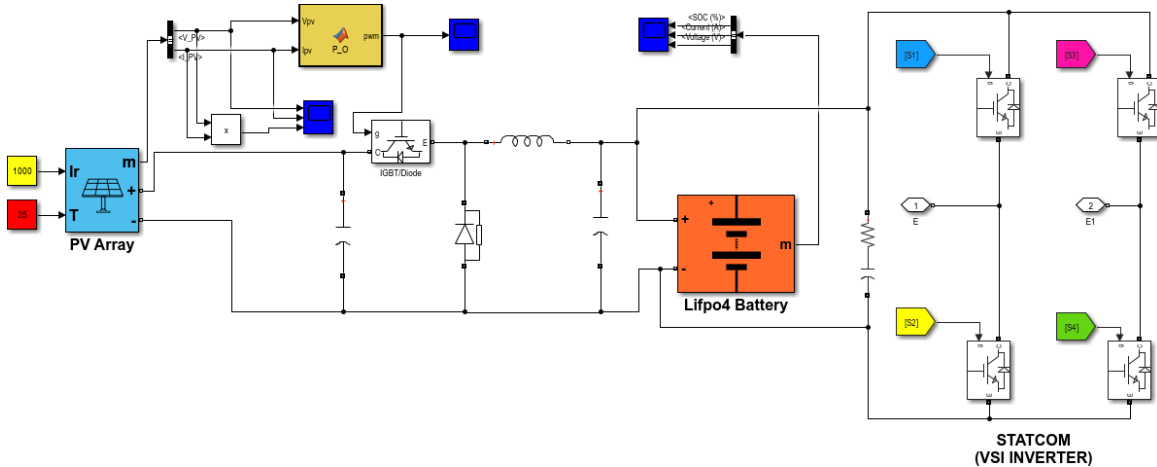


Figure 3. Photovoltaic (PV)/LiFePO₄-battery-supported direct-current (DC) link and single-phase voltage-source inverter (VSI) of the proposed static synchronous compensator (STATCOM)

Table 2. Electrical specifications of PV module

Parameter	Symbol
Model Solar Panel	Jinko Solar
Maximum Power Rated (P_{max})	535 W
Open-Circuit Voltage (V_{oc})	49.6 V
Short-Circuit Current (I_{sc})	13.7 A
Voltage at Maximum Power (V_{mp})	41.5 V
Current at Maximum Power (I_{mp})	12.9 A
Temperature Coefficient of (V_{oc})	-0.28 % / °C
Temperature Coefficient of (I_{sc})	+0.05 % / °C
Number of Cells	144

The generated PV power is calculated as shown in Eq. (2) [18]:

$$P_{PV} = V_{PV} I_{PV} \quad (2)$$

where, P_{pv} is the PV output power, V_{pv} is the PV-array voltage, and I_{pv} is the PV-array current.

2.3 Static synchronous compensator control

The STATCOM control system is implemented on an FPGA platform operating at a clock frequency of 50 MHz. The controller continuously measures the PCC voltage and compares it with the reference value of 215 V RMS. The PCC voltage error is calculated as shown in Eq. (3) [6]:

$$e(t) = V_{ref} - V_{PCC}(t) \quad (3)$$

where, V_{ref} is the reference voltage and V_{PCC} is the measured PCC voltage.

The PI controller output is expressed as shown in Eq. (4) [6]:

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau \quad (4)$$

2.3.1 Proportional–Integral controller tuning and selection

A structured empirical procedure, based on a parameter sweep comparison, was used to retune the PI gains. The control gains were tested in 6 combinations with the same voltage restoration condition. The transient responses were evaluated in terms of voltage overshoot, 98% response time, 2% settling time, steady-state convergence, and the absence of sustained oscillations. Based on these criteria, $K_p = 0.03$ and $K_i = 0.002$ were selected, as summarized in Table 3. A gain combination was considered stable gain combination if the PCC voltage reached the reference value without any oscillations. The transient responses were evaluated in terms of voltage overshoot, 98% response time, 2% settling time, steady-state convergence, and the absence of sustained oscillations. Based on these criteria, $K_p = 0.03$ and $K_i = 0.002$ were selected as the final gains, as summarized in Table 3.

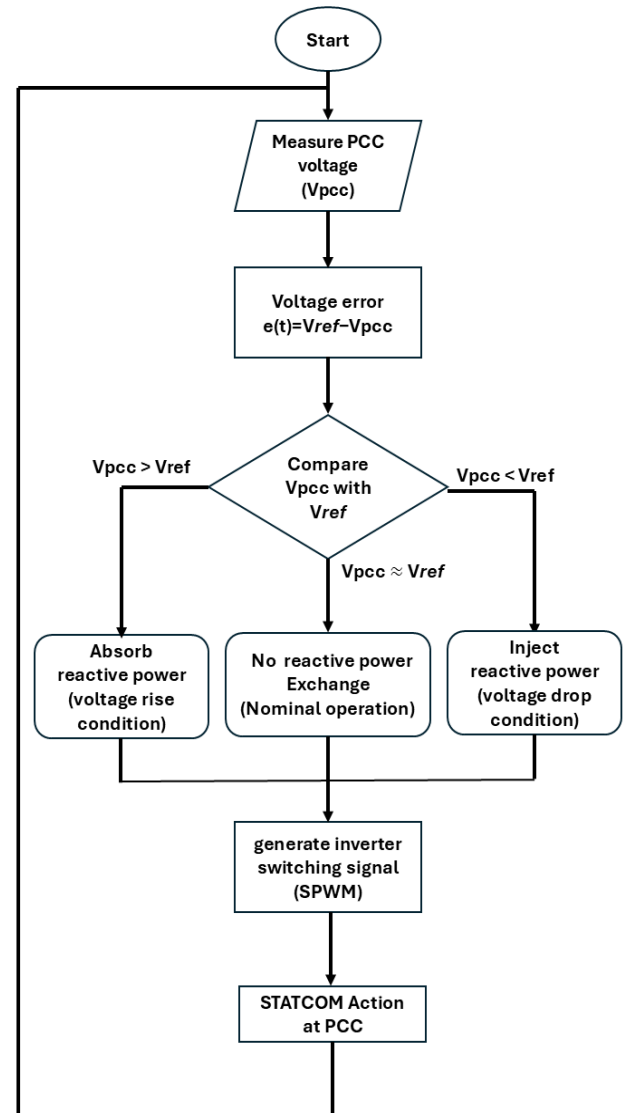
The output of the PI controller is used to regulate the SPWM modulation index [19]. By changing the modulation index, the controller adjusts the fundamental component of the inverter output voltage. When $V_{PCC} < V_{ref}$, the controller increases the inverter output-voltage magnitude, causing the STATCOM to inject reactive power and compensate for the voltage drop. When $V_{PCC} > V_{ref}$, the inverter output-voltage magnitude is reduced, causing the STATCOM to absorb reactive power and mitigate the voltage rise. When $V_{PCC} = V_{ref}$, the reactive power exchange remains small [20].

Table 3. Comparative evaluation of the tested proportional–integral controller gain combinations

K_p	K_i	OS (%)	t_{98} (ms)	$t_{s,2\%}$ (ms)
0.08	0.005	11.79	14.94	65.84
0.07	0.004	25.56	12.33	117.08
0.045	0.005	35.43	12.88	116.70
0.045	0.003	22.94	14.18	87.11
0.03	0.002	11.06	15.18	66.16
0.035	0.0025	17.62	14.64	65.25

Note: K_p : proportional gain; K_i : integral gain; OS: voltage overshoot; t_{98} : 98% response time; $t_{s,2\%}$: settling time within the $\pm 2\%$ band.

Grid synchronization is achieved using a ZCD, which converts the sensed grid voltage into a digital timing signal suitable for FPGA processing. This signal provides the timing reference required to align the inverter operation with the 50Hz grid voltage. The synchronized sinusoidal reference is compared with a triangular carrier operating at 4 kHz to generate the SPWM switching pulses for the full-bridge inverter.

**Figure 4.** Flowchart of the proposed field-programmable gate array (FPGA)-based point-of-common-coupling (PCC) voltage-control strategy

The FPGA platform was selected based on the authors' previous experience and its suitability for real-time converter control. Its parallel architecture enables fast execution of PCC-voltage processing, PI control, grid synchronization, and SPWM generation with deterministic timing [5]. These features improve timing reliability and support the automatic selection of reactive-current injection or absorption, making the FPGA appropriate for the developed prototype.

Figure 4 illustrates the proposed FPGA-based PCC voltage-control strategy. The control sequence starts by measuring the PCC voltage, calculating the voltage error, comparing the measured voltage with the reference value, selecting the required compensation mode, and generating the inverter switching signals. The resulting STATCOM action is then applied at the PCC, and the process is repeated continuously to maintain the voltage close to the reference value.

2.3.2 Field-Programmable gate array implementation details

The controller was implemented on the Intel MAX 10 FPGA device 10M50DAF484C7G available on the DE10-Lite development board. The control architecture was described using very high-speed integrated circuit hardware description language (VHDL) and compiled using Quartus Prime 23.1 Standard Edition. The development board operates with a 50 MHz system clock, while the analog-to-digital converter (ADC) and pulse-width-modulation modules operate with a 10 MHz clock.

The internal 12-bit ADC of the MAX 10 device was used for signal acquisition. The effective conversion rate was approximately 1 MS/s, providing approximately 20,000 raw samples during each 50 Hz grid cycle. A ten-sample moving-average stage generated one filtered output for every ten raw samples, resulting in approximately 2,000 filtered values per grid cycle.

The sinusoidal pulse-width-modulation generator employed 4096-point lookup tables for the numerical sinusoidal and triangular waveforms, corresponding to a 12-bit numerical resolution. For the 50 Hz sinusoidal reference, this represents a time increment of approximately 4.883 μ s and an angular increment of approximately 0.0879°. The 10 MHz pulse-width-modulation clock provides a switching-edge timing granularity of 0.1 μ s. At the adopted switching frequency of 4 kHz, each switching period contains 2500 clock intervals, corresponding to a nominal duty-ratio timing resolution of approximately 0.04%.

The successful Quartus compilation report showed a utilization of 12,182 out of 49,760 logic elements (24%), 487 registers, 42 out of 360 pins (12%), 768 out of 1,677,312 memory bits (less than 1%), four out of 288 embedded 9-bit multipliers (1%), one out of four phase-locked loops (25%), and one out of two internal ADC blocks (50%). The results show that the designed architecture is feasible with the available resources in the chosen FPGA device.

3. SIMULATION RESULTS

The proposed single-phase STATCOM was evaluated in MATLAB/Simulink under capacitive, inductive, and dynamic load-switching conditions. In the capacitive and inductive cases, the load was connected at $t = 1$ s, while the STATCOM was activated at $t = 2$ s. The simulation results were evaluated based on PCC voltage restoration, reactive-power exchange, compensation-current direction, and DC-link behavior.

3.1 Capacitive-load operation

When the capacitive load was connected at $t = 1$ s, the PCC voltage increased from approximately 215 V to 219 V RMS. This voltage rise occurred because of the excess reactive power introduced by the capacitive load. After the STATCOM was activated at $t = 2$ s, the controller reduced the inverter output-voltage magnitude, causing the STATCOM to operate in reactive-power absorption mode. As a result, the PCC voltage was reduced and restored to approximately 215 V RMS, as shown in Figure 5.

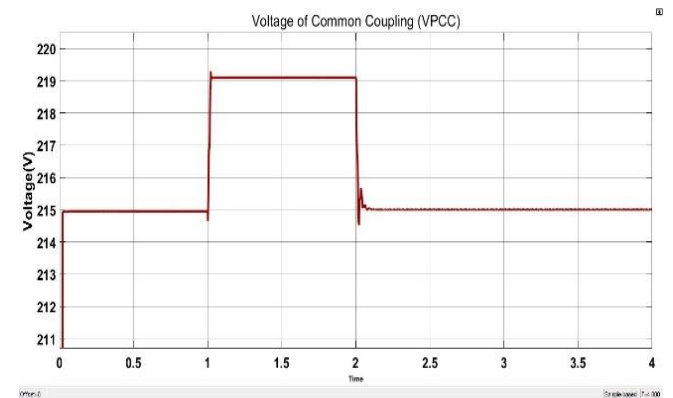


Figure 5. Simulated point-of-common-coupling (PCC) voltage before and after static synchronous compensator (STATCOM) activation under capacitive loading

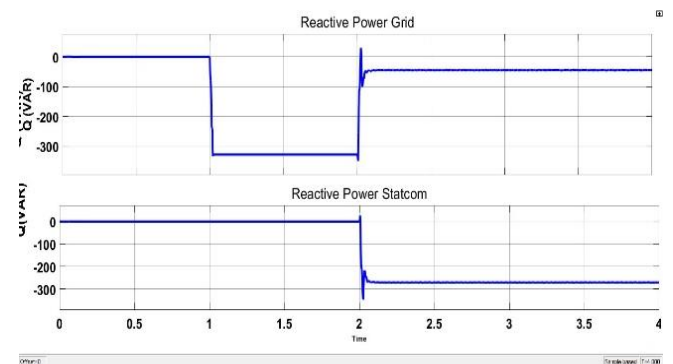


Figure 6. Simulated reactive-power response of the grid and static synchronous compensator (STATCOM) under capacitive loading

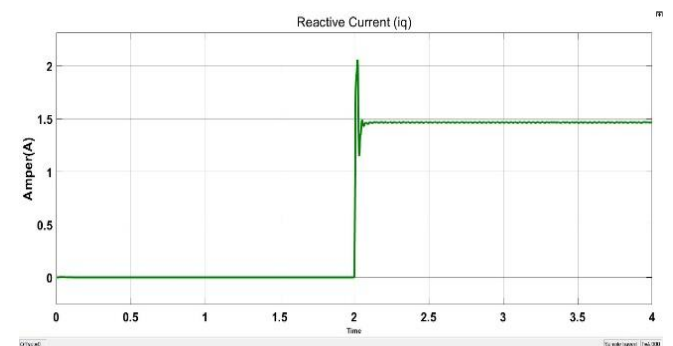


Figure 7. Reactive current absorbed by the static synchronous compensator (STATCOM) under capacitive loading

The reactive-power response under capacitive loading is shown in Figure 6. Before compensation, the capacitive load

caused a voltage rise at the PCC. After STATCOM activation, the compensator absorbed approximately 327VAR from the system. This confirms that the STATCOM selected the correct compensation direction to mitigate the voltage rise.

The corresponding STATCOM reactive-current waveform is shown in Figure 7. The absorbed reactive current reached approximately 1.47 A after the compensator was activated. The current direction confirms that the STATCOM operated in inductive mode during the capacitive-load condition.

3.2 Inductive-load operation

The inductive-load case was simulated to evaluate the ability of the proposed STATCOM to compensate for a voltage-drop condition at the PCC. As shown in Figure 8, the PCC voltage was initially maintained close to the reference value of 215V RMS. When the inductive load was connected at $t = 1$ s, the PCC voltage decreased to approximately 212 V RMS because of the increased reactive-power demand. After the STATCOM was activated at $t = 2$ s, the controller increased the inverter output-voltage magnitude, causing the STATCOM to operate in reactive-power injection mode. Consequently, the PCC voltage was restored to approximately 215 V RMS, with only a small transient overshoot during the compensation process.

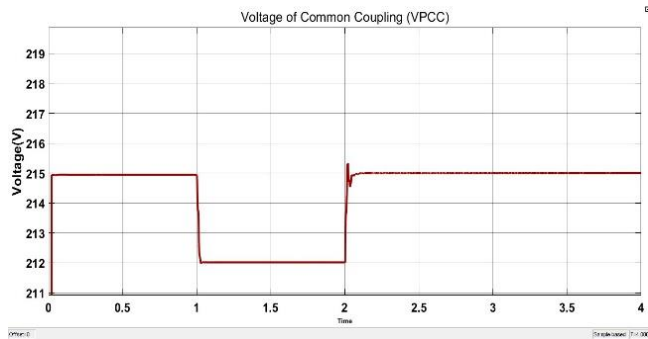


Figure 8. Simulated point-of-common-coupling (PCC) voltage before and after static synchronous compensator (STATCOM) activation under inductive loading

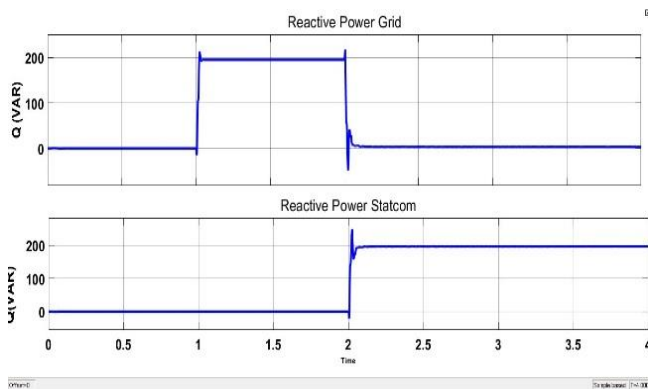


Figure 9. Simulated reactive-power response of the grid and static synchronous compensator (STATCOM) under inductive loading

The reactive-power response under inductive loading is shown in Figure 9. Before STATCOM activation, the grid supplied approximately 195 VAR to the inductive load. After the STATCOM was activated at $t = 2$ s, the reactive power supplied by the grid decreased significantly, while the

STATCOM injected approximately 210 VAR. This response confirms that the compensator supplied the required reactive power locally and reduced the reactive-power burden on the utility grid.

The corresponding reactive-current waveform is shown in Figure 10. Before STATCOM activation, the compensating current was approximately zero. After activation at $t = 2$ s, the STATCOM current increased rapidly and settled at approximately 1.16 A after a short transient. This confirms capacitive-mode operation and verifies that the proposed controller produced the required reactive-current direction to compensate for the voltage drop caused by the inductive load.

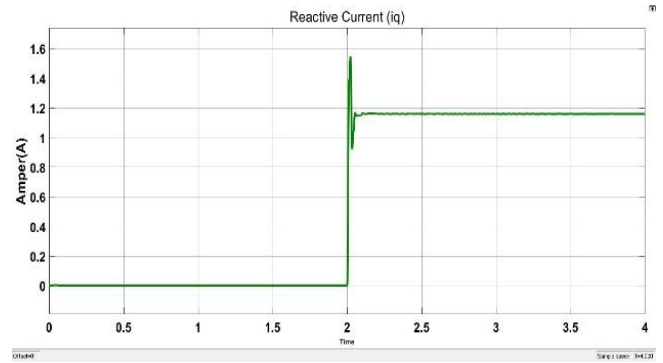


Figure 10. Reactive current injected by the static synchronous compensator (STATCOM) under inductive loading

3.3 Dynamic load-switching operation

The dynamic load-switching case was simulated to test the STATCOM's performance in switching between voltage control situations of voltage rise and voltage drop. During the simulation, the load condition was modified in this test to simulate both capacitive and inductive operating modes. The STATCOM was turned on at time ($t = 1$) s, and the capacitive load and the inductive load were switched on at times ($t = 2$) s and ($t = 3$) s, respectively. The controller changed the compensation mode when PCC voltage deviation occurred, based on the load condition. When the capacitive loading condition caused the PCC voltage to rise above the reference value, the STATCOM operated in reactive-power absorption mode. When the inductive loading condition caused the PCC voltage to fall below the reference value, the STATCOM changed to reactive-power injection mode. As shown in Figure 11, the PCC voltage returned close to the reference value of 215 V RMS after each load transition.

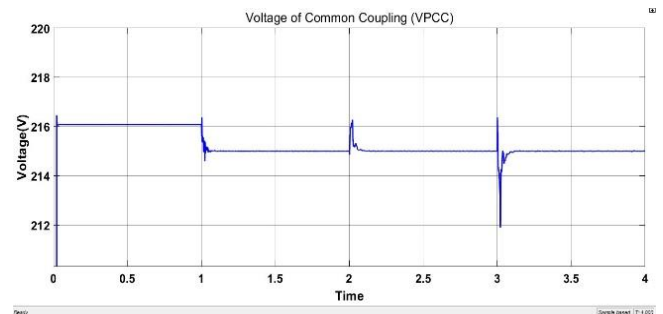


Figure 11. Simulated point-of-common-coupling (PCC) voltage response to static synchronous compensator (STATCOM) activation and successive capacitive- and inductive-load insertions

To quantify the dynamic performance, the peak voltage deviation, recovery time, and settling time were calculated for each switching event, as summarized in Table 4. The proportional action accelerates voltage correction, whereas the integral action eliminates the residual steady-state error. Although excessive gains may increase overshoot or produce oscillations, the selected gains returned the PCC voltage to its reference without sustained oscillations.

Table 4. Quantitative performance indices of the simulated dynamic load-switching response

Event	t_e (s)	ΔV_{peak} (%)	t_{98} (ms)	$t_{s,2\%}$ (ms)
STATCOM Action	1	0.6369	14.48	66.46
Capacitive Load	2	0.5936	84.34	98.021
Inductive Load	3	1.4410	35.781	84.767

Note: t_e : event time; ΔV_{peak} : peak voltage deviation; t_{98} : 98% response time; $t_{s,2\%}$: settling time within the $\pm 2\%$ band; STATCOM: static synchronous compensator.

Figure 12 presents the simulated battery response during dynamic load switching. The battery current varied with the switching events, while the battery voltage remained within a narrow range and the state of charge changed only slightly during the short simulation period. These results indicate DC-side support within the simulation model; however, no time-resolved experimental battery measurement was available, and no experimental claim is therefore made regarding its transient performance.

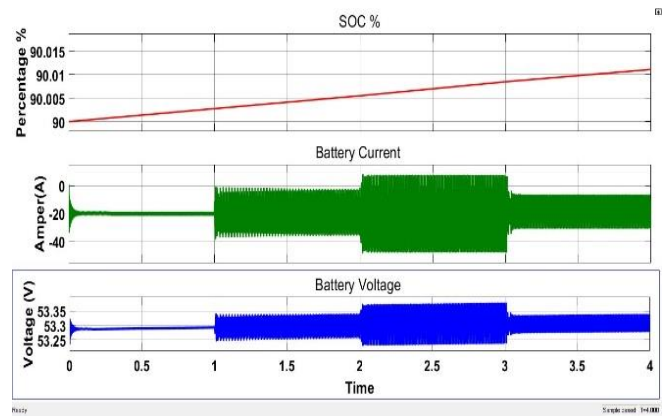


Figure 12. Simulated battery state of charge, current, and voltage under dynamic load-switching conditions

3.4 Influence of the inductor–capacitor–inductor filter on the output-voltage waveform

The results of the simulation of the voltage waveform are compared in Figure 13 with and without LCL filter. If no filter is used, the voltage waveform will contain a high-frequency switching ripple, which superimposes on the basic voltage waveform. This ripple is greatly reduced after the application of the LCL filter and the output is close to sinusoidal. The two inductors reduce the high frequency components, the filter capacitor allows the switching-frequency components to pass with low impedance and the damping resistor reduces filter resonance [17].

The adopted switching frequency involves a practical trade-off. Increasing it generally improves waveform quality and allows faster control updates, but increases semiconductor switching losses. Therefore, 4 kHz was selected as a practical

operating compromise for the prototype rather than as an optimized value.

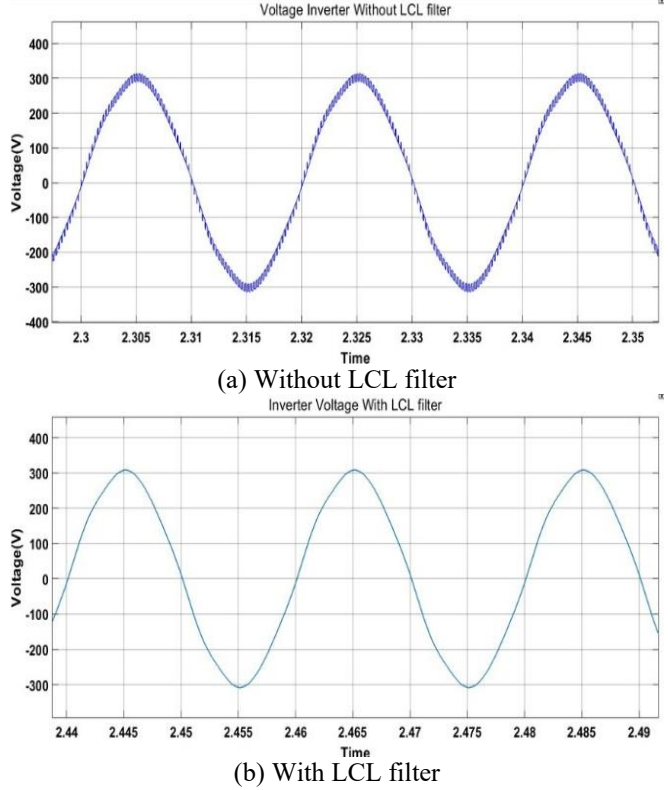


Figure 13. Simulated voltage waveforms before and after inductor–capacitor–inductor (LCL) filtering: (a) at the step-up-transformer output without the filter and (b) an LC filter

4. EXPERIMENTAL RESULTS

4.1 Experimental setup

To verify the simulation results under the laboratory operating conditions, the proposed FPGA-controlled single-phase STATCOM was implemented experimentally. The practical system is comprised of a PV-supported DC bus, a LiFePO₄ battery, a single-phase full-bridge voltage-source inverter, metal-oxide-semiconductor field-effect transistor (MOSFET) gate-driver circuits, a step-up transformer, an LCL filter, an isolation transformer, voltage and current sensors, a ZCD circuit and an FPGA-based control unit.

The experimental prototype is summarized of the principle electrical, control, hardware and load parameters shown in Table 1. The inverter power-switch model, the inverter rating, the voltage- and current-sensor models, the FPGA development software, and the actual inverter power-switch and load (inductive and capacitive) values and connections are identified in the table. The same values of load components were applied to the simulation model and to the lab set-up. For the experimental tests, the shunt connection of the inductive and capacitive load sections was made at the PCC and the load sections were energized separately. The STATCOM was connected in shunt at the PCC [21], while inductive and capacitive loading conditions were applied using a manual load selector [22]. The PCC voltage was measured and fed back to the FPGA controller. The controller processed the voltage error using the PI control algorithm and generated the SPWM switching signals required to drive the inverter. The

inverter output was then connected to the PCC through the step-up transformer and LCL filter, allowing the STATCOM to inject or absorb reactive current according to the loading condition. The practical experimental setup of the proposed STATCOM is shown in Figure 14.

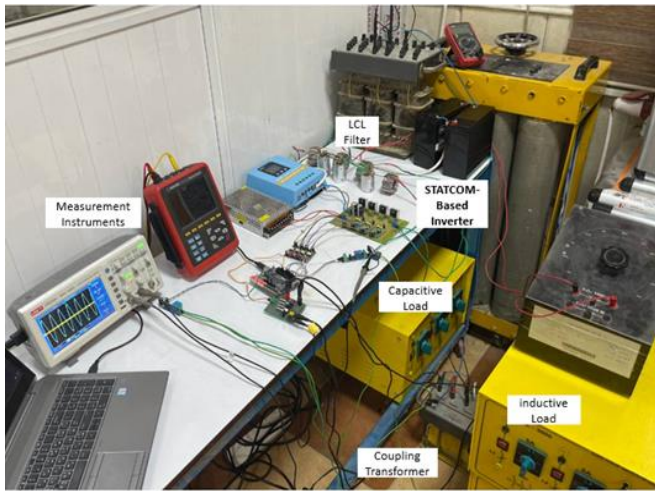


Figure 14. Photograph of the practical setup of the field-programmable gate array (FPGA)-controlled single-phase static synchronous compensator (STATCOM)

4.2 Direct-current link and synchronization verification



Figure 15. Measured direct-current (DC)-link voltage of the photovoltaic (PV)/LiFePO₄-battery-supported source

Before evaluating the voltage-regulation performance, the DC-link voltage was measured, as shown in Figure 15, to verify the availability of the inverter-side DC supply. The measured value closely agreed with the simulated level, confirming that the PV/LiFePO₄ subsystem provided the required operating voltage under the tested steady-state conditions. This measurement verifies only DC-side voltage availability and does not constitute an experimental assessment of the transient performance of the battery or MPPT controller. The synchronization between the grid voltage and the STATCOM output voltage was experimentally verified using an oscilloscope, as shown in Figure 16. The measured waveforms indicate that both voltages operate at the same frequency and exhibit close phase alignment. This confirms the practical operation of the synchronization stage and indicates that the zero-crossing-based control provided a suitable timing reference for FPGA-

based SPWM generation under the tested laboratory conditions.

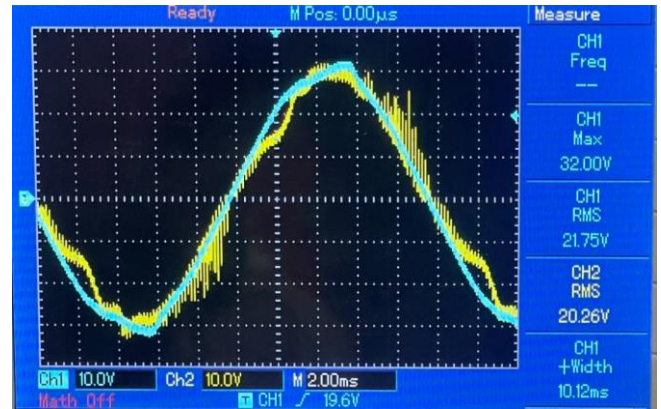


Figure 16. Experimental verification of synchronization between the grid voltage and static synchronous compensator (STATCOM) output voltage

4.3 Experimental voltage regulation under inductive loading

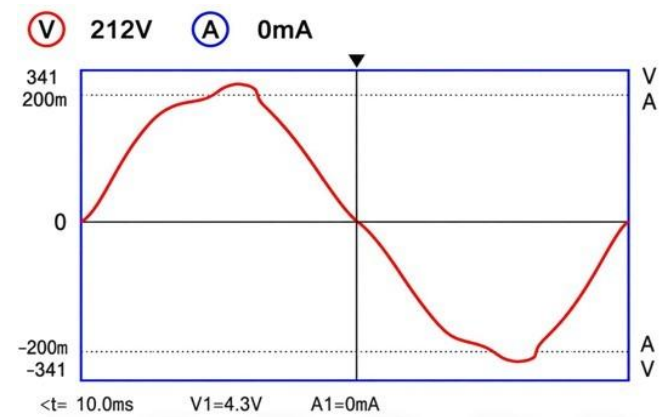


Figure 17. Experimental point-of-common-coupling (PCC) voltage under inductive loading before static synchronous compensator (STATCOM) compensation

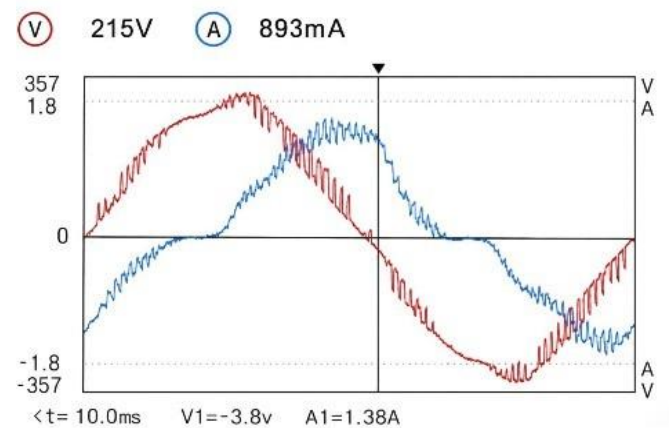


Figure 18. Experimental point-of-common-coupling (PCC) voltage and static synchronous compensator (STATCOM) current after compensation under inductive loading

The inductive-load test was performed to evaluate the ability of the proposed STATCOM to compensate for a PCC

voltage-drop condition. Before compensation, the inductive load caused the PCC voltage to decrease to approximately 212V RMS as shown in Figure 17. This reduction was caused by the increased reactive-power demand of the inductive load. After STATCOM activation, the FPGA controller increased the inverter output-voltage magnitude, causing the compensator to operate in reactive-power injection mode. Consequently, the PCC voltage was restored to 215 V RMS, with a measured STATCOM current of 0.893 A, as shown in Figure 18.

After STATCOM activation, the FPGA controller increased the inverter output-voltage magnitude, causing the compensator to operate in reactive-power injection mode. Consequently, the PCC voltage was restored to 215 V RMS, with a measured STATCOM current of 0.893 A. This confirms that the prototype injected reactive current in the required direction to compensate for the voltage drop.

4.4 Experimental voltage regulation under capacitive loading

The capacitive-load test was performed to evaluate the ability of the proposed STATCOM to compensate for a PCC voltage-rise condition. Before compensation, the capacitive load increased the PCC voltage to approximately 219 V RMS, as shown in Figure 19, which is higher than the reference value of 215 V RMS.

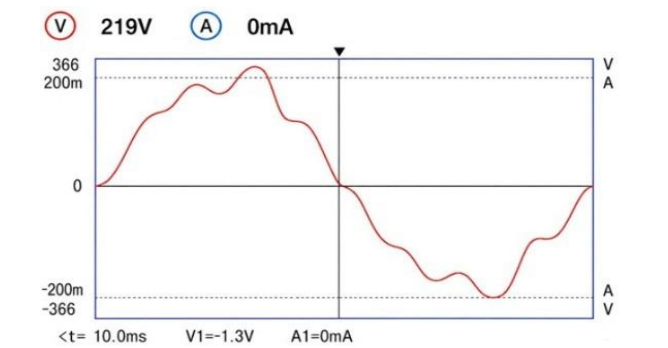


Figure 19. Experimental point-of-common-coupling (PCC) voltage under capacitive loading before static synchronous compensator (STATCOM) compensation

After STATCOM activation, the FPGA controller reduced the inverter output-voltage magnitude, causing the

compensator to operate in reactive-power absorption mode. Consequently, the PCC voltage was restored to approximately 215 V RMS, with a measured STATCOM current of 0.853 A, as shown in Figure 20. This confirms that the prototype absorbed reactive current in the required direction to mitigate the voltage rise.

The experimental results showed the same compensation behavior observed in simulation. In both cases, the STATCOM restored the PCC voltage to the reference value under inductive and capacitive loading conditions. Under inductive loading, the system operated in reactive-power injection mode and increased the PCC voltage from approximately 212V RMS to 215V RMS. Under capacitive loading, it operated in reactive-power absorption mode and reduced the PCC voltage from approximately 219V RMS to 215V RMS. Although the measured STATCOM current was lower than the simulated value because of the practical current and thermal limits of the laboratory prototype, the voltage-restoration behavior and compensation direction were consistent with the simulation results.

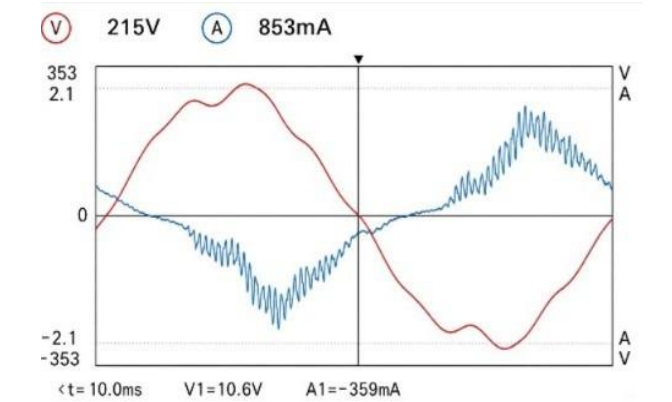


Figure 20. Experimental point-of-common-coupling (PCC) voltage and static synchronous compensator (STATCOM) current after compensation under capacitive loading

4.5 Simulation–experiment validation

Table 5 presents a quantitative comparison between the simulation and experimental results in terms of PCC voltage regulation, compensation current, DC-link voltage, and steady-state regulation error.

Table 5. Quantitative comparison between simulation and experimental results

Operating Scenario	Simulation Result	Experimental Result
PCC voltage under normal operating condition (RMS)	215 V	215 V
PCC voltage under inductive load before compensation (RMS)	212 V	212 V
PCC voltage under capacitive load before compensation (RMS)	219 V	219 V
PCC voltage after compensation under both loading conditions (RMS)	215 V	215 V
Compensation current under inductive loading (RMS)	1.16 A	0.893 A
Compensation current under capacitive loading (RMS)	1.47 A	0.853 A
DC-link voltage during operation (V _{DC})	53 V	52.3 V
Steady-state voltage-regulation error after compensation (%)	≈ 0	≈ 0

4.6 Experimental harmonic-performance evaluation

The experimental harmonic performance was evaluated under normal operation, reactive-power absorption, and reactive-power injection. Figures 21-23 present the measured PCC-voltage and STATCOM-current waveforms together

with their corresponding total harmonic distortion (THD) values. The PCC-voltage THD values were 3.8%, 3.9%, and 4.9% under normal, absorption, and injection conditions, respectively. The corresponding STATCOM-current THD values were 6.7% during absorption and 11.2% during injection. Current THD was not applicable during normal

operation because the STATCOM current was approximately zero.

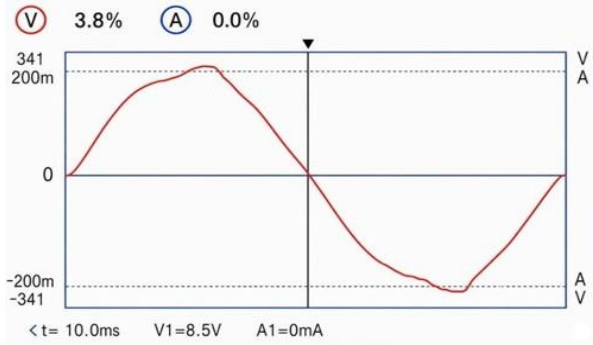


Figure 21. Measured point-of-common-coupling (PCC) voltage waveform and total harmonic distortion (THD) during normal grid operation

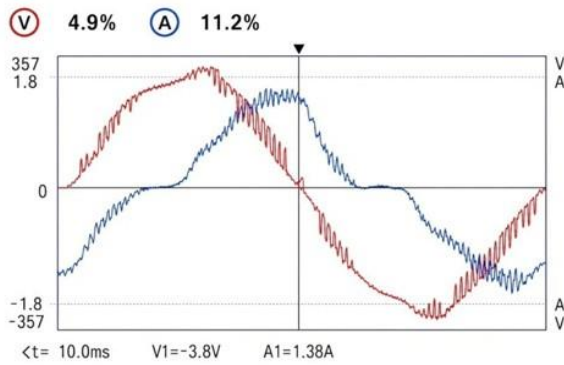


Figure 22. Measured point-of-common-coupling (PCC) voltage and static synchronous compensator (STATCOM) current waveforms and total harmonic distortion (THD) during reactive-power injection

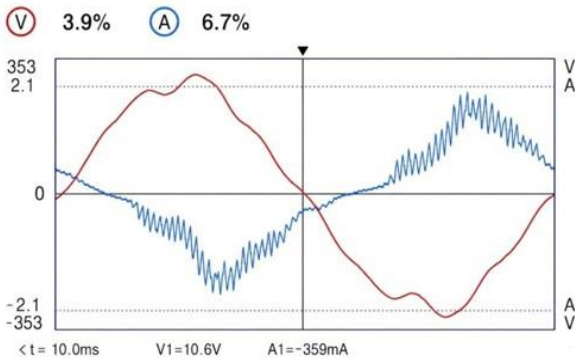


Figure 23. Measured point-of-common-coupling (PCC) voltage and static synchronous compensator (STATCOM) current waveforms and total harmonic distortion (THD) during reactive-power absorption

5. CONCLUSION

This paper presented the design, simulation, and laboratory validation of an FPGA-controlled single-phase STATCOM for PCC-voltage regulation under inductive and capacitive loading conditions. The PV/LiFePO₄ subsystem provided inverter-side DC-link support through the MPPT charge controller and remained independent of the PCC-voltage control loop. The simulation and experimental results

demonstrated consistent voltage-restoration behavior through reactive-current injection under inductive loading and reactive-current absorption under capacitive loading, confirming the feasibility of the proposed control system under the tested laboratory conditions.

The study is limited to a low-power single-phase prototype. The available experimental validation covers steady-state inductive and capacitive loading, whereas dynamic load switching was evaluated only through simulation. Furthermore, the fixed-gain PI controller may require retuning under wider operating conditions. Future work will include higher-power and three-phase implementation, experimental dynamic load-switching tests using synchronized high-speed voltage and current data acquisition, and adaptive or advanced control techniques to improve transient performance.

ACKNOWLEDGMENT

The authors would like to thank Northern Technical University, Technical Engineering College of Mosul, for providing the laboratory facilities and technical support required to carry out the experimental part of this work. The authors also express their appreciation to the Department of Electrical Power Engineering Techniques for its assistance during the implementation and testing of the proposed STATCOM prototype.

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NOMENCLATURE

C_f	LCL-filter capacitance
C_{load}	Capacitive-load capacitance
$e(t)$	PCC-voltage error
f_{clk}	FPGA system-clock frequency
f_{grid}	Grid frequency
f_{sw}	Inverter switching frequency
I_{mp}	Current at the maximum power point
I_{PV}	Photovoltaic-array current
I_{sc}	Short-circuit current of the photovoltaic module
K_i	Integral gain of the proportional-integral controller
K_p	Proportional gain of the proportional-integral controller
L_1	Inverter-side filter inductance
L_2	Grid-side filter inductance
L_{load}	Inductive-load inductance
C_{load}	Capacitive-load Capacitive
OS	Voltage overshoot
$P_{inv,max}$	Maximum inverter power rating
P_{max}	Maximum power of the photovoltaic module
P_{PV}	Photovoltaic-array output power
Q	Reactive power
R_C	Capacitive-load resistance
R_d	LCL-filter damping resistance
R_L	Inductive-load resistance
t	Time
t_e	Switching-event time
t_{98}	98% response time
$t_{s,2\%}$	Settling time within the $\pm 2\%$ band
$u(t)$	Proportional-integral controller output
V_{grid}	Grid voltage
V_{inv}	Inverter output voltage
V_{mp}	Voltage at the maximum power point
V_{oc}	Open-circuit voltage of the photovoltaic module
V_{PCC}	Voltage at the point of common coupling
V_{PV}	Photovoltaic-array voltage
V_{ref}	PCC reference voltage
X	Coupling reactance
ΔV_{peak}	Peak voltage deviation
φ	Phase difference between the inverter and PCC voltages
τ	Integration variable