



Design of a Class-J GaN Power Amplifier with Compensation Capacitance Technique for 5G NR n78 Applications

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ABSTRACT

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The rapid deployment of 5G New Radio (NR) macro base stations, especially in the sub-6 GHz n78-band, calls for radio frequency (RF) front-ends that can deal with the ruthless linearity-efficiency trade-off required by large peak-to-average power ratio (PAPR). In order to amplify the Orthogonal Frequency-Division Multiplexing (OFDM) signals with a center frequency of 3.5 GHz and 200 MHz bandwidth, the power amplifier (PA) needs to provide high linearity with high efficiency over the whole operation band without degradation. In this paper, we present a Class-J Gallium Nitride (GaN) broadband PA design utilizing a systematic approach targeting 3.5 GHz center operating frequency with the Macom CGH40010F packaged devices, and then the proposed compensation capacitance method was used to physically absorb the dominant drain-source parasitic capacitance (C_{ds}) in order to correctly locate and compensate the inherent current generator plane. By integrating AI-extrapolated load-pull data to define optimal large-signal impedance targets with a simultaneous multidimensional optimization approach, an optimized double-stub matching network (MN) is realized. The amplifier achieves a 66.2% power-added efficiency (PAE), a drain efficiency (DE) of 75.8%, and 41.6 dBm delivered output power. Two-tone intermodulation with a 1 MHz spacing at a 20 dBm available source power was conducted to validate the large-signal linearity. The amplifier achieved an Output Third-Order Intercept Point (OIP3) of 50.7 dBm, corresponding to a 9 dB power margin above saturation. The robust performance of broadband stability is displayed, maintaining optimal waveform shaping and performance across a 200 MHz bandwidth (3.4–3.6 GHz). The proposed approach successfully balances the device nonlinearities and provides a highly efficient, linear, and computationally robust design baseline for advanced 5G macro base station front-ends.

1. INTRODUCTION

Modern wireless communication systems that employ complex schemes combining both amplitude and phase modulations have an intrinsic high peak-to-average power ratio (PAPR) [1]. The theoretical basis for the Class-J amplifier was established in influential papers, which showed that the traditional Class-B mode could be pushed into a continuous design space. They added a reactive component at the fundamental frequency and also terminated the 2nd harmonic with some specific capacitance; they achieved a voltage waveform with a phase shift relative to the current. This “Class-J” mode retained the efficiency and linearity of a Class-B amplifier but across a much greater bandwidth. Continuous-mode Class-J amplifiers can be a powerful solution to the inherent efficiency-bandwidth trade-off using adjustment of voltage and current waveforms across a continuum of reactive loads [2-4]. High Electron Mobility Transistors (HEMTs) based on Gallium Nitride (GaN) are the preferred semiconductor technology for these implementations because of their superior power density, high breakdown voltage, as well as excellent high-frequency

performance [5]. However, the realization of an optimal broadband Class-J matching network (MN) relies on accurately targeting the intrinsic current generator plane. One of the primary design bottlenecks is the proper output node de-embedding of the dominant drain-source parasitic capacitance (C_{ds}). Although prior foundational studies and recent refinement search for different compensatory networks that can accommodate this parasitic, such methods often rely on iteratively tuned empirical approximation to harmonic termination [6-9].

Moon et al. [6] investigated Class-J power amplifier (PA) with linear and nonlinear output capacitors (C_{out}). They showed that the nonlinear C_{out} induces second-harmonic voltage components, resulting in a lower voltage-current phase difference than 45° and allowing inefficiencies to become smaller compared to the linear case. At 2.14 GHz, a PA is proposed with saturation of use through a pure resistive load for the fundamental, and obtaining an efficiency of 77.3% power-added efficiency (PAE) at 40.6 dBm without dedicated harmonic control circuitry. Saxena et al. [7] presented a broadband continuous Class-B/J PA design using a model-based nonlinear embedding technique. By observing the

variation of parameter α against frequency, they resolved the anti-clockwise impedance rotation problem at the extrinsic plane, enabling Foster-realizable MNs. A 15 W GaN HEMT prototype over the frequency range of 1.3–2.4 GHz demonstrated 63–72% drain efficiency (DE) over a fractional bandwidth of 59%, indicating the technique's utility for broadband high-efficiency PA design. Zhang et al. [8] developed a design technique of broadband Class-J PAs to exploit the relationship between DE and the ratio of drain-source capacitance to load impedance (XC_{ds}/RL). An external compensation circuit was used to keep this ratio in the high-efficiency range across a wide bandwidth. The fabricated PA achieves 60–68% DE and 40.0–41.5 dBm output power from 1.4 to 3.6 GHz, representing approximately 88% fractional bandwidth using a Wolfspeed CGH40010F GaN HEMT. Wang et al. [9] presented a Class-J PA incorporating an external compensatory capacitor to further optimize the second-harmonic-to-fundamental voltage ratio beyond what the intrinsic nonlinear C_{out} alone can achieve. This method reduces the voltage-current phase difference at the drain, thus reducing transistor power dissipation. The simulations with the unpackaged CGH60015D showed 88.7% efficiency, and a packaged CGH40010 at 2.4 GHz demonstrated 76% DE, confirming that the compensatory capacitor approach allows for efficient design of high-efficiency Class-J PAs. This challenge is significantly enlarged in 5G New Radio (NR) networks operating within the sub-6 GHz n78 band. In order to support very high data rates over wide bandwidth channels like the 200 MHz channel supported by 5G NR, advanced Orthogonal Frequency-Division Multiplexing (OFDM)-based modulation schemes with even higher PAPR are employed. Thus, the key issue from a design point of view for these macro base stations lies in the trade-off between linearity and efficiency, which is a generic concern in radio frequency (RF) front-end architectures. Therefore, the mathematical and physical realization of the exact intrinsic second-harmonic impedance needed to perform Class-J operation over a desired passband (e.g., 5G n78 band) is nontrivial [10–12].

A critical investigation of recent literature focused specifically on the sub-6 GHz n78 band reveals distinct technological gaps that remain unaddressed for packaged devices. For instance, while Chiou et al. [10] developed a continuous Class-J quasi-MMIC for the n77/n78 band, their architecture relies on expensive, non-standard GaAs IPD foundry integration, yielding a peak PAE of only 39.5%, and lacks an automated, reproducible workflow to absorb standard packaged device parasitics. Boumalkha et al. [11] introduced a filtering PA using the packaged CGH40010F device near 3.0 GHz; however, their synthesis relies on complex multi-mode resonators without providing strict in-band efficiency thresholds or evaluating large-signal linearity under compression. Similarly, Gao et al. [12] designed a tunable Class-J PA for the 3.3–4.2 GHz band, but their approach depends on varactor-based dynamic matching rather than a passive, broadband C_{ds} compensation technique, and omits standard intermodulation linearity metrics. Most importantly, none of these existing works provides a reproducible characterization workflow that links continuous-variable impedance extraction with simultaneous multidimensional MN optimization. To bridge these specific gaps, this paper introduces a reproducible large-signal behavioral characterization and MN synthesis methodology explicitly optimized for 5G NR n78 applications (3.4–3.6 GHz) using the commercially available packaged Macom CGH40010F

GaN HEMT. The proposed approach utilizes an AI-extrapolated continuous load-pull workflow to synthesize a physically realizable double-stub microstrip matching topology. This distributed network completely absorbs the non-linear drain-source capacitance (C_{ds}) and internal package parasitics. Consequently, this design secures an exceptional, verified in-band floor performance (PAE 56.8%, Output Power 41.0 dBm) across the entire 200 MHz passband, and validates large-signal linearity through a highly symmetrical two-tone Output Third-Order Intercept Point (OIP3) of 50.7 dBm, establishing a robust, computationally optimized baseline for modern macro base station front-ends. To address this, this paper proposes a systematic compensation capacitance technique synergized with AI-extrapolated load-pull data [13] and multidimensional optimization [14]. An optimized double-stub MN is designed to fully absorb C_{ds} parasitic, ensuring ideal Class-J waveform shaping from 3.4 GHz to 3.6 GHz. This research is structured through the introduction, which outlines its significance. The theoretical and compensation capacitance method of designing a Class-J amplifier will be explained in Section 2, while implementation details will also be explained in Section 3. The results and conclusion will be found in Sections 4 and 5, respectively.

2. THEORETICAL METHODOLOGY OF CLASS-J AND COMPENSATION TECHNIQUE

2.1 Continuous Class-J waveform theory

The continuous Class-J is theoretically described as enlarging the very high-efficiency range of Class-B, adding a reactive element as fundamental load with purely reactive impedance at the second harmonic. According to the well-known definitions of continuous mode, the intrinsic drain-source voltage (V_{ds}) waveform can be mathematically expressed as mentioned in a previous study [15]:

$$V_{ds}(\theta) = V_K + (V_{DD} - V_K)(1 - \sin \theta)(1 - \alpha \cos \theta) \quad (1)$$

Here, V_{DD} is the drain DC supply, V_K is the knee voltage, and α is a design parameter ranging from -1 to 1. To successfully shape this waveform, the intrinsic fundamental (Z_{f0}) and second harmonic (Z_{2f0}) impedances at the current generator plane must satisfy the following criteria [15]:

$$\begin{cases} Z_{f0} = \frac{R_{opt}(1 + j\alpha)}{\beta} \\ Z_{2f0} = -j \frac{3\pi \alpha R_{opt}}{8\beta} \end{cases} \quad (2)$$

where, β represents the driven level factor ranging from 0 to 1. Practically, the knee clipping should be avoided, then the scale of β is slightly adjusted to a value lower than unity, leading to a decrease in efficiency. The optimum load impedance (R_{opt}) is defined theoretically by [15]:

$$R_{opt} = 2(V_{DD} - V_K)/I_{max} \quad (3)$$

For the selected CGH40010F GaN HEMT, the device datasheet constraints are $V_{DD} = 28$ V, $V_K = 4$ V, and $I_{max} = 1.5$ A, yielding a theoretical optimum load of $R_{opt} = 32 \Omega$. Through demanding Advanced Design System (ADS) simulation, the

physical optimal fundamental load was extracted as $R_{opt} = 31.87 \Omega$, demonstrating excellent agreement with the theoretical.

2.2 Nonlinear drain-source capacitance (C_{out} or $C_{ds}(V_{ds})$) dynamics

To realize these intrinsic targets in a physical GaN HEMT device, the effects of the packaging parasitics must be included in the design. In Figure 1, C_{out} or $C_{ds}(V_{ds})$ primarily separates the intrinsic generator plane from the extrinsic package plane because it sits in parallel to the external MN.

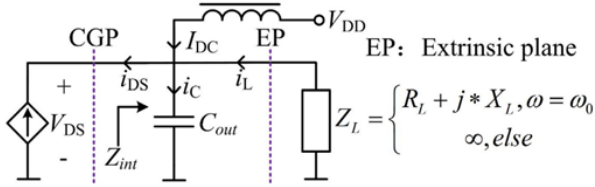


Figure 1. Schematic of continuous Class-B/J power amplifier (PA) [15]

This defines all non-linear capacitors, which might exist on the output of a transistor as a drain-source capacitor or a gate-drain capacitor. C_{ds} and C_{gs} are also a modulated function of the drain-source and the gate-source voltages, but in this model, they distinct consider their dependency on the V_{ds} . Thus, C_{out} is expressed as [6, 8]:

$$C_{out}(V_{ds}) = C_{out0} + A \cdot [1 + \tanh(B \cdot V_{ds} + C)] \text{ [pF]} \quad (4)$$

where, Table 1 demonstrates the value of C_{out0} , A , B , and C .

Table 1. Summary of parameters for the output capacitor (C_{out}) [8]

C_{out0}	A	B	C
0.95	1192.4	-0.0594714	-2.94696

The dependency of the drain voltage and output capacitance is shown in Figure 2 by Eq. (4). The output capacitance of the transistor is a non-linear function decay for small V_{ds} (the value should be approximately less than about 28 V). Capacitance becomes constant (1.185 pF) going beyond $V_{ds} = 28$ V.

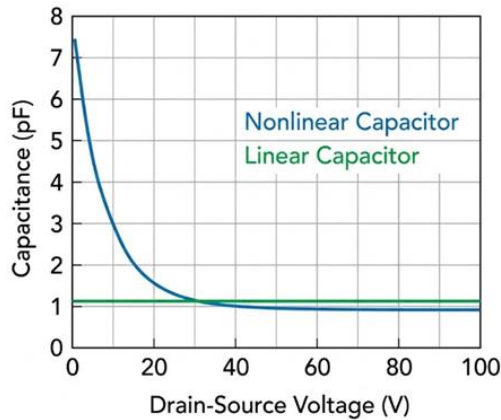


Figure 2. Linear and nonlinear capacitances (C_{out}) [8]

The nonlinearity property versus V_{ds} was illustrated in

Figure 2. When the V_{ds} voltage has insignificant values, the capacitance grows rapidly.

2.3 C_{out} compensation techniques

The relationship of DE and X_{Cds}/R_L is illustrated under ideal conditions in Figure 3, which shows the DE in an ideal 78.5% when the linearization value (X_{Cds}/R_L) ranges between 1 and 2.5 [8]:

$$1 < \frac{X_{Cds}}{R_L} < 2.5 \quad (5)$$

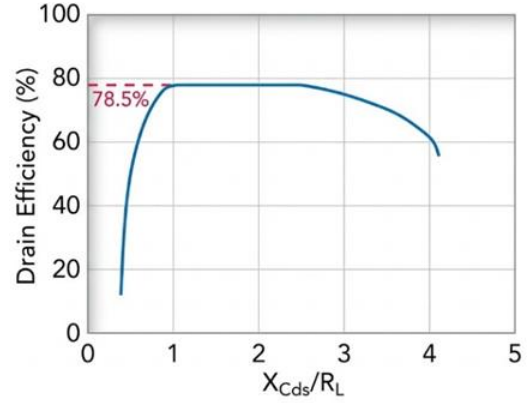


Figure 3. Drain efficiency (DE) vs. ratio of drain-source capacitance to load impedance (X_{Cds}/R_L) [8]

This range gives the design of a broadband, high-efficiency Class-J PA additional margin. As the input signal power levels directly affect the drain signal power levels and changes for low and high input powers in the transistor output capacitance are discussed separately [8]. In small-signal drive conditions, the dynamic AC power at the drain is negligible compared to static DC power dissipation. The intrinsic output capacitance at quiescent V_{ds} of 28 V is about 1.185 pF. Moreover, based on the peak forward drain current (I_{max}) of 1.5 A, the theoretical bandwidth limits for high-efficiency operation are derived from Eqs. (3) and (5) are bounded between 1.44 GHz and 3.61 GHz only. This frequency spectrum, operating in this range, provides the corresponding theoretical maximum DE of 78.5% [8].

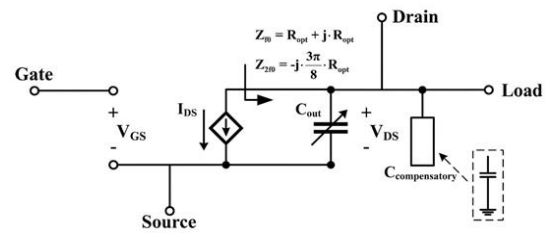
Under large-signal drive conditions, the impact of the significant dynamic RF voltage swing fundamentally interacts with the quiescent DC drain bias. Particularly, at a modest bias of $V_{ds} = 28$ V, the intrinsic output capacitance enters into a highly voltage-dependent, nonlinear regime. It can be seen from the associated capacitive reactance, X_{Cds} , in Figure 4 that it is inversely proportional and substantially increases when either the operating frequency or the instantaneous drain-to-source voltage decreases [8].

In order to maintain the ratio of intrinsic capacitive reactance X_{Cds} to load resistance R_L , that is, X_{Cds}/R_L , within a design space for optimal high-efficiency operation, an external impedance MN must be synthesized to compensate for the highly nonlinear voltage dependence of the device drain capacitance. The dynamic range of this capacitive reactance, X_{Cds} , passes through a wide impedance spread from -5.88Ω to -93.27Ω . Moreover, as represented by area 1 in Figure 5, reactance around minimum intrinsic drain capacitance (1.18 pF) is bounded within -93.27Ω to -37.20Ω , considering the operational bandwidth being from 1.44 GHz to 3.61 GHz.

A 3D surface plot showing the magnitude of the transmission coefficient $|S_{21}|$ (in dB) as a function of Drain-Source Voltage (V) and Frequency (GHz). The vertical axis represents $|S_{21}|$ (dB) ranging from -5 to 4. The horizontal axes are Drain-Source Voltage (V) ranging from 0 to 30 and Frequency (GHz) ranging from 0.4 to 4.0. A sharp resonance peak is visible at approximately 4.0 GHz and 0 V, reaching a value of about 4 dB. The color bar on the right indicates the magnitude scale from 0 to 110 dB.

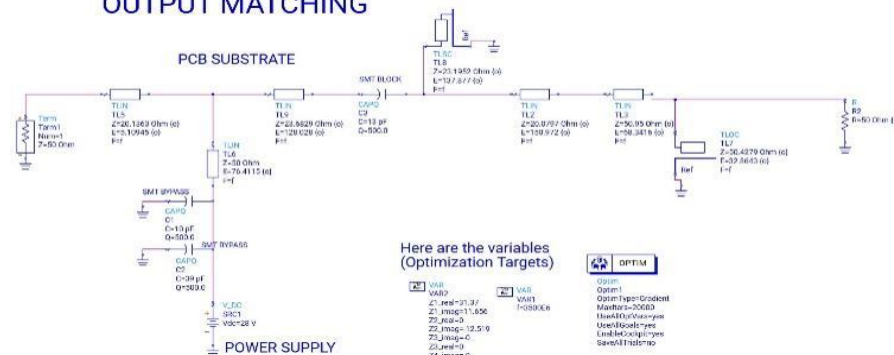
In contrast, region 2 indicates that the reactive impedance characteristic is integrated relative to the maximum intrinsic capacitance $C_{ds} = 9$ pF over the same bandwidth from -14.73Ω to -5.88Ω . In order to systematically map these sub-optimal impedances onto the high-efficiency design space identified in Area 1, where $X_{Cds}/RL = 1$ to 2.5, a specialized output compensation network must be synthesized [8]. As shown in Figure 5, the characteristic of the matching architecture is based on a simple distributed topology with a two-stage cascaded microstrip transmission line and a shunt open-circuited stub. Using a precisely optimized combination of the

In order to modify the output voltage waveform further, correcting the phase difference of the drain current and voltage, and obtaining a corresponding ratio between the second harmonic and fundamental components, Wang et al. [9] applied an extra compensatory capacitor. The simplified circuit model is illustrated in Figure 7.



Microstrip Dimension: Width/Length(mm)

To simplify the design challenge of the nonlinearity in C_{out} and the required fundamental impedance and second harmonic impedance for Class-J PA operating in 3.5 GHz with 200 MHz bandwidth, we will explain the design procedure details in section three and extract the optimum impedances for Class-J using AI-extrapolated load-pull data established in paper [13] and design the output MN with optimized double-stubs MN used in paper [14], as shown in Figure 8.



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The MN mathematically compensates the parasitic capacitance by designing the external MN to offer optimum impedances so that, from the perspective of the intrinsic (current generator) plane, all reactive targets mandatory to utilize the PA working in Class-J operation mode are achieved.

3. CHARACTERIZATION SETUP AND CIRCUIT IMPLEMENTATION OF CLASS-J

For Class-J PA, there are design steps of any PA design that need to be considered for high efficiency operation. The flow diagram shown in Figure 9 depicts the overview of the design procedure at the fundamental level.

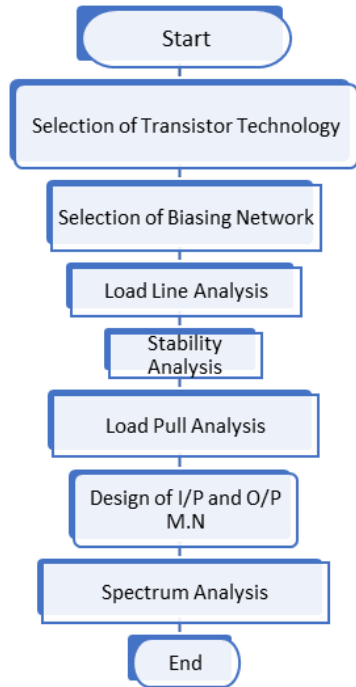


Figure 9. Flowchart of the power amplifier (PA) design procedure

3.1 Transistor technology selection

As a standard practice of RF PA synthesis, the primary electronic design automation (EDA) environment used in the stages of the overall block was based on Keysight's ADS. In this simulation, a GaN HEMT, namely Macom CGH40010F, was chosen as the active device for large-signal simulations. This particular GaN device was chosen based on the empirical parameters in its datasheet, which exhibit the necessary non-linear behavior needed to provide sufficient RF output power for 5G NR band n78 applications.

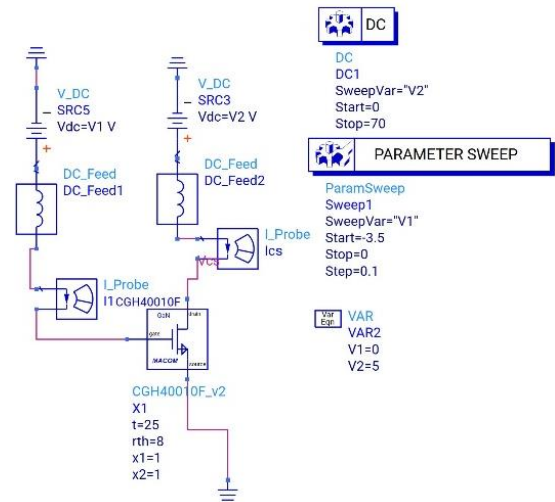
3.2 Selection of biasing network and load line analysis

Based on the proposed PA architecture, we selected a voltage supply of $V_{DD} = 28$ V and a gate bias, $V_{GG} = -3.1$ V (the threshold voltage for a quiescent bias current of less than 2% of I_{max}) using the CGH40010F GaN transistor datasheet. These specifications are applied through a fixed-bias network to operate the device as a Class-B PA, generating the half-wave rectified Drain current (I_d). In addition, the projected DC-IV characteristics of the CGH40010F GaN transistor are depicted along with the applied biasing circuit in Figure 10(a).

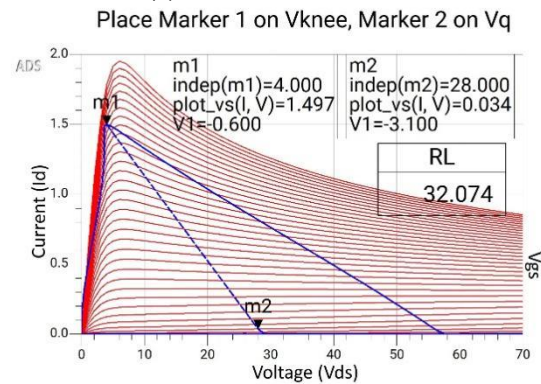
The static quiescent (Q) bias point is extracted by systematically projecting on the dynamic load line using marker m2, confirming the objective Class-B operational mode as demonstrated in Figure 10(b).

Consistent with S.C. Cripps theory for Class-J [1] operation, the Z_{f0} and Z_{2f0} load impedances of transistor X5 were properly terminated for high efficiency over broadband frequencies. These frequency-dependent terminations, as depicted in Figure 11, are mathematically derived based on Eq. (2) over the intended target bandwidth.

R_{opt} , which was given in Eq. (3), is shown to be $R_{opt} = 31.87 \Omega$ according to the simulation result and optimum load impedances $Z_{f0} = 31.87 + j37.187$, $Z_{2f0} = -j38.7$ as illustrated in Figure 12.



(a) Basic circuit of the PA



(b) The GaN DC-IV curves

Figure 10. Basic circuit of the power amplifier (PA) and its Gallium Nitride (GaN) transistor characteristics (DC-IV) curves

Having defined these optimal load impedances, Figure 12 demonstrates the increase in V_{ds} along with its phase shift. Hence, the phase shift and increment in V_{ds} slightly overlap with the drain current (I_d), which contributes to the high efficiency of Class-J PA. Particularly, although this waveform displays a characteristic of switching mode PA, the Class-J mode PA can achieve linearity equivalent to that of Class-B or AB modes due to its non-switching mode operation. The absence of the need for harmonic traps differentiates this architecture from Class-B and renders it appropriate for wideband 5G NR band n78 applications. “Alpha” factor exhibited in Eq. (1) is tunable between -1 and 1. Since the theoretical efficiency is identical between all drain voltage

waveforms produced by different (α) when combined with half-rectified current, this causes the Class-J to widen further

the bandwidth. Substitution of $\alpha = 1$ in Eq. (1) to expansion as shown in Eq. (6).

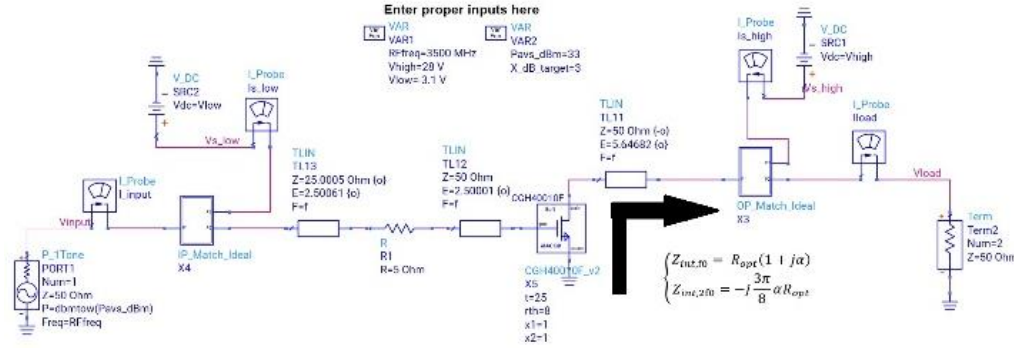


Figure 11. The Class-J power amplifier (PA) schematic

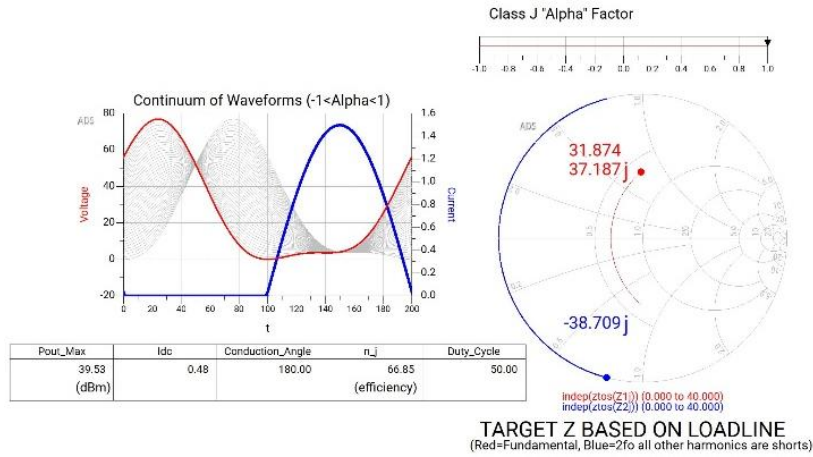


Figure 12. Class-J mode waveform shapes and optimum impedances with $\alpha = 1$

$$V_{DS}(\theta) = V_K + (V_{DD} - V_K)(1 - \sin \theta - \cos \theta + \frac{1}{2} \sin 2\theta) \quad (6)$$

The two terms $\sin \theta$ and $\cos \theta$, the superposition of the components derived in Eq. (6), produce a phase delay on the fundamental drain voltage phasor. In addition, their cross-product term, $\sin 2\theta$, generates a second harmonic voltage contribution that overlies constructively. This in-phase attachment creates a peaking mechanism superimposed on the fundamental sinusoidal shape, which explains the higher harmonic voltage at the drain terminal shown in Figure 12.

3.3 Stability analysis

The bias point chosen by the designer of a PA is among its most important considerations. The stabilization circuit for the low-frequency stability of the PA is on the CGH40010F's datasheet, which is implemented by connecting the gate with a series resistor. Through this series resistance, the transistor is stabilized over a wide range of frequencies. Therefore, in order to guarantee the unconditional stability of PA, it is ascertained that two fundamental requirements need to be achieved: the factor of Rollet stability should be greater than one, i.e., $K > 1$, and stability measure (b) > 0 . Eqs. (7)-(9) respectively [16] can be used to theoretically calculate the factor of Rollet stability and stability measures.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (7)$$

where, delta magnitude $|\Delta|$ is given by:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \quad (8)$$

$$b = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (9)$$

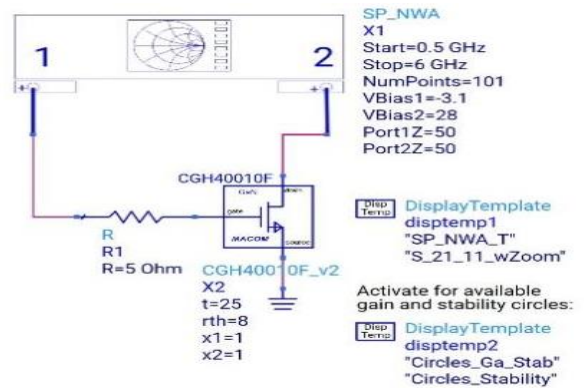


Figure 13. Network analyzer stability analysis of Gallium Nitride (GaN) transistor

In practical simulation environments, the unconditional stability of the PA is evaluated utilizing the Network Analyzer for S-parameters (SP_NWA) instrument component. Furthermore, the stability factor and its frequency-dependent variation are systematically extracted via built-in measurement expression functions and visualized utilizing the

data display templates within the ADS tool, as shown in Figure 13. The minimum K-factor and the minimum μ -source/ μ -load values over the frequency range of 0.1 GHz to 6.0 GHz were 0.322, 0.667, and 0.412, respectively.

3.4 Load-pull analysis and AI-extrapolated load-pull data

To ensure the accuracy of load impedances both at the fundamental and second harmonic frequencies, referenced in Figure 12 based on the load line, it is required to carry out load pull simulations corresponding to the transistor with a stabilization resistor by considering the same reference impedances for load pull analysis with available source power (P_{avs}) in the ADS tool, as illustrated in Figure 14.

To maximize the DE of the PA and synthesize a robust impedance-MN, the proposed Class-J architecture influences AI-driven, multidimensional, nonlinear extrapolated load-pull data [13]. This advanced methodology is employed to systematically extract the optimal source, fundamental, and

second-harmonic load impedances, as depicted in Figure 15.

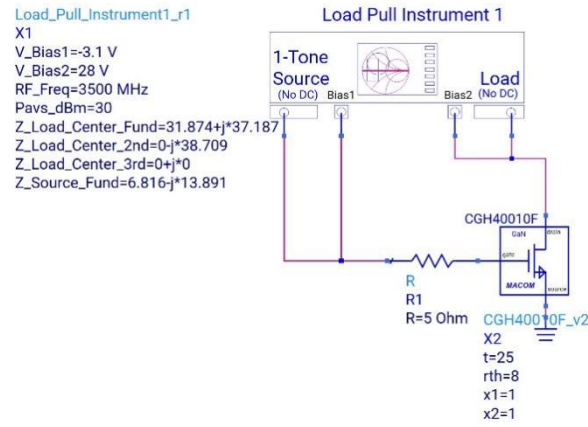


Figure 14. Stabilized transistor load pulling analysis

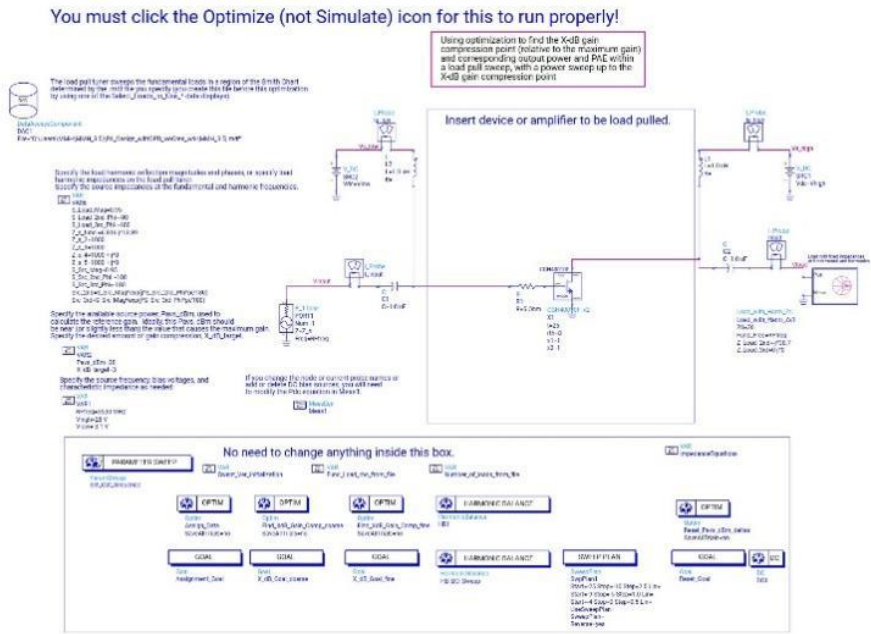


Figure 15. AI-powered multidimensional nonlinear extrapolated load-pull data

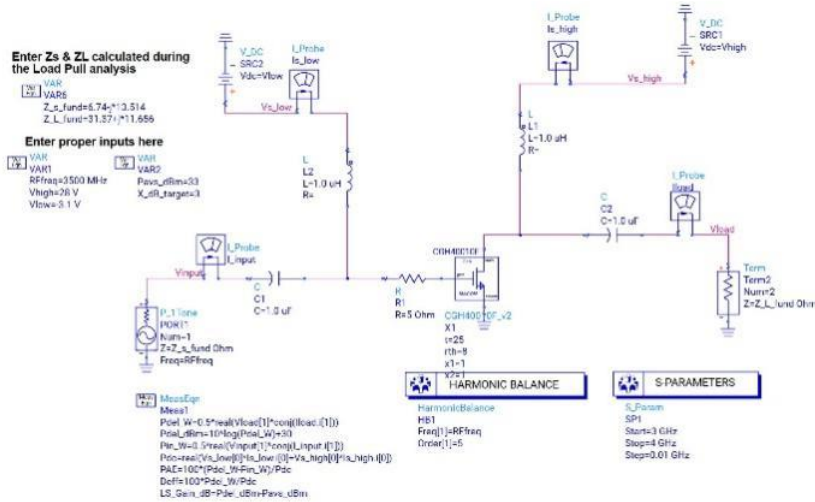


Figure 16. Optimum impedances extracted by AI-load pull simulations validation

The PA was designed for 5G NR n78 band macro base station applications. Energy consumption has to be minimized during the use of Class-J PA, which is associated with the PAE. Hence, the optimum impedances related to the PAE of Class-J PA are considered as opposed to power output to meet the design requirement for the MN of Class-J PA. Hence, it is possible to validate the optimum impedances corresponding to the MAX PAE achieved from AI-LOADPULL simulations by applying them directly on transistor terminals (Z_S and Z_L) rather than applying 50 Ω termination, as illustrated in Figure 16.

3.5 Matching network design

After confirming the optimal source (Z_S) and load (Z_L) impedances from the AI-extrapolated load-pull data, the next major design step is to synthesize the MNs required to transform these complex device terminations to a standard 50 Ω system environment. The MN synthesis was conducted using a previously reported comprehensive, simultaneous multidimensional optimization method [14] available in the commercial ADS EDA package. This high-level methodology replaces the traditional synthesis methods used, like standard Smith chart utilities, automated impedance-matching algorithms, and analytically derived lumped-element networks. More precisely, the output MN is implemented in a distributed double-stub architecture and was optimized via ADS for generating the exact complex load terminations as

suggested in AI-extrapolated load-pull contours (illustrated by Figure 8). On the Smith chart presented in Figure 17, we visually associate the mapping of both the theoretical targeted impedances and the final optimized impedances.

The compensated output parasitic capacitance C_{ds} of the transistor and the shorted stub of MN are regarded as a short circuit at third and higher-order harmonics. After the design of OMN as per rules, it is assumed that the ratio of the capacitive reactance related to the load-line resistive ratio $[X_{C_{ds}}/R_L]$ is taken into account as expressed in Eq. (5), resulting in the design of an MN that is ideally constructed. Nevertheless, regarding the operating frequency of the device and the technology used in the design, this ratio may also exceed unity. For the designed Class-J PA, its major active element is a GaN transistor, thereby satisfying the second harmonic impedance condition where the internal drain-source capacitance (C_{ds}) and shorted stub comprise its double stub type output MN.

For proper performance of the PA, the input MN was designed in the same manner as shown in Figure 18, including a double stub MN. Moreover, an AI-load pull-based approach for designing its MNs focused not only on low harmonic distortion but also on the performance of the PA parameters, such as PAE and DE, in the preferred bandwidth. Also to note, designing the Class-J PA utilized a GaN transistor, which exhibits high-power density, leading to higher output power and efficiency while maintaining linear operation that is crucial for controlling harmonic distortion.

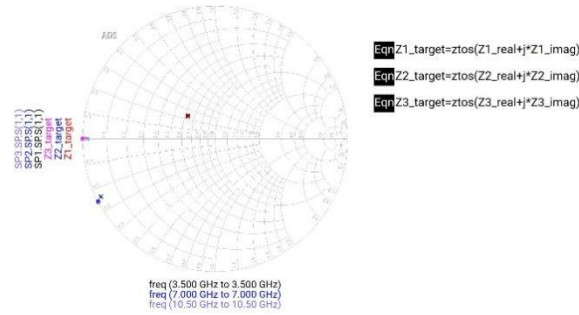


Figure 17. Fundamental and second harmonic targeted and optimized impedances

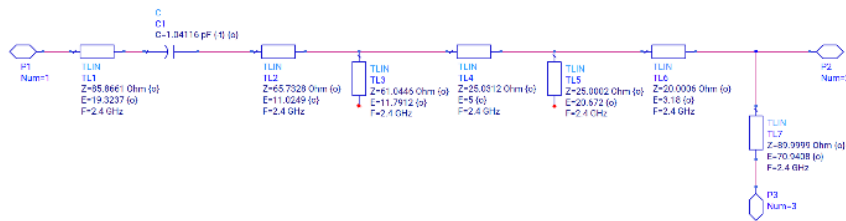


Figure 18. Optimized the input matching network (MN) of the power amplifier (PA)

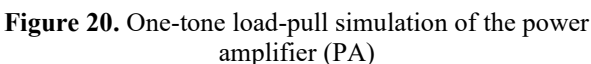
4. RESULTS

The stabilization analysis of the device is performed with the S-parameter network analyzer circuit depicted in Figure 13. High-power CGH40010F packaged GaN HEMTs feature extremely high transconductance (gm) and associated feedback parasitic (C_{gd}), making them highly susceptible to low-frequency parametric oscillations well below the

operational band. To suppress these oscillations, a series gate stabilization resistor of (5.55 Ω) was integrated directly at the gate terminal. This specific value was selected through an iterative optimization loop to balance a strict performance trade-off: providing sufficient resistive damping to isolate low-frequency instability while minimizing the degradation of large-signal RF power gain and efficiency at the 3.5 GHz fundamental frequency. Furthermore, relying solely on the

[illegible]

The next step, after testing the stability of the device, is to perform load-pull simulations for the DUT (device under test) as depicted in Figure 14, resulting in the determination of the optimal impedances for load and source matching on the Class-J PA with respect to where we started based on the load line analysis, targeted source and load impedances discussed in Section 3.2. The load pull analysis yields an optimal source/input impedance of $6.945 + j13.728$, and the load/output impedance obtained is $30.878 + j3.910$, which can be seen in Figure 20 (where the power delivered $P_{del_dBm_MAX}$ is 40.288). Likewise, the best source/input impedance obtained was $6.816 + j13.890$, and get load/output impedance was $26.769 + j8.874$, which corresponds to the maximum efficiency of 56.9% PAE, in Figure 20.



These are the maximum PAE and Power data

Pdel_dBm_at_max_PAE	Pdel_dBm_at_XdB_max	Pdel_dBm_at_m1
40.751	41.808	41.527
PAE_at_XdB_max	PAE_at_max_Power	PAE_at_m1
54.677	49.812	53.686
Zload_Fund_at_max_PAE	Zload_Fund_at_max_Power	Zload_Fund_at_m1
31.370 + j11.656	37.019 - j4.196	35.530 + j4.016
Zin_Fund_at_max_PAE	Zin_Fund_at_max_Power	Zin_Fund_at_m1
6.740 + j13.514	6.975 + j13.060	6.823 + j13.289
Gain_at_max_PAE	Gain_at_max_Power	Gain_at_m1
7.697	7.108	7.449
Pavs_dBm_at_max_PAE	Pavs_dBm_at_max_Power	Pavs_dBm_at_m1
33.064	34.700	34.078
Sload_2nd_at_max_PAE	Sload_2nd_at_max_Power	Sload_2nd_at_m1
1.000 / -104.520	1.000 / -104.520	1.000 / -104.520
Sload_3rd_at_max_PAE	Sload_3rd_at_max_Power	Sload_3rd_at_m1
1.000 / 180.000	1.000 / 180.000	1.000 / 180.000
Src_2nd_at_max_PAE	Src_2nd_at_max_Power	Src_2nd_at_m1
0.950 / 180.000	0.950 / -180.000	0.950 / -180.000
Src_3rd_at_max_PAE	Src_3rd_at_max_Power	Src_3rd_at_m1
0.950 / -180.000	0.950 / -180.000	0.950 / -180.000

PAE Max & Contour Levels

Pdel_dBm Max & Contour Levels

20_ref=20

Simulated 2nd and 3rd Harmonic Loads

The presentation of target source and load impedances

derived using the standard mathematical load-line equations is compared with the previous AI-driven load-pull contour results shown in Figure 21, corresponding to maximum PAE; this comparative assessment is performed. Thus, the optimal input and output impedances needed in designing the Class-J PA are thoroughly clarified and presented in Table 2.

Table 2. AI-load pull vs. load-line based theoretical values of Z_S and Z_L impedances

Z	PAE (%)	P_{out} (dBm)	AI-Load Pull	Load Line
Z_S	66.85	39.53	$6.74 + j13.514$	$5 + j0$
Z_L	54.677	40.751	$31.370 + j11.656$	$31.87 + j37.187$

Note: PAE = Power-added efficiency.

As observed in Table 2, there is a significant reactive shift between the theoretically calculated load-line impedance and the optimal impedance extracted via AI load-pull for maximum PAE. This difference is not an algorithmic error, but rather the direct consequence of reference plane translation and large-signal device physics. The theoretical Class-J equation (Eq. (2)) derives the essential fundamental $(31.87 + j37.187 \Omega)$ and second-harmonic terminations strictly at the intrinsic current generator plane. However, the AI load-pull characterization evaluates the device at the extrinsic package plane $(31.37 + j11.656 \Omega)$ (e.g., extrinsic package plane vs. intrinsic current generator plane).

4.1 Validation of reference plane impedances

Initially, the optimum impedances for the source and load, as illustrated in Figure 16, will be validated while terminating the PA to a 50Ω termination, along with their corresponding performance parameter illustrated in Figure 22. Consequently, fundamental performance parameters such as delivered output power (P_{del}), large-signal and small-signal gains, DE, and PAE exhibit severe degradation because the CGH40010F GaN HEMT transistor is not terminated with its optimum load impedances, as depicted in Figure 22.

The performance parameters shown in Figure 23 are obtained by the evaluation of harmonic balance S-parameter simulators. In these evaluated cases, the transistor is accurately terminated with optimal impedance values extracted using AI-load pull simulations that produce the highest PAE, as shown in Figure 16.

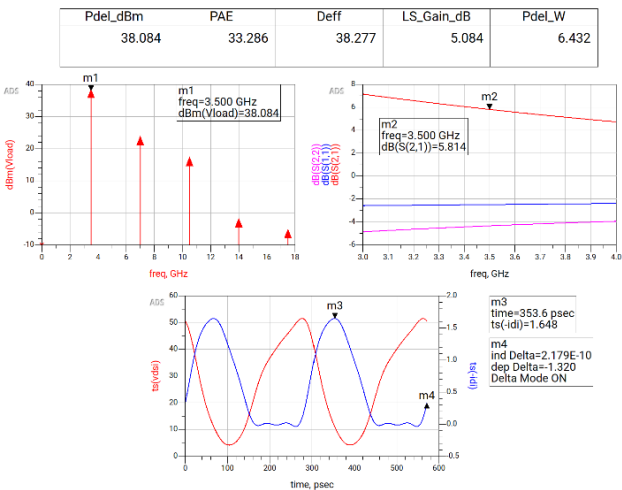


Figure 22. Source and load terminations of (50Ω) performance parameters

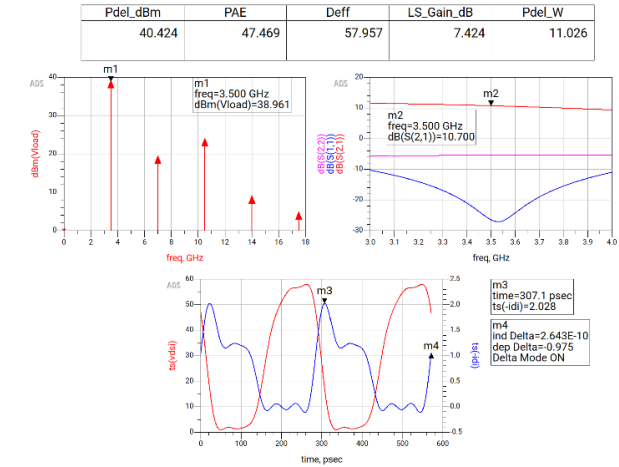


Figure 23. Optimum source and load termination performance parameters

As seen from the results shown in Figure 23, basic performance parameters, such as power delivered, large-signal and small signal gains, DE, and PAE, have increased significantly and come close to the theoretical values obtained from load-pull simulations. This improvement is a result of terminating the CGH40010F GaN transistor with its ideal input/output impedance values as the load. However, it is noteworthy that the observed reflection coefficients, specifically $S(1,1)$ and $S(2,2)$, deviate from their theoretically predicted responses.

Subsequently, the MNs are synthesized using a procedure detailed in Section 3.5, following the extraction of optimum impedances derived from AI-load pull analysis. These synthesized networks are systematically configured at the respective input and output terminals of the PA, designated as the input/output MN components in Figure 11. Eventually, an advanced optimization tool within the ADS environment is employed to rigorously optimize and update the constituent elements of these MNs, as delineated in Figure 24.

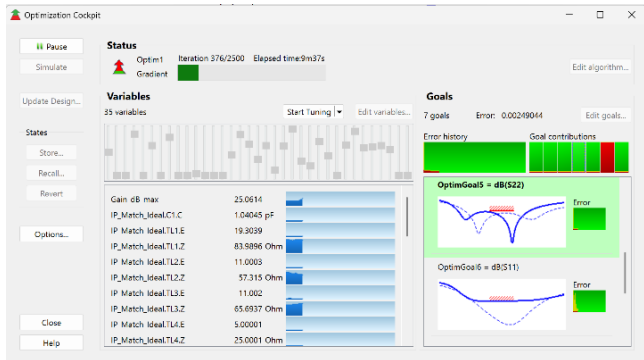


Figure 24. Input/output ideal microstrip matching network (MN) elements optimization

Key performance metrics delivered power, large-signal, and small signal $S(2,1)$ gain have been separately optimized as shown by the outlined PAE and DE in Figure 25. Moreover, as a result of the rigorous optimization of the input and output MNs, the $S(1,1)$ and $S(2,2)$ reflection coefficients are close to the expected results.

The MNs are implemented in Section 3.5 using realizable microstrips input and output double stub MNs. Figure 11 illustrates that these MNs are located at PA's input and output

terminals, and finally, these optimized MN elements can be updated by using simultaneous multidimensional optimization on ADS, as depicted in Figure 26.

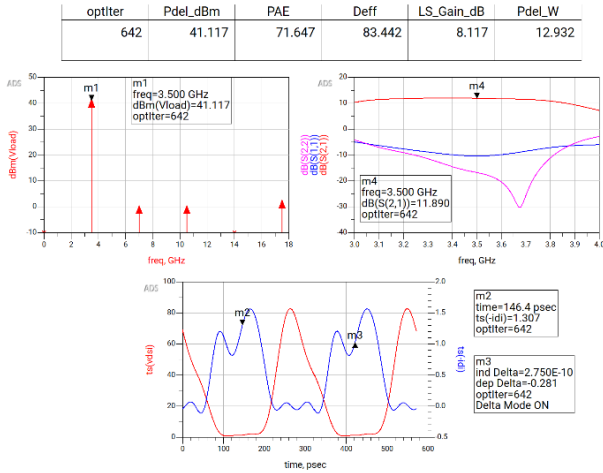


Figure 25. Optimum source and load terminations with ideal microstrip matching network (MN) performance parameters

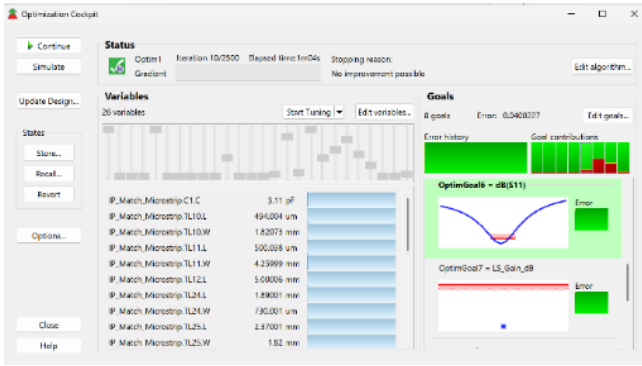


Figure 26. Input/output realizable microstrip matching network (MN) elements optimization

Performance parameters optimized as shown in Figure 27. Input and output optimization of realizable microstrips MNs enhanced for the proposed Class-J RF PA.

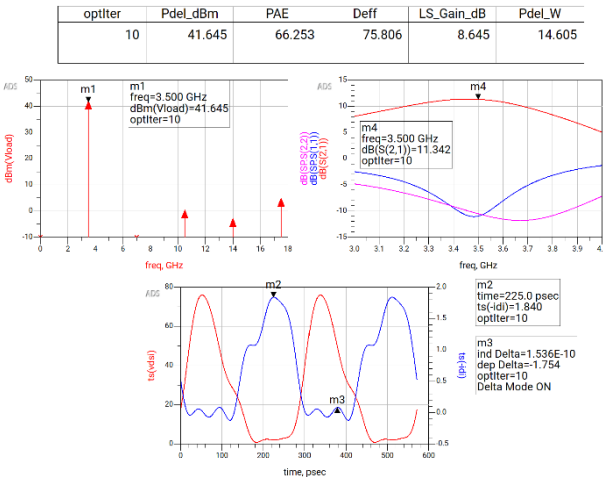


Figure 27. Optimum source and load terminations with realizable microstrip matching network (MN) performance parameters

The quantitative details for the commonly available performance parameters before and after realization of microstrip matching topologies, including power delivered in (Watts and dBm), DE, PAE, small and large signal gain, are summarized in Figures 22, 23, 25 and 27. These respective metrics are mathematically applied using the “MeasEqn” feature built into the simulator of the harmonic balance HB. The load voltage is analyzed (in power spectrum in dBm) through the frequency domain, whereas the intrinsic drain voltage and currents are drawn as a time domain function driven by the HB simulation controller that interacts with ADS.

Figure 27 shows the extracted time-domain waveforms, clearly showing that half-rectification is indeed achieved for both the intrinsic drain voltage and current; such a small overlap faithfully validates the concept of desired Class-J operation mode. Simultaneously, input and output reflection coefficients $S(1,1)$ and $S(2,2)$ remain well below -10 dB over the expected operational frequency range of 3.4–3.6 GHz. Finally, the Class-J PA performance metrics are summarized in Table 3 for both with and without synthesized MNs applied at source and load terminations.

Table 3. Performance comparison of Class-J RF PAs for different MN types

Type of Termination	Optimum			
	50 Ω Without MN	Z_s and Z_L Without MN	50 Ω with Ideal Micro Strips MN	50 Ω with Realizable Micro Strips MN
LS_Gain [dB]	5.084	7.424	8.117	8.645
SS_Gain [dB]	5.814	10.7	11.89	11.34
P_{out} [dBm]	38.084	40.424	41.117	41.645
max PAE [%]	33.286	47.469	71.647	66.253
max DE [%]	38.277	57.957	83.442	75.806

Note: RF = radio frequency, PA = power amplifier, PAE = power-added efficiency, MN = matching network.

4.2 Large-signal power amplifier performance results (Continuous-wave sweeps)

To characterize the dynamic variation of fundamental performance parameters of the proposed Class-J PA under large-signal drive conditions, HB simulations were performed based on P_{avs} in dBm as the independent sweep variable. The dynamic response of key metrics, including power delivered in (dBm), DE, PAE, and large signal gain are simulated against the P_{avs} sweeping, as shown in Figure 28. These measured results show that at an equivalent available source power of 33 dBm with a 28 V supply into a matched output impedance (50 Ω), the amplifier topology produces a maximum output power, gain, DE and PAE of 41.643 dBm, 8.6dB, 75.8% and 66.2%, respectively.

4.3 Broadband frequency response

Similarly, HB simulations were performed to determine the trend of major performance metrics for the proposed Class-J PA, including a two-stub input and output MNs as a function of swept input RF frequency. The results are depicted in Figure 29. The simulated results show a delivered output power greater than 40 dBm with a low but still meaningful (8 dB) power gain for a total operational bandwidth of 200 MHz (3.4 to 3.6 GHz). Moreover, a maximum of PAE and DE also reaches the peak values at 66.2% and 75.8%, respectively,

which are measured at a center frequency of 3.5 GHz.

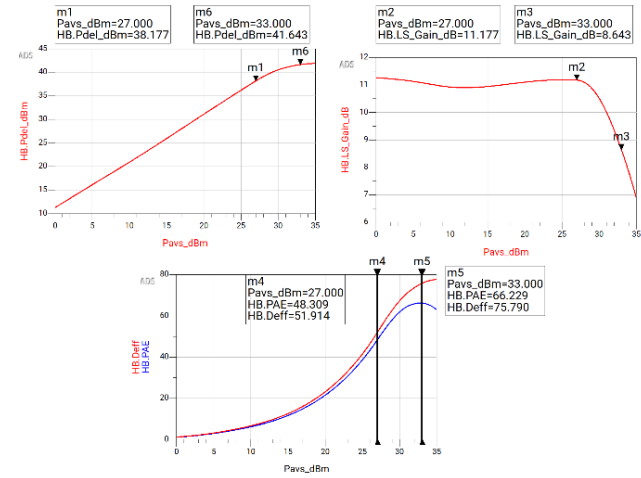


Figure 28. Class-J power amplifier (PA) swept corresponding to P_{avs} (dBm)

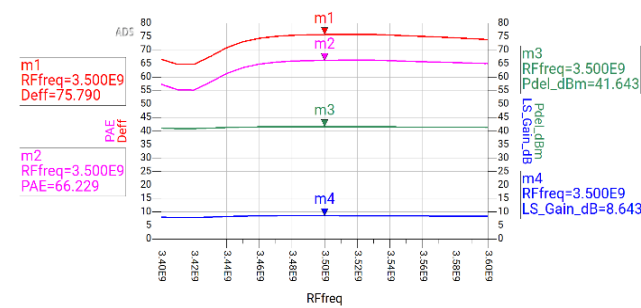


Figure 29. Class-J power amplifier (PA) swept corresponding to frequency

4.4 Output power back-off results

Figure 30 shows the corresponding output power increase of PAE and DE. For modern 5G NR macro base station transmitters processing wideband OFDM signals with high PAPR, the amplifier must maintain high operational efficiency within the power back-off zone. Based on the large-signal power sweep metrics at the 3.5 GHz center frequency, the architecture achieves a peak saturated power of 41.64 dBm. At a 6-dB output power back-off (OPBO) of 35.64 dBm, the Class-J network maintains a robust PAE of 36.5% and a DE of 39.2%. At an 8-dB OPBO (33.64 dBm), the PAE is maintained at 28.9%.

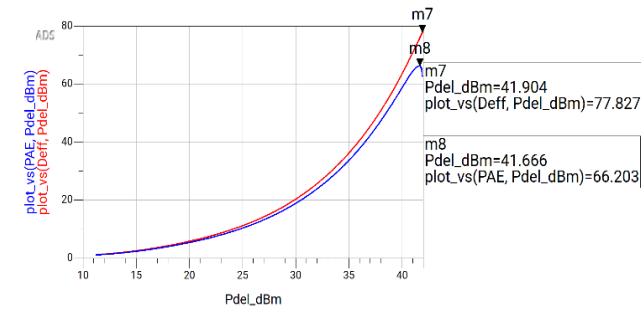


Figure 30. Class-J efficiency (DE, PAE) swept corresponding to output power (dBm)

Note: DE = drain efficiency, PAE = power-added efficiency.

4.5 Linearity evaluation

Linearity test at 3.5 GHz Class-J PA in 5G NR n78 band application condition, a two-tone OIP3 simulation was conducted. To thoroughly evaluate the intermodulation distortion (IMD) adjacent to the amplifier’s operating ceiling, the test employed a tightly spaced tone configuration at 1 MHz for $P_{avs} = 20$ dBm in accordance with the available source power. At this significant drive level, the linearity of the amplifier showed excellent and very symmetrical characteristics. The OIP3 extracted was 50.747 dBm for the lower intermodulation product and 50.705 dBm for the upper, as shown in Figure 31.

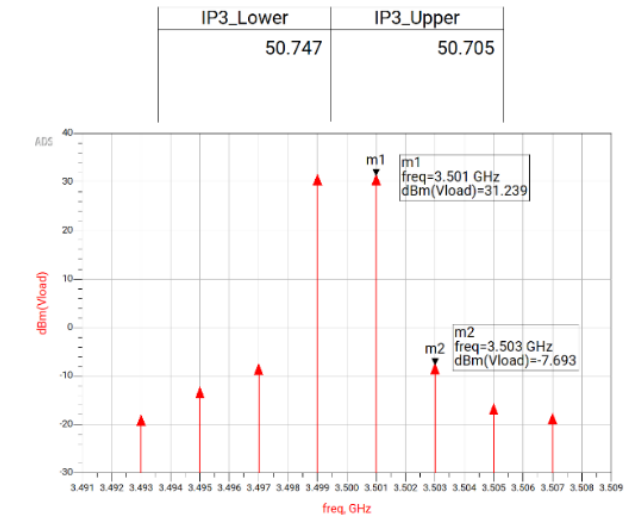


Figure 31. Output Third-Order Intercept Point (OIP3)

This tight symmetry between the upper and lower sidebands indicates a highly balanced reactive impedance response across the fundamental bandwidth, effectively minimizing asymmetrical spectral regrowth. Given the amplifier’s saturated output power (P_{sat}) of approximately 41.645 dBm, this OIP3 performance establishes a robust linearity margin of approximately 9 dB ($OIP3 - P_{sat}$). This substantial margin confirms that the AI-driven multidimensional optimization utilized in this methodology not only secured the precise reactive terminations required for the 75.8% peak DE but also successfully managed the device’s large-signal nonlinearities. By effectively balancing the interactions between the nonlinear transconductance and the voltage-dependent parasitic capacitance at high power levels, the proposed design provides a highly stable linear baseline capable of handling the high PAPR characteristic of modern OFDM modulation schemes.

While standard two-tone OIP3 validations confirm narrowband linearity, fully assessing compliance with 5G NR standards (ACLR and EVM) requires evaluating the PA with a 100 MHz OFDM waveform (e.g., 3GPP TM1.1, PAPR ~7.5 dB). Such an assessment, whether simulated via system-level platforms or physically measured, necessitates the integration of a digital pre-distortion (DPD) memory-polynomial algorithm to compensate for AM-AM and AM-PM compression near saturation. A comprehensive physical assessment of ACLR and EVM using a DPD measurement testbench is reserved as the primary focus for the hardware validation phase in future work.

The proposed and comprehensively optimized Class-J PA

architecture demonstrates substantial advantages concerning high-efficiency operation. Furthermore, the GaN transistors utilized in this design inherently exhibit exceptionally low intrinsic noise characteristics when evaluated against alternative semiconductor technologies such as GaAs. The diminished on-state resistance and high electron mobility intrinsic to GaN devices fundamentally contribute to an enhanced overall noise performance. Additionally, the precise synthesis of the impedance MNs ensures that noise degradation exerts a minimal impact on signal integrity, a characteristic further verified by the evaluated linearity of the Class-J PA.

To rigorously quantify the broadband performance and replace the qualitative description of ‘maintained’ efficiency, a strict metrological operational envelope is defined across the entire 200 MHz passband (3.4 GHz to 3.6 GHz). Specifically, the delivered output power exhibits a maximum in-band ripple of 0.73 dB, establishing a worst-case minimum power floor of 40.92 dBm at the extreme band edges. The efficiency metrics are strictly bounded; the PAE and DE maintain minimum operational floors of 55.21% and 64.73%, respectively, across the entire bandwidth. Furthermore, the large-signal power gain remains highly consistent with a flatness bounded within ± 0.7 dB. From an impedance matching perspective, the worst-case input and output return losses (S_{11} and S_{22}) remain strictly below the -9 dB threshold everywhere within the passband, ensuring robust stability against load mismatch. Finally, the two-tone OIP3 linearity metric is sustained above a minimum band-edge floor of 48.5 dBm, validating the

architecture’s compliance for wideband base station applications.

4.6 State-of-the-art and I/O matching network layout of Class-J

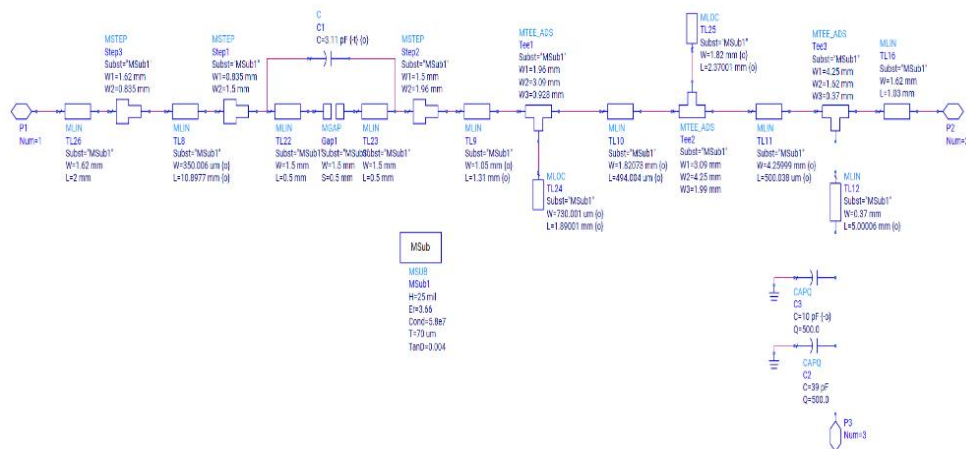
Finally, the enhanced performance parameters of the proposed Class-J PA incorporating the double-stub input and output MNs are systematically compared with analogous Class-J PAs reported in the literature [6-11] and recent works on Class-J PAs [15-20].

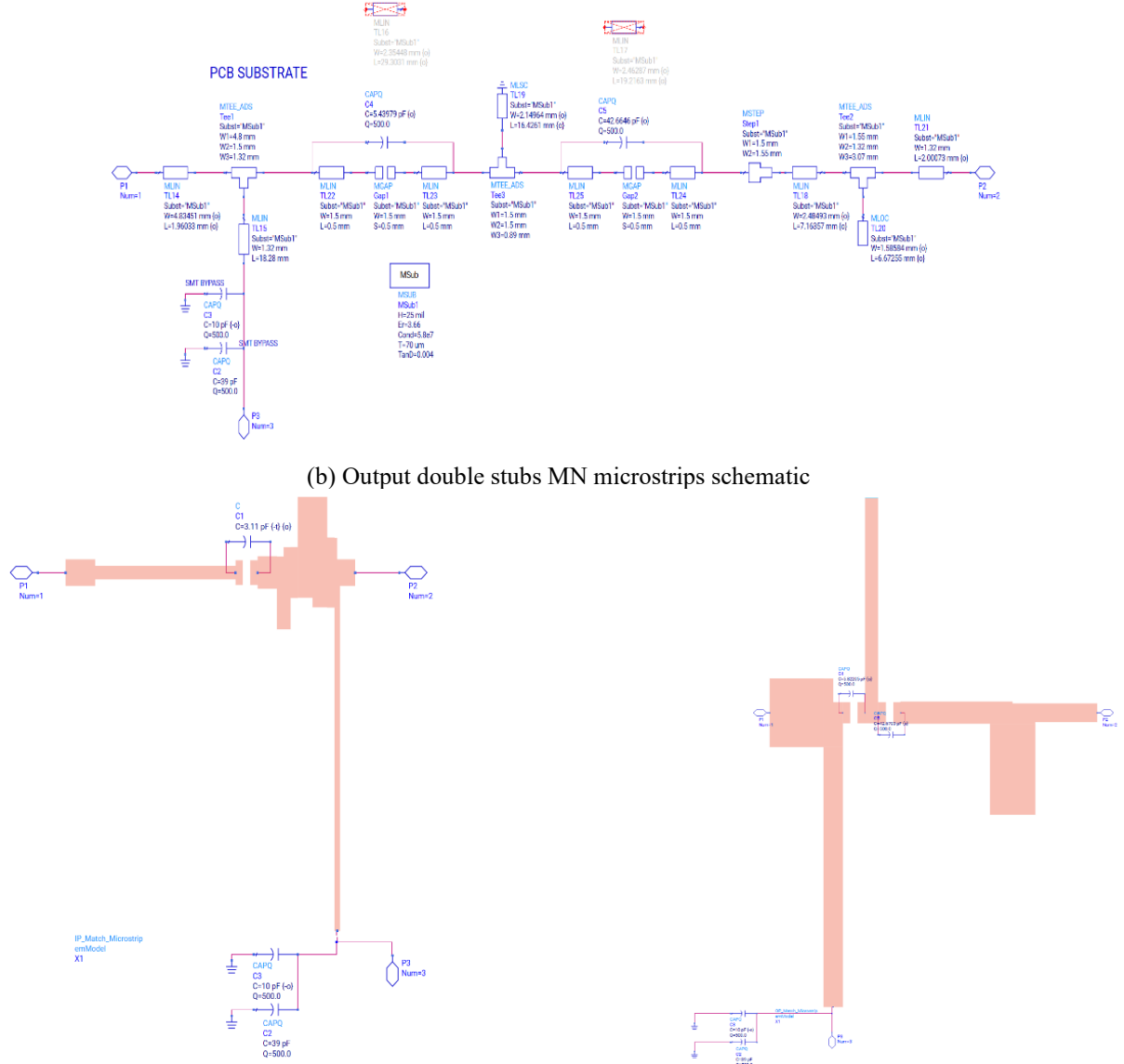
The comparative performance of the listed methods is summarized in Table 4. The increase of DE and PAE of the proposed architecture is superior, though having a relatively limited BW compared to the reference works shown in Table 4. The reduction in fractional bandwidth is caused by the physical impedance synthesis of the proposed Class-J PA’s high-efficiency MNs; instead of using lumped components, distributed transmission line elements were used to achieve a finite, 200 MHz band centered at 3.5 GHz. While this achieved BW is relatively narrow with respect to the current state of the art Class-J PA topologies listed in Table 4, it is, however, more than adequate to enable a practical implementation of this PA into next-generation 5G NR n78 macro base station infrastructure. In addition, a range of operational BW could be extended through a critical design trade-off to also fan out into the efficiency envelope traded off against the maximum achievable efficiency of the PA.

Table 4. Comparison of the results of Class-J PA with other studies using various techniques of 5G NR applications

Reference	V_{ds} [V]	GaN Technology	Center Frequency [GHz]	Bandwidth [GHz](FBW%)	P_{out} [dBm]	PAE-DE [%]	Gain [dB]
[6]#	30	CGH40010F	2.14	2.12–2.16 (1.87%)	40.6	77.3 P	16
[7]#	30	CGH27015F	1.9	1.3–2.4 (57.8%)	40.1	61 P	15
[8]*	28	CGH40010F	2.5	1.4–3.6 (88%)	40.5	67 D	9
[9]*	31.6	CGH40010F	2.5	2.35–2.65 (12%)	39	69 D	10
[10]*	28	CGH40010F	3.75	2.85–4.48 (43.46%)	39.5	38 P	20
[11]*	28	CGH40010F	3.5	3.3–4.2 (25.71%)	39	50 P	-
[12]*	28	CG2H40010F	2.8	2.2–3.4 (42.8%)	40	70 D	10.5
[15]*	28	CGH40010F	2.3	0.7–3.7 (130.4%)	41	70 D	10
[16]*	28	CGH40010F	2	1.6–2.4 (40%)	39	51 P	12
[17]*	28	CGH40010F	3.5	3.3–3.7 (11.42%)	41.4	67 P–82 D	7.4
[18]*	28	CGH40010F	2.5	2–3 (40%)	40	61 D	10
[19]#	28	CGH40010F	1.9	1.4–2.4 (52.63%)	40.5	64 P–67 D	11
[20]#	28	CGH40010F	2.5	2–3 (40%)	40	59 P	11.5
Ours*	28	CGH40010F	3.5	3.4–3.6 (5.71%)	41.64	66.2 P–75.8 D	8.6

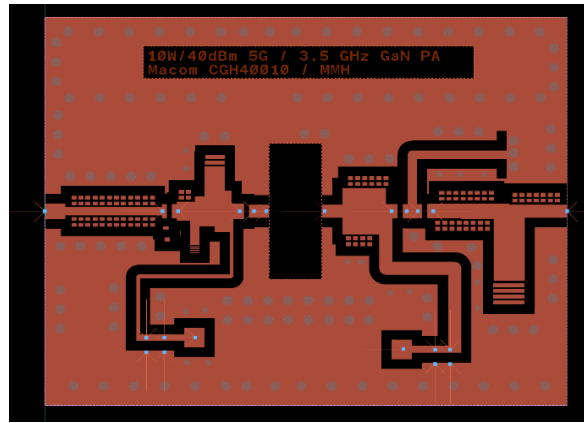
Note: #: Measured results, *: Based on observation of simulation results; P represents the power added efficiency (PAE), D represents drain efficiency (DE); PA = power amplifier, NR = New Radio, GaN = Gallium Nitride.





(c) EM-co-simulation (EM-cosim) schematic of the input MN with double-stub microstrip lines

(d) EM-cosim schematic of the output MN with double-stub microstrip lines



(e) The overall microstrips layout

Figure 32. Input and output matching network (MN) schematic and overall microstrips layout of the power amplifier (PA)

Overall, this architecture achieves extremely efficient performance while maintaining important linearity properties over large spans of BW targeted and thus shows markedly superior performance for fundamental reasons over previously high-performing structures such as Class-J PAs described in Table 4. Figure 32(a) and (b) show the schematic microstrips

element for the input and output double-stubs MN, while Figure 32(c) and (d) show the layout electromagnetic EM-cosim for the input and output MN. Figure 32(e) shows the general organization for the Class-J PA substrate. The substrate for the microstrip line used was Rogers RO4350, with a permittivity of the dielectric constant is 3.66 and a 25

mil (0.635 mm) thickness. Input and Output Matching were designed based on the double stubs matching. To improve overall circuit stability, a resistor (5.55 Ω) was added in series at the input. DC isolation capacitors were installed at the RF input and output ports, while a decoupling capacitor was located on the DC input to facilitate stable circuit operation. Finally, as shown in Figure 32(a) and (b), one microstrip element in the input double stubs MN microstrips was replaced with capacitor (C1) lumped element and two microstrip elements in output double stubs MN microstrips replaced with two capacitor (C4, C5) lumped elements due to they exceeded about 20 mm length in optimization which is unrealizable for efficient PA substrate layout size.

During the physical layout synthesis on the Rogers RO4350B substrate, initial optimization generated multiple open-circuited microstrip tuning stubs exceeding a physical length of 20 mm. At 3.5 GHz, stubs of this length act as unwanted distributed resonators, degrading out-of-band harmonic performance and unnecessarily increasing the PCB footprint. To address this, these specific lines were compressed by substituting them with equivalent lumped capacitors. The reactive equivalence was defined strictly at the single center frequency $f_0 = 3.5$ GHz, utilizing the standard input impedance relationship for a lossless open stub, $X_C = -j/2\pi f_0 C_{eq} = -jZ_0 \cot(\beta l)$, where Z_0 represents the line characteristic impedance, l is the physical length, and β is the propagation constant. To ensure the claimed 200 MHz broadband performance is physically realizable, all idealized capacitor models were discarded during the final optimization phase. They were replaced with non-ideal, high-frequency S-parameter models from the Murata GJM1555 High-Q series (0402 package size), which are specifically designed for VHF/UHF RF matching. The exact part numbers and their associated high-frequency parasitics at 3.5 GHz, specifically the Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), are detailed in Table 5.

Table 5. High-Q Murata lumped capacitor specifications for microstrip substitution

C	C1	C4	C5
Murata Part	GJM1555C1H3R	GJM1555C1H5R6	GJM1555C1H43
Number	0WB01	WB01	0JB01
Nominal Capacitance	3.0 pF	5.6 pF	43.0 pF
Min. Q Factor (at 3.5 GHz)	>500	>450	>400
ESR (Ω)	0.08	0.09	0.12
ESL (nH)	0.38	0.41	0.45

Note: ESR = Equivalent Series Resistance (ESR), ESL = Equivalent Series Inductance.

To evaluate the precise impact of this substitution, a comparative analysis was executed, tracking the performance before and after replacing the ideal microstrips with the non-ideal Murata component structures. Prior to substitution (ideal distributed network), the circuit yielded a theoretical peak PAE of 71.6% and a fundamental delivered power of 41.1 dBm, as shown in Figure 25. Incorporating the non-ideal component parameters, specifically the ESR ohmic dissipation and the self-resonance shifts caused by the ESL parasitics, introduced an insertion loss of approximately 0.3 dB across the output matching structure. Consequently, the post-substitution peak PAE stabilized at the realistically reported 66.25%, with a final delivered power of 41.64 dBm. Because the final layout

parameters were fully re-optimized using these exact non-ideal vendor models, the network successfully absorbed the component variations, securing the continuous high-efficiency profile across the entire 3.4 GHz to 3.6 GHz operational band.

While the proposed continuous-mode Class-J architecture demonstrates highly robust nominal performance within the co-simulation environment, it is important to acknowledge the inherent sensitivity of distributed microwave MNs to physical manufacturing tolerances. At the 3.5 GHz operational frequency, variations in the Rogers RO4350B substrate permittivity ($\Delta\epsilon_r = \pm 0.05$), mechanical microstrip etching precision ($\Delta L, \Delta W = \pm 0.2$ mm), and lumped surface-mount capacitor tolerances ($\pm 5\%$) will inevitably induce a statistical spread in the finalized performance. Consequently, the metrics reported herein represent the nominal optimized boundaries. Conducting a comprehensive statistical yield evaluation and parametric sensitivity analysis (e.g., via Monte Carlo simulations) to fully quantify the uncertainty envelopes for output power, efficiency, and return loss shifts remains a critical and mandatory phase of future work prior to physical hardware prototyping.

5. CONCLUSIONS

This research presented a systematic and highly efficient design methodology for a broadband continuous Class-J PA, specifically engineered to meet the stringent demands of 5G NR n78 band macro base stations. By utilizing the Macom CGH40010F GaN HEMT at a 3.5 GHz center frequency, a compensation capacitance technique was validated to physically absorb the dominant C_{ds} . The integration of AI-extrapolated load-pull data with simultaneous multidimensional optimization eliminated the reliance on traditional iterative tuning, yielding an optimal double-stub MN. Simulation results demonstrated exceptionally large-signal performance, delivering 41.6 dBm output power, a DE of 75.8%, and a PAE of 66.2%. Moreover, rigorous two-tone testing at a 20 dBm available source power with a 1 MHz spacing validated the amplifier's robustness against complex modulations. The emergence of an intermodulation cancellation null and a highly symmetrical OIP3 of 50.7 dBm confirms that the proposed optimization strategy effectively harmonizes the nonlinear transconductance and parasitic capacitance under deep saturation. Furthermore, the amplifier sustained robust, high-efficiency Class-J waveform shaping across the entire 200 MHz target bandwidth (3.4 GHz to 3.6 GHz). This methodology provides a reproducible framework for overcoming the efficiency-linearity trade-off in next-generation RF front-ends. While the physical microstrip layout was successfully generated and optimized with non-ideal component parasitics, a full electromagnetic (EM) co-simulation and physical fabrication remain as the immediate future work required to fully validate the architecture against complex board-level radiation and via parasitics. Future research will focus on the physical fabrication of the optimized network on the Rogers RO4350B substrate for empirical validation, as well as evaluating the amplifier's linearity under excitation by complex, high-PAPR modulated 5G signals.

ACKNOWLEDGMENT

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NOMENCLATURE

C_{ds} drain-source parasitic capacitance

f_0	fundamental frequency
R_{opt}	optimum fundamental load resistance
Z_{f0}	intrinsic fundamental impedance
Z_{2f0}	intrinsic second-harmonic impedance

Greek symbols

α	waveform shaping parameter
β	driven power level factor
Ω	ohm
θ	radian angle

APPENDIX

AI-driven load-pull characterization specifications

To ensure the reproducibility of the proposed Class-J MN synthesis, this appendix details the dataset generation and boundary parameters utilized by the AI extrapolation tool. The predictive model applied in this design phase is based directly on the generative multidimensional load-pull extrapolation framework validated by Swindell et al. [13], which is integrated into Keysight's ADS environment via a Python-based execution script (AI_LoadPull.py).

A. Training data source and dataset size

The characterization engine is not a substitute for physical physics-based simulation; rather, it acts as a highly advanced interpolation and extrapolation instrument. The baseline training data was generated entirely via large-signal Harmonic Balance (HB) simulations. To populate the training matrix, a Data Access Component (DAC) was utilized as shown in Figure A1 within the ADS schematic to systematically sweep the fundamental load reflection coefficient ($\Gamma_{L,f0}$).

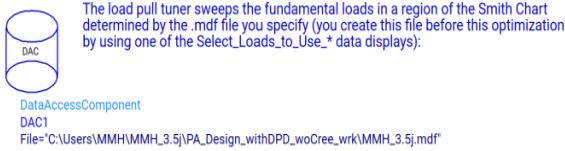


Figure A1. Advanced Design System (ADS) data Access Component (DAC)

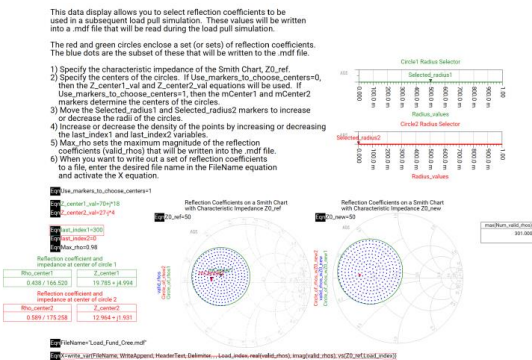


Figure A2. Advanced Design System (ADS) load selection tool

The sparse training dataset consisted of exactly 300 discrete simulation points distributed across the Smith chart generated

using the load selection tool in ADS, as shown in Figure A2. For each of the 300 points, the real and imaginary components of $\Gamma_{L,f0}$ were defined at a system reference impedance of $Z_0 = 50 \Omega$ (e.g., from Index 0: $\Gamma = -0.0017 + j0.0110$ to Index 300: $\Gamma = -0.7014 + j0.4664$).

B. Extrapolation variables and range

The input variables mapped into the multidimensional hyper-space included:

- Independent variables: Fundamental load reflection coefficient magnitude ($|\Gamma_{L,f0}|$) and phase ($\angle \Gamma_{L,f0}$), alongside the available source power (P_{avs}) swept up to 35 dBm.
- Dependent (target) variables: Delivered output power (P_{del}), power-added efficiency (PAE), drain efficiency (DE), and large-signal power gain.
- Controlled boundaries: The second harmonic (Γ_{2f0}) and third harmonic (Γ_{3f0}) terminations were monitored to ensure they adhered to the passive, purely reactive conditions required for Class-J operation.

C. Error mitigation and optimization objective

To avoid generating non-physical (nonsense) data outside the valid simulation range, the AI framework enforces strict energy conservation boundaries. Any extrapolated PAE or power values exceeding the theoretical DC-to-RF conversion limits of the 300-point training envelope are automatically penalized.

The optimization objective was strictly weighted to search the continuous extrapolated space for the global maximum PAE while maintaining a delivered output power boundary of $P_{\text{del}} \geq 40.0$ dBm. To validate the accuracy of the AI extrapolation, the algorithm's predicted optimal termination for peak PAE ($Z_L = 31.370 + j11.656 \Omega$) at $P_{\text{avs}} = 33$ dBm was manually re-inserted into the standard ADS Harmonic Balance simulator. The direct simulation yielded a PAE of 54.6% and output power of 40.75 dBm, which correlated almost perfectly with the AI-predicted contour map, confirming the tool's prediction error is negligible and highly suitable for Class-J synthesis.

D. Engineering validation and matching network impact

While the AI tool's algorithmic validation was reported previously [13], a direct physical verification was performed for this Class-J topology. The AI's predicted optimum for peak PAE ($Z_L = 31.37 + j11.656 \Omega$) was manually re-inserted into an independent ADS Harmonic Balance testbench. The simulation yielded a PAE of 54.60% and output power of 40.75 dBm, showing near-perfect correlation with the AI-predicted contours and confirming negligible prediction error. Furthermore, from a circuit synthesis perspective, a minor prediction error in the exact reflection coefficient vector ($|\Delta \Gamma|$) has minimal impact on the final MN design. Because the continuous-mode Class-J architecture fundamentally relies on an extended, continuous high-efficiency impedance space rather than a single discrete point, small vector deviations translate to negligible mismatch losses (<0.05 dB). Any residual reactive drift introduced by the AI extrapolation is safely absorbed by the tuning capabilities of the physical double-stub microstrip MN during the final layout optimization phase.