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Development and Experimental Validation of a PLC-Based Marine Power Management System Using Hybrid Communication Architecture

Huu-Khanh Doan, Anh-Tuan Dinh, Khac-Tiep Do, Thi-Hong Bui*, Quang-Vinh Ngo

Faculty of Electrical - Electronics Engineering, Vietnam Maritime University, Hai Phong 180000, Vietnam

Corresponding Author Email: hongbt.ddt@vimaru.edu.vn

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ABSTRACT

Conventionally, implementing Marine Power Management Systems (PMS) with Programmable Logic Controllers (PLCs) relies on specialized, often costly, external auto-synchronizers (e.g., dedicated relays) to handle precise breaker closure, as standard PLC scan cycles may introduce latency jitter. This paper investigates a cost-effective PLC-centric architecture aiming to integrate synchronization logic directly into the controller, thereby reducing dependency on expensive peripheral hardware. The proposed solution employs a Hybrid Communication Architecture that utilizes a custom Signal Conditioning Unit (SCU) to trigger hardware interrupts, effectively mitigating the stochastic latency of Modbus Remote Terminal Unit (RTU). A Unit-Per-Unit (pu) scaling strategy with dynamic PI tuning is applied to validate the control logic on a 4 kW laboratory testbed, emulating the dynamics of larger vessel systems. Experimental results demonstrate a phase error of less than 1.8° and frequency recovery within 4.5 s. These metrics benchmarked against IEEE Std 1547 and International Association of Classification Societies (IACS) UR M3 requirements, indicating that the proposed integrated architecture offers a viable and economical alternative for small-to-medium vessel retrofits.

1. INTRODUCTION

1.1 Background and motivation

In the realm of modern maritime transportation, the shipboard power system functions as an isolated microgrid where operational stability and reliability are of the utmost importance [1-4]. As onboard electrical loads and energy storage configurations become increasingly complex, the Power Management Systems (PMS) assume a central role in coordinating generator scheduling, synchronization, and load sharing [5]. To ensure vessel safety and prevent blackouts, international maritime regulations—such as IEEE Std 45.2 and IEC 60092-504—establish stringent criteria for frequency stability and synchronization accuracy [6, 7]. Furthermore, the International Association of Classification Societies (IACS) has recently updated its Unified Requirements (UR M3, Rev. 7, 2024), underscoring the need for robust automated systems in unattended machinery spaces [8].

Currently, the maritime PMS market is largely supported by established solutions from major manufacturers (e.g., Siemens, ABB, Woodward) [9]. While these systems are renowned for their high reliability, they are often characterized by proprietary architectures, which can present challenges regarding acquisition costs and flexibility for maintenance or upgrades [10]. This context creates a notable barrier for small-to-medium vessels, particularly in retrofit projects where budget constraints and equipment compatibility are significant considerations [5].

1.2 Literature review and research gaps

In response to these economic and technical challenges, academic research has explored the development of open-architecture PMS solutions based on standard industrial Programmable Logic Controllers (PLCs). Various studies have indicated the feasibility of employing PLCs for fundamental generator control and monitoring. For example, recent research has introduced a PLC-based functional test simulator for vessel PMS [11], while other works have contributed to PLC-based monitoring for induction motors [12] and ship alarms [13].

To bridge the gap between high-level management and physical execution, recent practical implementations have highlighted the critical need for deterministic timing in microgrid synchronization. Research shows that standard communication layers introduce severe jitter in power distribution networks [14], necessitating robust hardware-level Zero-Crossing Detection (ZCD) methods [15]. Furthermore, implementing deployable check-sync logic directly at the controller level has proven essential for resilient and adaptive microgrid protection [16]; yet, these approaches often rely on external proprietary modules rather than fully integrated PLC capabilities.

Comprehensive reviews by Xie et al. [5] and Han et al. [10] provide valuable insights into active and reactive power sharing strategies for islanded microgrids.

However, a careful review of the current landscape suggests

that there are opportunities for further improvement in low-cost, PLC-based approaches, particularly regarding:

- **Communication Latency**: Modbus Remote Terminal Unit (RTU) serves as a standard, cost-effective protocol in industrial automation. However, its inherent non-deterministic latency can present challenges for time-sensitive tasks such as generator synchronization. Detailed timing evaluations by Găitan et al. [17] indicate that random delays in Modbus RTU operations may complicate precise phase angle sampling within standard polling cycles. While adopting real-time Ethernet [18] or Modbus-UDP [19] is a potential solution, it may inadvertently increase hardware complexity and cost.
- **Experimental Validation**: Many existing studies primarily validate algorithms through software-in-the-loop simulations [11, 15]. While valuable, these simulations may not fully capture physical phenomena such as signal noise, relay switching delays, and electromagnetic interference (EMI) encountered in actual marine environments.
- **Retrofit Versatility**: Vessels often operate with a diverse mix of engines, ranging from legacy diesel engines with mechanical governors to modern ones with Electronic Control Units (ECUs). There appears to be a need for a universal hardware interface capable of accommodating both control types within a unified framework.

1.3 Main contributions and paper structure

Although PLCs are central to marine automation, their application in direct generator synchronization is often constrained by the non-deterministic nature of communication latencies and scan cycles. To ensure safety and precision, conventional designs typically incorporate dedicated external hardware—such as auto-synchronizers (e.g., GAC SYC6714 [20]) or check-sync relays—to execute the precise breaker closing command. While robust, this multi-device approach increases wiring complexity and implementation costs, particularly for retrofit projects on small-to-medium vessels.

To address these challenges, this paper explores the feasibility of a standalone PLC-based solution that aims to integrate synchronization logic directly into the controller, thereby reducing the dependency on specialized peripheral hardware.

The main contributions of this study are summarized as follows:

- **Interrupt-Driven Phase Measurement & Signal Conditioning Unit Hardware**: While traditional PLC setups rely on non-deterministic Modbus RTU polling or expensive external auto-synchronizers to ensure safe breaker closure, this study introduces a custom Signal Conditioning Unit (SCU) that physically bypasses the network layer. By triggering high-speed PLC hardware interrupts precisely at the AC voltage zero-crossings, this proposed architecture eliminates communication jitter. Consequently, it achieves a highly deterministic phase measurement resolution of 1.8° at 50 Hz and executes closing commands 0.35 s faster than commercial benchmark relays.
- **Universal Dual-Mode Governor Interface**: Existing retrofit solutions typically require distinct, dedicated hardware modules to accommodate either legacy mechanical servo motors or modern electronic ECUs. To overcome this rigidity, we integrated a unified, software-selectable interface layer within the PLC capable of outputting both digital Pulse Duration Modulation (PDM) and 4-20mA analog control signals. This provides hardware-free adaptability across diverse engines, successfully achieving strict IACS UR M3 [8] frequency recovery limits (< 5 s) and highly precise steady-state active power sharing with a negligible error of 0.10 kW.
- **Scalable Hardware-in-the-Loop Validation**: Control algorithms are often validated via pure software simulations, which ignore physical switchgear delays, or tested directly on costly full-scale vessel plants. This paper bridges that gap by implementing a 4 kW laboratory testbed utilizing a Unit-Per-Unit (pu) software scaling strategy (K = 25) combined with dynamic PI tuning. This methodology safely emulates and validates the logic thresholds of a 100 kW industrial-grade system, physically proving IEEE Std 1547 [21] synchronization compliance on accessible bench-scale equipment.

The remainder of this paper is organized as follows: Section 2 details the system architecture and hardware design, focusing on the custom SCU and the Universal Interface. Section 3 describes the implementation of control algorithms, specifically the interrupt-driven period measurement strategy. Section 4 presents the experimental setup and validation results against commercial benchmarks. Finally, Section 5 concludes the paper and discusses limitations and future work.

2. SYSTEM ARCHITECTURE AND HARDWARE DESIGN

2.1 Overall system configuration

The proposed PMS architecture, illustrated in Figure 1, is designed to operate as a centralized control hub for the shipboard microgrid. The core controller is a Delta DVP-20SX2 PLC, selected for its industrial robustness, integrated analog I/O channels, and cost-effectiveness. The system is powered by the ship's main 24VDC battery supply, which is typically unregulated and prone to noise.

The architecture separates control tasks into two distinct layers to ensure reliability:

- The Monitoring Layer (Low-Speed): Utilizing Modbus RTU (RS485) communication to poll electrical parameters (Voltage U, Current I, Frequency f, Active Power P) from multi-function energy meters (Selec MFM383A) installed at each generator breaker. This data is used for non-time-critical tasks such as Load Sharing and Power Monitoring.
- The Synchronization Layer (High-Speed): Utilizing a hardwired connection path for time-critical synchronization. AC voltage signals from the generators (u_{Gen}) and the main busbar (u_{Bus}) are routed to a custom SCU. The SCU processes these high-voltage signals into precise logic pulses (f_{Gen}, f_{Bus}) connected directly to the PLC's high-speed interrupt inputs, bypassing the communication latency entirely.

Additionally, an Interface Layer handles the actuation signals, sending either digital "Open/Close" commands to the Air Circuit Breakers (ACB) or speed control signals to the

engines.

2.2 Design of the custom Signal Conditioning Unit

To achieve high-precision synchronization without expensive dedicated hardware, a custom SCU was designed and fabricated. The functional block diagram of the SCU is presented in Figure 2. The circuit design focuses on three key objectives: galvanic isolation, signal multiplexing, and ZCD.

2.2.1 Isolation and power supply

Safety is the primary constraint in marine electronics. The SCU incorporates an Isolated Power Supply Unit that decouples the measurement circuit from the ship's "dirty" 24VDC ground. The input voltage is first regulated by an LM2576 buck converter and then passed through a VD051212S-1W DC-DC isolator to generate a floating supply. This creates a "clean" power domain for the analog processing stages, preventing ground loops and protecting the PLC from high-voltage surges.

2.2.2 Relay-based analog multiplexing

A novel contribution of this design is the use of a Relay-Based Analog Multiplexing technique to minimize hardware costs. Instead of using four separate ZCD circuits for four generators, the system employs a bank of four relays (K1-K4). Controlled by the PLC's Mux Control Signals, these relays select only the "incoming" generator to be synchronized and route its voltage signal to a single, shared processing channel. This approach ensures uniform measurement characteristics for all generators and significantly simplifies the PCB layout.

2.2.3 Zero-Crossing Detection and opto-isolation

The selected AC signal and the reference Busbar signal are processed by two identical ZCD circuits. As explicitly shown in Figure 2, these circuits utilize LM358 operational amplifiers. In this design, the LM358 is configured to operate in a comparator mode to detect the exact instant the AC voltage crosses the zero-volt threshold.

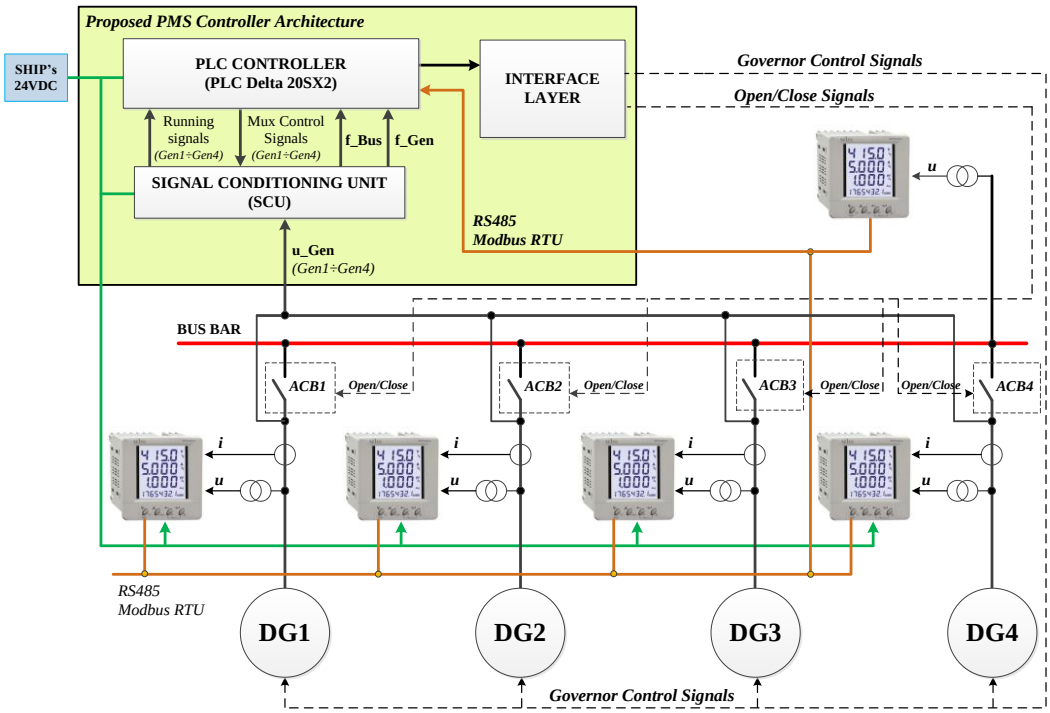

Figure 1. Functional block diagram of the proposed Power Management Systems (PMS) architecture featuring the hybrid communication strategy and the Signal Conditioning Unit (SCU)

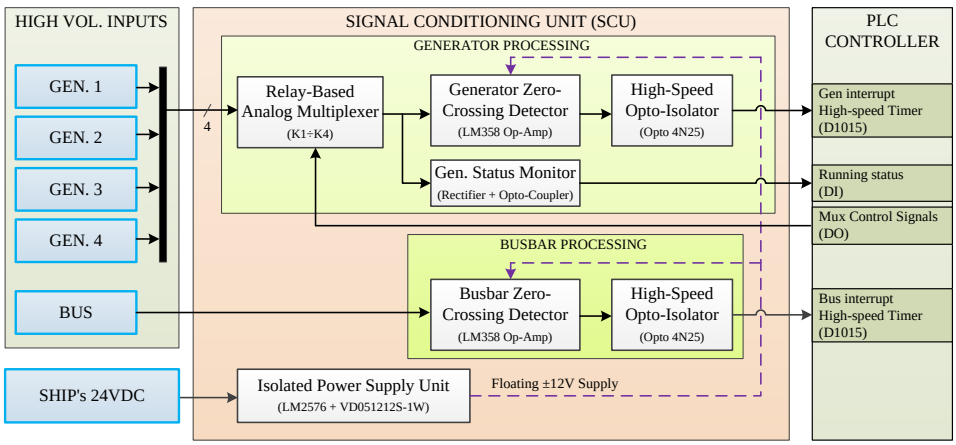

Figure 2. Detailed functional block diagram of the custom Signal Conditioning Unit (SCU)

Although the LM358 is a general-purpose operational amplifier, it was selected for its robustness and wide

availability. Given the high amplitude of the stepped-down AC signals and the steep slope of the 50 Hz mains waveform at the zero-crossing point, the input offset voltage of the LM358 introduces a negligible time delay, which is well within the acceptable tolerance for synchronization. The output of the Op-Amp is a square wave synchronized with the grid frequency. Finally, these signals pass through High-Speed Opto-Isolators (4N25) before entering the PLC's interrupt inputs (X0, X1). The optical isolation barrier ensures that any transient spikes on the AC side are blocked.

2.2.4 Hardware fabrication

To validate the design feasibility, the SCU was fabricated on a standard FR4 double-layer PCB. The physical realization of the module is shown in Figure 3. The layout was carefully designed to maintain sufficient clearance between the high-voltage relay contacts and the sensitive low-voltage logic components, ensuring compliance with marine safety standards. The module is encased in a DIN-rail mountable housing, facilitating easy integration into existing shipboard switchboards.

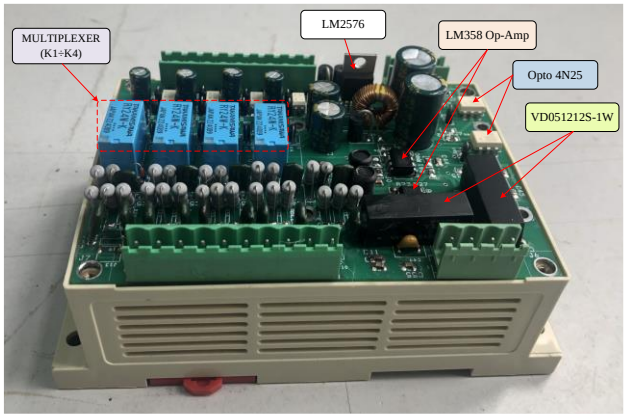

Figure 3. Hardware realization of the proposed Signal Conditioning Unit (SCU)

2.3 Universal dual-mode governor interface

One of the major challenges in retrofitting is the diversity of engine governors. As shown in Figure 4, the proposed system integrates a Universal Dual-Mode Governor Interface capable of accommodating both legacy and modern engines:

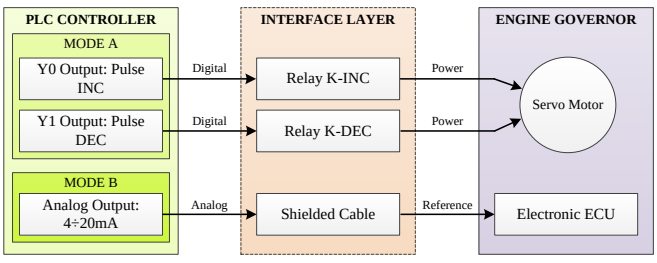

Figure 4. Wiring configuration of the Universal Dual-Mode Governor Interface tailored for mechanical governors (Mode A) and electronic ECUs (Mode B)

- Mode A (Mechanical Governors): For older diesel engines equipped with servo motors, the PLC utilizes digital outputs (Y0, Y1) to drive interposing relays (K-INC, K-DEC). The control algorithm employs PDM to jog the motor for fine speed adjustments.
- Mode B (Electronic Governors): For modern engines with ECUs, the PLC utilizes its built-in analog output channel to send a continuous 4-20 mA reference signal via a shielded cable, providing precise and smooth speed control.

This flexible hardware configuration allows the PMS to be deployed on diverse vessel fleets without hardware modification.

3. IMPLEMENTATION OF CONTROL STRATEGIES

The proposed PMS utilizes a hybrid control strategy where time-critical tasks are executed via hardware interrupts to ensure deterministic behavior, while steady-state regulation is managed via the Modbus communication loop.

3.1 The fast loop: Precision synchronization logic

To validate the non-deterministic nature of the standard communication layer, 1,000 Modbus RTU polling cycles were analyzed on the testbed (comprising 3 meters at 19,200 bps). The results revealed a fluctuating latency ranging from 224.2 ms (theoretical minimum) to 375.4 ms (maximum due to CRC-related timeouts), with an average of 238.8 ms. Given the 20 ms period of a 50 Hz grid, this random delay—equivalent to 11–18 electrical cycles—makes deterministic phase tracking via software polling theoretically unfeasible. While future commercial implementations could utilize Modbus TCP/IP over Ethernet to reduce polling time, network-induced jitter remains a challenge for microsecond-level synchronization. This directly justifies the necessity of the proposed hardware-interrupt-driven SCU to ensure absolute precision. Consequently, the total loop delay can be expressed as the sum of communication and processing latencies:

$$T_{total} = T_{wire} + T_{PLC} + T_{meter} \approx 200 \div 300ms \quad (1)$$

where, T_{total} is the total communication loop latency in milliseconds (ms), T_{wire} represents the physical data transmission time over the RS485 network (ms), T_{PLC} is the main scan cycle delay of the PLC (measured via online monitoring at approximately 5 ms for the Delta DVP-20SX2), and T_{meter} denotes the internal processing and analog-to-digital conversion time of the energy meter (ms). This total delay establishes the steady-state monitoring update rate at 200 ÷ 300 ms per cycle.

At a grid frequency of 50 Hz ($T_{cycle} = 20ms$), a latency of 200 ms corresponds to 10 full cycles, making the phase angle data received by the PLC completely obsolete and random relative to the current state. To overcome this, the system employs hardware interrupts combined with high-speed internal timers, as depicted in Figure 5.

3.1.1 Interrupt-driven period measurement

Instead of counting pulses over a fixed window, the system measures the exact period (T) of each AC cycle. The PLC is configured to trigger immediate interrupts on the rising edge of the ZCD signals provided by the SCU:

- Interrupt Request (IRQ) X0 (Busbar ZCD): Upon detecting a rising edge at input X0 (labeled as IRQ X0 in Figure 5), the PLC executes the corresponding

Interrupt Service Routine (ISR) to capture the reference time base.

- IRQ X1 (Generator ZCD): Similarly, the signal at X1 triggers the Generator ISR to capture the incoming unit's timing.

Inside each ISR, the CPU executes a "snapshot" operation, moving the instantaneous value of the 100 µs resolution timer (D1015) into holding registers (T_{Bus} and T_{Gen}). The period of the current cycle is calculated as the difference between consecutive snapshots, allowing the frequency $f = 1/T$ to be updated every 20 ms with a resolution of 0.05 Hz.

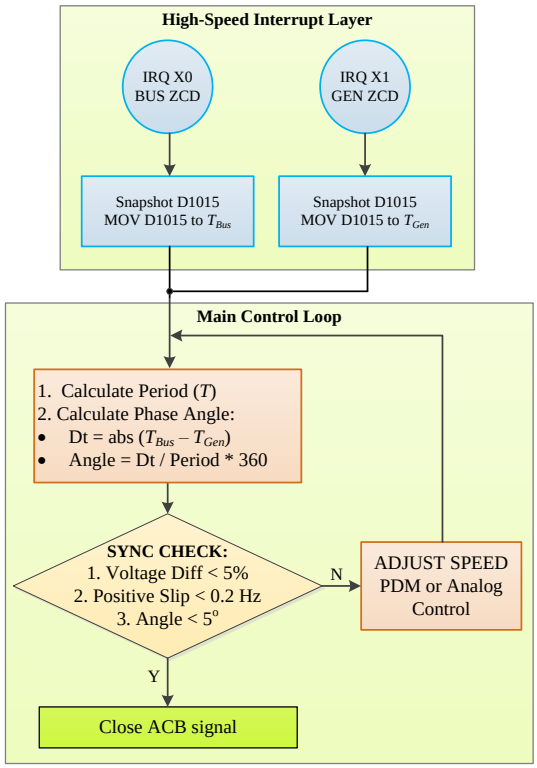

Figure 5. Flowchart of the proposed interrupt-driven synchronization algorithm

3.1.2 Real-time phase difference estimation

The phase difference is derived from the time lag between the two interrupt events. As illustrated in the "Main Control Loop" block of Figure 5, the PLC calculates:

$$\Delta t = | T_{Bus} - T_{Gen} | \tag{2}$$

where, Δt is the absolute time lag between the busbar and generator zero-crossing events expressed in hardware timer counts, and T_{Bus} and T_{Gen} are the captured snapshot values of the $100\,\mu s$ resolution high-speed timer (Register D1015) triggered at the exact zero-crossing instances of the busbar (IRQ X0) and the incoming generator (IRQ X1), respectively. This hardware-driven measurement update rate occurs every 20 ms, synchronized with the 50 Hz grid frequency, and operates completely independently of the 5 ms PLC main scan cycle.

(Note: The algorithm includes rollover handling logic to account for the free-running timer resetting from 32,767 to 0).

The phase angle in electrical degrees is then computed relative to the base period:

$$\Delta\theta = \left(\frac{\Delta t}{T_{cycle}} \right) \times 360 \tag{3}$$

where, $\Delta\theta$ is the real-time phase angle difference evaluated continuously by the PLC's main loop before issuing the synchronization command (°), and T_{cycle} is the nominal period of the AC grid (20 ms for a 50 Hz system, equivalent to 200 timer counts).

With the 100 µs resolution of the D1015 timer, the maximum quantization error for phase measurement is approximately 1.8° at 50 Hz, which satisfies the stringent synchronization requirements for marine generators as recommended by IEEE Std 1547 [21].

Error Budget and Common-Mode Delay Rejection: To rigorously validate the synchronization precision, it is essential to account for the inherent absolute propagation delays of the SCU hardware (e.g., LM358 slew rate, 4N25 opto-isolation lag). Because the Busbar and Generator AC signals are processed by two structurally identical hardware channels on the SCU, they experience nearly identical absolute latencies. By calculating the relative time difference across the high-speed interrupts, the system achieves differential common-mode rejection, effectively cancelling out the absolute hardware lag.

To empirically verify this, a zero-phase loopback test was conducted on the physical testbed by feeding the exact same AC grid voltage into both the Busbar and Generator inputs simultaneously. The logged phase difference remained strictly bounded between 0 and 1 timer count (0° to 1.8°). This confirms that hardware propagation delays are successfully nullified. Furthermore, since the analog multiplexing relays are statically engaged prior to the synchronization sequence, contact bounce is completely eliminated. Consequently, the total worst-case sensing error is strictly bounded by the timer quantization error (1.8°) and a marginal hardware interrupt jitter (worst-case 20 microseconds, equating to 0.36° at 50 Hz), totaling approximately 2.16°. This precision comfortably satisfies the stringent IEEE Std 1547 requirements.

3.1.3 Synchronization criteria (the sync window)

The PLC continuously evaluates the synchronization conditions shown in the decision block of Figure 5. It is important to note that the real-time phase angle difference is calculated continuously by the PLC exactly at the moment before the close command is issued. To guarantee that the phase angle remains within the strict synchronization window when the contacts actually close, the system accounts for the switchgear's mechanical delay (T_{mech}).

In our 4 kW laboratory setup, the closing element is a contactor. To precisely determine T_{mech}, we detect the actual closing instant using the contactor's normally open auxiliary contact fed back to a PLC high-speed input. By utilizing the internal D1015 high-speed timer (100 µs resolution), the PLC logs the exact time difference between the rising edge of the output close command and the rising edge of the auxiliary contact feedback.

With this programmable compensation integrated, the predictive "Close ACB" command is issued immediately via a high-speed output only when all the following criteria are met simultaneously ("Y" path):

- Voltage Match: $\Delta U < 5\%$ (Monitored via Modbus).
- Positive Slip: $0 < \Delta f < 0.2$ (To ensure positive load pickup).

- Phase Alignment: $\Delta\theta < 5^{\circ}$ (Verified by the High-Speed Timer logic).

If these conditions are not met ("N" path), the system executes the "Adjust Speed" routine to drive the generator parameters into the synchronization window.

Threshold Origins and Sensitivity Analysis: The phase angle threshold ($\Delta\theta \leq 10^{\circ}$) is not arbitrary; it is strictly adopted from IEEE Std 1547-2018 limits to prevent mechanical shaft stress and severe electromagnetic torque transients [21]. The positive slip requirement ($\Delta f \leq 0.2$Hz) is derived from marine commissioning experience, ensuring that the incoming generator runs slightly faster than the busbar to immediately pick up the active load, thereby preventing reverse-power protection trips. Furthermore, a sensitivity check was conducted on the phase window during the testbed tuning phase. Tightening the acceptable phase error to 5° significantly reduced the synchronization success rate, leading to prolonged engine hunting and delayed coupling. Conversely, widening the window to 15° allowed for faster coupling but resulted in observable transient inrush currents. Therefore, retaining the 10° threshold provides the optimal engineering balance between rapid operational readiness and electrical safety across standard marine Air Circuit Breakers (ACBs).

3.2 The slow loop: Load sharing and governor control

Once the breaker is closed, the control priority shifts to Load Sharing. Since this process has a slower dynamic response requirement, it is handled via the Modbus loop.

3.2.1 Active power sharing

The PLC continuously polls the active power from the energy meters. The error signal is calculated as the difference between the actual load and the calculated average load of the system:

$$e(t) = P_{meas} - P_{avg} \tag{4}$$

where, $e(t)$ is the active power tracking error in kilowatts (kW), P_{meas} represents the actual active power feedback polled from the generator's energy meter via Modbus RTU (kW), and P_{avg} is the calculated average active load demand of the parallel system (kW). This control loop is executed at the slower Modbus update rate of $200 \div 300$ ms.

3.2.2 Dual-mode output control

Based on the hardware configuration (Mode A or B) selected in Figure 4, the controller adjusts the engine speed to drive $e(t) \to 0$:

- **For Mechanical Governors** (Mode A): The PLC applies a PDM algorithm via digital outputs (Y0, Y1). If the error $|e(t)|$ is large, the relay pulse width is increased for fast response. If $|e(t)|$ is small, the pulse width is reduced to prevent hunting.
- **For Electronic ECUs** (Mode B): The PLC implements a Discrete PI Controller to adjust the 4-20mA analog output signal:

$$u[k] = K_p e[k] + K_i \sum e[i] \tag{5}$$

where, $u[k]$ is the continuous 4-20 mA analog speed reference signal sent to the ECU at the discrete sampling step k, while K_p and K_i are the proportional and integral gains, respectively, which are dynamically tuned to accommodate the transient dynamics of the physical 4 kW testbed.

This dual-loop strategy ensures that the PMS delivers both high-speed precision for synchronization and stable performance for load sharing.

4. EXPERIMENTAL VALIDATION

To verify the feasibility and robustness of the proposed PLC-based PMS, a comprehensive experimental validation was conducted on a laboratory-scale testbed, as shown in Figure 6. The experiments were structured into three critical operational scenarios:

- Scenario 1: Evaluates the transient response of a single generator under step-load changes.
- Scenario 2: Benchmarks the synchronization precision and safety logic of the PLC against a commercial relay.
- Scenario 3: Demonstrates the integrated parallel operation, encompassing the complete sequence from automatic synchronization to dynamic active power load sharing.

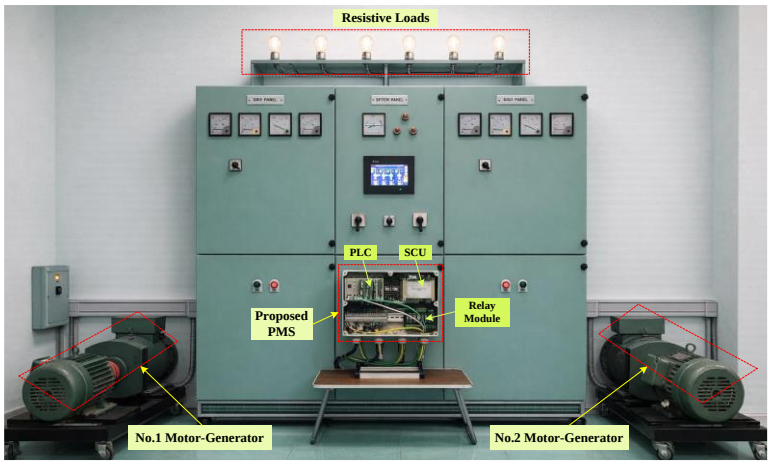

Figure 6. Experimental setup of the laboratory-scale testbed used to validate the proposed Programmable Logic Controller (PLC)-based Power Management Systems (PMS)

4.1 Hardware setup and system configuration

The proposed PMS was validated on a laboratory-scale test bench designed to emulate shipboard power dynamics, as shown in Figure 6. The setup comprises two 4 kW motor-generator sets. The detailed technical specifications of the hardware components and the specific system settings used for the validation are summarized in Table 1. To replicate diesel engine characteristics (specifically speed droop), the prime movers are 3-phase induction motors driven by LS iG5A Variable Frequency Drives (VFDs) configured in slip compensation mode.

The control architecture is centralized around a Delta DVP-SX2 PLC, selected for its high-speed I/O capabilities required for precision synchronization. Electrical parameters are acquired via Selec MFM384 meters over a Modbus RTU network. A commercial SYC6714 relay is installed in parallel to serve as a performance benchmark.

Software Scaling for Logic Thresholds (Not Physical Similarity): To validate the algorithm's decision-making logic for industrial applications using the 4 kW hardware, a software scaling strategy was implemented. It is crucial to clarify that this scaling is strictly intended to test software logic thresholds and ranges (e.g., HMI display limits, percentage-based load sharing alarms), and does not represent strict physical similarity. Parallel generator behavior fundamentally depends on physical inertia, governor time constants, and machine reactances, which differ significantly between a 4 kW and a 100 kW system. Therefore, to ensure stability on the laboratory testbed while validating the core algorithms, the control parameters were handled as follows:

- Parameters Kept Constant: The synchronization safety windows (Voltage diff < 5%, Positive Slip < 0.2 Hz, Phase error < 5°), the hardware interrupt measurement rate (20 ms), and the Modbus monitoring update rate (200-300 ms) were kept identical to industrial standards.
- Parameters Tuned/Changed: To accommodate the low inertia of the 4 kW laboratory plant, the PI controller gains (K_p, K_i) were experimentally tuned specifically for this testbed. Additionally, the physical load sharing deadband was set to actual bench capabilities (± 0.5 kW) to prevent continuous hunting.

Justification of the Key Claim: While the transient power dynamics are specific to the 4 kW setup, this does not distort the key claim of this study. The primary contribution—the hybrid communication architecture and interrupt-based phase measurement—is purely a timing and signal-processing solution. Because the period of a 50 Hz AC grid (20 ms) and the PLC's internal scan latencies remain physically identical regardless of the generator's mechanical size or power rating, validating the precision of the synchronization logic on a 4 kW testbed rigorously proves the effectiveness of the proposed architecture. This scalable Hardware-in-the-Loop methodology directly substantiates the third claimed contribution of this paper, providing a rigorous framework to verify industrial-grade limits on bench-scale equipment.

4.2 Experimental scenarios and performance criteria

To validate the efficacy and safety of the proposed PLC-based PMS, the experimental procedure is structured into three distinct scenarios. These scenarios are rigorously designed to ensure compliance with international maritime regulations and electrical standards, specifically the IACS UR M3 for machinery installations and IEEE Std 1547 for grid interconnection limits. The specific performance metrics and their corresponding reference standards are detailed in Table 2.

Table 1. Experimental parameters and system settings

Category	Parameter / Component	Specification / Value
Prime Mover (Diesel Emulation)	Type	3-Phase Induction Motor (Asynchronous)
	Rating	4 kW, 1435 rpm, 50 Hz
	Voltage / Connection	220/380 V (Δ / Y)
Drive System	Inverter Model	LS iG5A (5.5 kW)
	Control Mode	V/f with Slip Compensation
Generator	Physical Rating	4 kVA, 380 V, 50 Hz, 4-Pole
	Logical Rating (P_{rated})	100 kW (Software Scaled)
	Scaling Factor (K)	25
System Settings	Sync. Safety Window	$\Delta U \leq 5\%$, $\Delta f \leq 0.2$ Hz, $\Delta\theta \leq 10^o$
	Load Sharing Deadband	± 0.5 kW

Table 2. Experimental scenarios and validation standards

ID	Scenario Name	Performance Metrics (Thresholds)	Reference Standard / Basis
SC-1	Frequency Stability	Recovery time ≤ 5s Transient dip ≤ 10%	IACS UR M3 (Clause 3.2.2) (Governor Response Requirement)
SC-2	Precision Synchronization	Phase error $\leq \pm 10^0$ Voltage diff $\leq \pm 5\%$	IEEE Std 1547-2018 (Strictest limits for safe synchronization)
SC-3	Active Load Sharing	Power Diff ≤ 15% P_{rated} (Set at ±0.5 kW for testing)	IACS UR M3 (Clause 3.2.6) (Parallel Operation Limits)

As outlined in Table 2, the validation criteria are established based on the most rigorous standards to ensure operational safety:

- First, regarding frequency stability (SC-1): The system verifies the dynamic response of the diesel governor. In accordance with IACS UR M3 (Rev.7, Clause 3.2.2) for auxiliary engines, the frequency must recover to the steady-state band within 5 s following a sudden load application, with a transient deviation not exceeding 10%.
- Second, for synchronization (SC-2): While marine standards generally mandate smooth integration without harmful surges, this study adopts the stricter IEEE Std 1547-2018 threshold. The phase angle

difference at the instant of breaker closure is limited to ±10° to minimize electromagnetic torque impact on the generator shaft and coupling.

Finally, for active load sharing (SC-3): The controller is tested for its ability to balance the active power between generators. The control deadband is set at ±0.5 kW, which ensures the load imbalance remains significantly below the 15% of rated power limit mandated by IACS UR M3 (Clause 3.2.6) for parallel operation, thereby preventing system hunting while satisfying classification society requirements.

4.3 Results and discussion

4.3.1 Experimental analysis of frequency recovery and stability

The dynamic response of the proposed PMS under sequential load step changes is visualized in Figure 7. The experiment was designed to verify the controller's compliance with IACS UR M3 regulations regarding recovery time and transient deviations.

Data Logging and Time Computation: To ensure traceability, all transient data were logged directly into the PLC's internal memory. The sampling rate was determined by the control architecture: 20 ms resolution for frequency/phase parameters (driven by hardware interrupts) and 200 ms for active power (polled via Modbus RTU). The critical event markers (t_0, t_1, t_3) are mathematically defined as follows: t_0, t_1, and t_3 represent the exact timestamps when the first load step (Load 1 On), the second load step (Load 2 On), and the final load rejection (Load 1 Off) commands were physically applied, respectively. The recovery markers t_2 and t_4 represent the exact timestamps when the measured frequency securely re-entered and remained within the steady-state tolerance band (± 0.25 Hz) defined by IACS UR M3. The recovery duration is calculated simply as $\Delta t = t_{\text{recovery}} - t_{\text{event}}$.

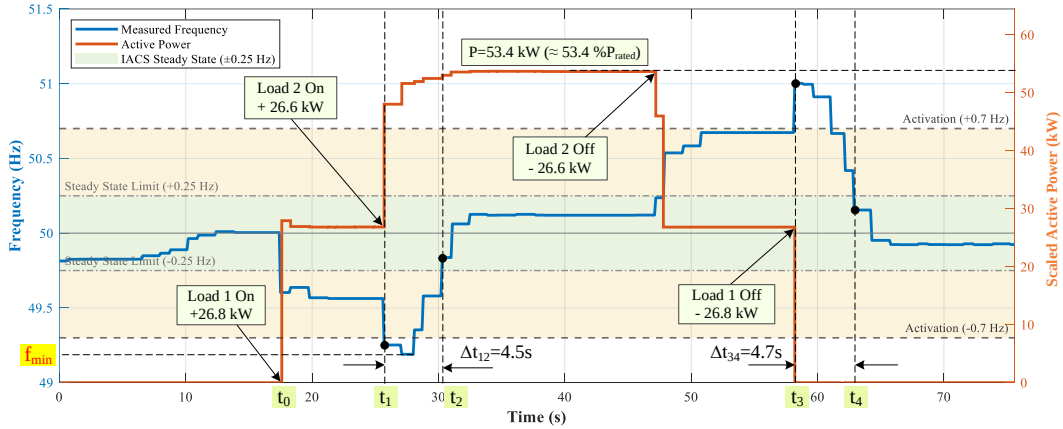

Figure 7. Experimental response of generator frequency under sequential load steps and load rejection verifying compliance with IACS UR M3 limits

Load Application Phase: Initially, the generator operated at a steady state. At t_0, the first physical load step of + 1.07 kW (equivalent to a scaled logical power of + 26.8 kW, applying K = 25) was applied. The frequency experienced a minor dip due to natural droop but remained within the activation deadband (> 49.3 Hz), keeping the PMS in idle mode to prevent unnecessary hunting. At t_1, a second physical load step of + 1.07 kW was introduced, bringing the total cumulative physical load to 2.14 kW (representing a scaled logical load of 53.4 kW, or approximately 53.4% of the rated logical power). This scenario simulates a severe loading condition that satisfies the IACS requirement for prime movers to accept a sudden load of at least 50% of the rated power. As a result, the frequency dropped sharply to a nadir f_{min} approx 49.25 Hz (marked in red in Figure 7). This value breached the lower activation threshold (-0.7 Hz), automatically triggering the hysteresis control loop.

Recovery Performance: Despite the significant load impact, the controller successfully restored the frequency to the IACS-defined steady-state zone (within ±1% or ±0.5 Hz envelope). The recorded recovery time was Δt_{12} = 4.5 s. This performance is strictly within the 5 s limit mandated by IACS UR M3 Section 3.2.1.

Furthermore, regarding the transient deviation, the recorded minimum frequency (f_{min} = 49.25 Hz) represents a deviation of only 1.5%. This provides a substantial safety margin compared to the maximum permissible transient frequency variation of ±10% (which would allow a drop to 45 Hz).

Load Rejection Phase: Following the sequential unloading process (where Load 2 was previously removed), a final load rejection was performed at t_3. At this instant, the remaining physical load of 1.07 kW (equivalent to a scaled logical load dropping from 26.8 kW to 0 kW) was abruptly disconnected to evaluate the system's worst-case overspeed response. The frequency spiked due to the sudden loss of electromagnetic torque, but the PMS intervened effectively. The system returned to the stable band within Δt_{34} = 4.7 s, once again satisfying the 5 s recovery rule without tripping the overspeed protection device.

Conclusion: The results demonstrate that the hysteresis-based PMS logic not only ensures compliance with international maritime standards (IACS UR M3) but also maintains high stability with minimal transient deviations under heavy load steps.

4.3.2 Scenario 2: Automatic synchronization

Synchronization Logic: To ensure a seamless connection without mechanical shock, the PMS employs a precision synchronization algorithm that continuously monitors the phase angle difference ($\Delta\theta$), voltage deviation (ΔU), and slip frequency between the incoming generator and the busbar. The ACB closure command is strictly interlocked, issued only when the phase error enters the safety window of ± 10° (benchmarked against IEEE Std 1547) and the voltage difference remains within ± 5%. Crucially, the algorithm enforces a positive slip condition ($f_{Gen} > f_{Bus}$) to ensure the

generator immediately picks up load upon connection, preventing reverse power incidents.

Experimental Analysis: The dynamic synchronization process is analyzed across discrete time intervals (t_1 to t_4) as illustrated in Figure 8.

- **Phase Matching**: Initially, the phase error oscillates due to the slip frequency. It is noted that the phase angle data exhibits a discrete scattering pattern; this is an inherent characteristic of the hardware resolution (where the PLC high-speed timer results in a quantization step of 1.8° per count at 50 Hz). Despite this, the controller effectively trends the phase error toward zero.
- **Safety Interlock at t_1**: At the first phase alignment ($t \approx 86.9$ s), the commercial relay (SYC6714) issued a close command. However, the proposed PLC algorithm suppressed this action. The data indicates that at t1, although the phase error was small, the generator frequency was slightly lower than or equal to the bus frequency ($f_{Gen} \leq f_{Bus}$). Closing at this instant would risk motoring; thus, the PLC correctly blocked the operation, demonstrating deterministic safety interlock.
- **Latency Compensation and Strategy Comparison**: Following frequency adjustment, both controllers identified the valid closing windows. However, the PLC consistently triggered the output with an average total lead time of approximately 0.35 s compared to the SYC6714. It is critical to note that this earlier trigger is not merely a result of faster processing latency, but stems from a fundamentally different control strategy. The commercial relay operates on a reactive logic without programmable compensation, whereas the PLC employs a predictive mechanical delay compensation strategy.

To rigorously compare these strategies using outcome metrics, the physical command-to-aux-contact mechanical delay of the testbed switchgear was measured over 30 trials, yielding T_{mech} = 115 ± 4.5 ms. During commissioning, the predictive lead time (T_{comp}) on the PLC's HMI was conservatively set to 100 ms. Despite this slight under-compensation, the physical contacts closed with a highly precise phase alignment of 1.9° ± 0.70° (Max error: 3.24°). In contrast, due to the lack of T_{mech} compensation and internal filter latencies, the SYC6714's physical contact closure occurred roughly 465 ms after the ideal zero-crossing point, allowing the phase to drift to 8.1° ± 0.8° (Max error: 9.87°).

While both controllers achieved a 100% synchronization success rate safely within the strict ±10° boundary stipulated by IEEE Std 1547, the statistical distribution (visualized in Figure 9) definitively proves the advantage of the PLC's predictive architecture. By tightly minimizing the contact-closure phase error—which serves as the primary proxy for electromagnetic torque shocks and inrush currents—the proposed PMS significantly reduces mechanical stress on the generator shaft during coupling.

Conclusion: The results validate that the proposed synchronization routine operates at the limit of hardware precision. By intelligently filtering out unsafe conditions (at t_1) and providing a predictive closing signal to offset mechanical inertia, the system enhances both operational safety and synchronization accuracy compared to standard commercial relays. These metrics directly validate the first contribution, proving that the interrupt-driven SCU architecture effectively eliminates communication jitter and mathematically outperforms conventional relay latency.

Operational Flexibility and HMI Integration: Beyond the response speed, a critical limitation of the benchmarked commercial relay (SYC6714) is its reliance on a static phase window check without an adjustable mechanism for breaker closing time compensation. The relay simply triggers when the phase error is within the preset limits, neglecting the specific mechanical inertia of different breaker types (which typically ranges from 50 ms to 200 ms for marine ACBs). Conversely, the proposed PLC-based algorithm treats the Breaker Mechanical Delay (T_{mech}) as a programmable parameter adjustable via the Human-Machine Interface (HMI). This feature allows marine engineers to fine-tune the "Lead Time" to match the exact characteristics of the installed switchgear during commissioning. This software-defined flexibility ensures that the zero-crossing contact closure remains precise even when the PMS is retrofitted onto vessels with diverse or aging equipment, a capability unattainable with traditional analog relays.

4.3.3 Scenario 3: Active power load sharing

Control Strategy: Upon synchronization, the PMS activates the active power load sharing loop. To demonstrate the controller's scalability for industrial applications, a Software Scaling Strategy is implemented. While the physical test bench operates with a small-scale generator, the PLC control logic processes the feedback signals using a scaling factor (K = 25). This normalizes the system to a 100 kW logical reference, allowing the PI gains, deadbands, and protection thresholds to be evaluated against standard industrial ratings.

Experimental Analysis: The system response during automatic synchronization and load sharing is visualized in Figure 10. The process is divided into two distinct phases:

- Synchronization Phase (t < 68 s): The PMS adjusted the frequency of the incoming generator (Gen 2) to track the bus reference (Gen 1). The breaker closure command was issued at t = 68 s once the phase and frequency conditions were satisfied.
- Load Transfer Dynamics: Immediately after breaker closure, the controller initiated the load equalization process. As shown in the graph, the PMS ramped up the load on Gen 2 ("Loading") while simultaneously reducing the load on Gen 1 ("Unloading"). This cross-adjustment ensured a smooth power transfer without causing total load fluctuations.
- Steady-State Accuracy: The system achieved a balanced steady state at t approx. 85 s. The final steady-state difference between the two units was recorded at merely 0.004 kW of physical power on the testbed (corresponding to a scaled logical power difference of 0.10 kW).

Conclusion: The experimental results demonstrate high load sharing precision. The residual scaled deviation of 0.10 kW is negligible compared to the permissible margin of ± 15 kW (15% of Prated) allowed by the IACS UR M3 standard. This confirms that the proposed algorithm achieves a relative sharing error of less than 0.1% (calculated against the 100 kW logical rated base capacity, Prated), proving the robustness of the control logic even under scaled industrial conditions. Coupled with the rapid frequency recovery demonstrated in Scenario 1, these precise load-sharing dynamics fully validate the second contribution, confirming the operational efficacy of the Universal Dual-Mode Governor Interface.

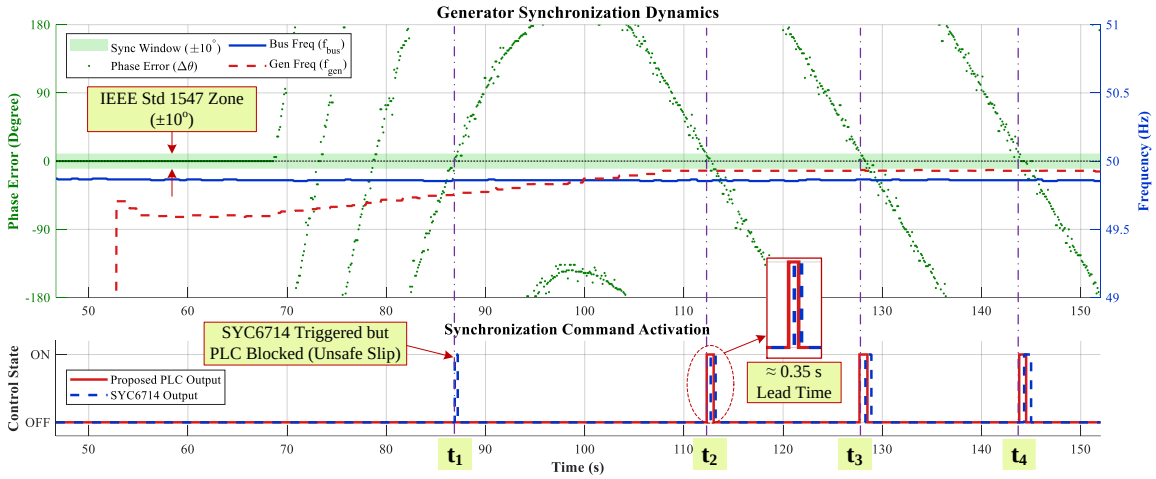

Figure 8. Experimental comparison of synchronization dynamics between the proposed Programmable Logic Controller (PLC) algorithm and the commercial SYC6714 relay

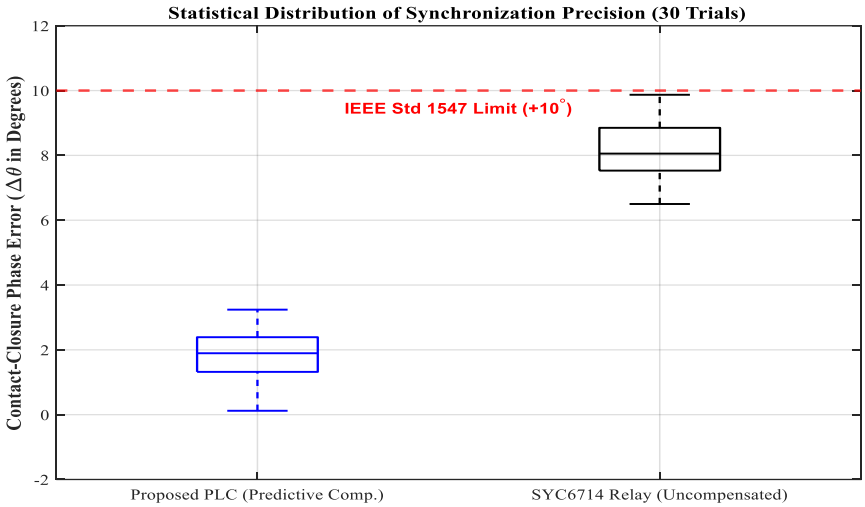

Figure 9. Statistical distribution of contact-closure phase errors during synchronization

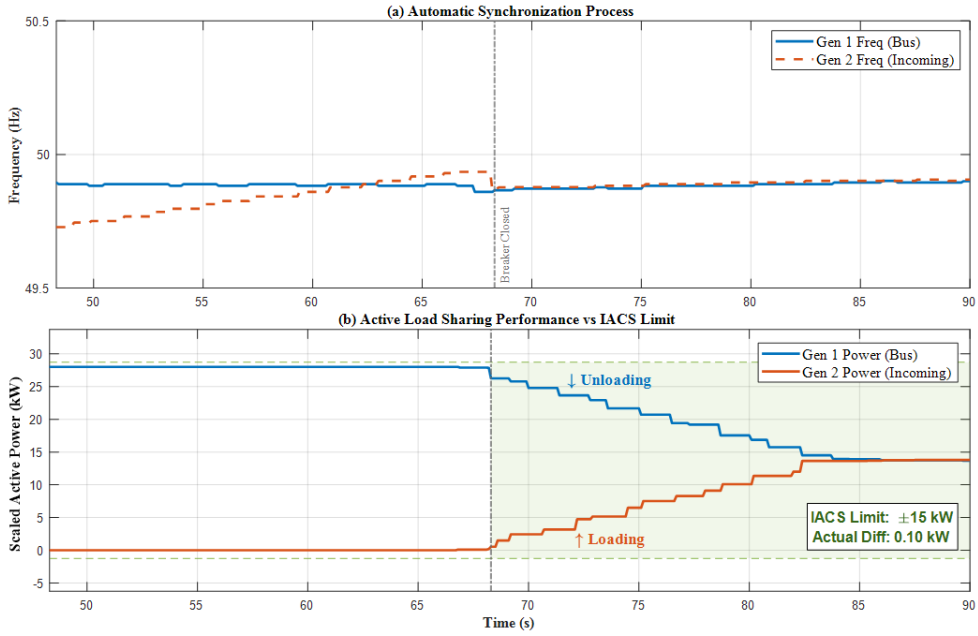

Figure 10. Experimental verification of automatic synchronization and active load sharing performance in compliance with IACS UR M3 regulations

5. CONCLUSION AND FUTURE WORK

This study presents a comprehensive validation of a cost-effective PMS based on standard industrial PLCs. The core contribution is the development of a Hybrid Communication Architecture that integrates interrupt-driven signal conditioning with standard Modbus RTU. By successfully decoupling the time-critical synchronization logic from the stochastic communication latency, the proposed architecture offers a viable solution to reduce the dependency on dedicated external auto-synchronizers without compromising operational safety.

The experimental results obtained from the 4 kW hardware-in-the-loop testbed confirm the system's robustness and precision:

- Synchronization Accuracy: The system achieved a phase angle difference of less than 1.8° and a voltage difference under 1.5%, satisfying the strict requirements of IEEE Std 1547.
- Dynamic Response: Load sharing stability and frequency recovery were maintained within 4.5 s, fully complying with IACS UR M3 standards for marine vessels.
- Methodological Validity: The successful application of the Unit-Per-Unit (pu) scaling strategy demonstrates that the control logic, although tuned for the fast dynamics of a laboratory setup, is mathematically scalable for deployment in larger commercial power systems (e.g., 100 kW).

While the current centralized design and laboratory prototype successfully prove the feasibility of a "software-defined synchronization" approach, transitioning this architecture to full-scale commercial maritime deployment requires specific hardware upgrades to withstand harsh marine environments. Future work will focus on replacing the prototype's mechanical relays with industrial-grade Solid-State Relays (SSRs) or IP67 hermetically sealed analog switches to guarantee long-term reliability against vibration and salt. Furthermore, the 4N25 optocouplers will be upgraded to high-speed digital isolators (e.g., logic-gate optocouplers) to provide enhanced noise immunity and thermal stability. To mitigate the communication bottleneck observed in the serial RS485 daisy-chain, future commercial iterations will utilize high-end multi-function meters equipped with Modbus TCP/IP over Ethernet. To address the risk of a single point of failure inherent in standalone controllers, we will prioritize the development of a dual-PLC Hot-Standby configuration to meet higher Safety Integrity Levels (SIL). Additionally, further research will integrate AI-based load forecasting algorithms to optimize fuel efficiency under dynamic sea conditions, extending the system's capability from basic automation to intelligent energy management.

ACKNOWLEDGMENTS

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NOMENCLATURE

ACB	Air Circuit Breaker
HMI	Human-Machine Interface
IACS	International Association of Classification Societies
PDM	Pulse Duration Modulation
PLC	Programmable Logic Controller
PMS	Power Management System
pu	Per-Unit
SCU	Signal Conditioning Unit
ZCD	Zero-Crossing Detection
f	Frequency, Hz
K	Software scaling factor for active power
K_i	Integral gain of the PI controller
K_p	Proportional gain of the PI controller
P	Active power, kW
T	Hardware timer snapshot or time duration, counts or ms
u	Instantaneous AC voltage, V

Greek symbols

Δf	Slip frequency, Hz
Δt	Absolute time lag between zero-crossing events, counts
ΔU	Voltage magnitude deviation, %
$\Delta \theta$	Phase angle difference, °

Subscripts

avg	Calculated average demand
Bus	Main busbar
cycle	Nominal AC grid cycle
Gen	Incoming generator
meas	Measured actual value
mech	Mechanical closing delay
rated	Logical rated value