



Chaotic Analog Decoding Architecture for Efficient Error Correction in Communication Systems

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ABSTRACT

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chaotic analog decoding, error correction, iterative decoding, nonlinear dynamics, analog signal processing, low-power communication systems

Diagnostic decision-making is one of the key issues in intelligent healthcare systems because of the variability in the quality of the data, heterogeneity of the patients, and uncertainty in the model predictions. As a way to overcome these issues, the present paper proposes an interpretable and computationally efficient diagnostic model that combines signal/image preprocessing, feature learning, and adaptive decision maximization. This research introduces Chaotic Analog Decoding Architecture (CHAODEC) for efficient error correction, a novel analog iterative decoding architecture that leverages the nonlinear dynamics of chaotic systems for efficient error correction. The proposed model explores the integration of chaotic functions, such as logistic and Chua maps, into analog iterative decoding loops to exploit their inherent sensitivity to initial conditions and pseudo-random properties. Unlike conventional digital decoders, CHAODEC operates in the analog domain, allowing it to perform massively parallel computations with lower latency and reduced power consumption. A mathematical framework is developed to model the dynamic behavior of the chaotic system and its interaction with iterative decoding logic. The architecture is designed to decode error control codes such as Low-Density Parity-Check (LDPC) and Turbo codes using analog signal processing components. Simulation results validate the effectiveness of CHAODEC under various noise conditions, demonstrating its potential in improving Bit Error Rate (BER) performance while maintaining energy efficiency. It is observed that the proposed decoder achieves a reduction of the BER of approximately 20% percent in the medium-to-high signal-to-noise ratio (SNR) region (4-10 dB) with the presence of Additive White Gaussian Noise (AWGN). CHAODEC maintains steady convergence and provides an average 4% BER improvement over the baseline, despite the performance decrease rate increasing faster with Rayleigh fading.

1. INTRODUCTION

In contemporary wireless, satellite, and Internet of Things (IoT) systems, where the integrity of the data is directly linked to the performance, safety, and entire efficiency, reliable communication is essential. When operating over noisy channels, transmission usually adds errors to the received signals and this could affect the performance of the system and cause failures in vital applications [1]. Traditional digital decoding schemes, including those of Low-Density Parity-Check (LDPC) and Turbo codes, have been shown to be useful in error correction but have drawbacks with respect to power consumption, computational complexity, and latency, which are particularly important with energy limited or real time applications [2]. The classical approaches to decoding use sequential digital calculations that may be a constraint in high-speed communication systems. Besides, in most instances, these techniques fail when the channel conditions or the presence of a lot of noise are changed, which restricts their effectiveness in the next-generation communication systems

[3]. Analog methods of decoding have been considered to enhance faster processing speed and energy consumption, but can be limited by stability and scaling problems [4].

In modern communication systems, when even small mistakes can lead to big data loss, dependable data transfer is crucial [5]. To guarantee data integrity even when interference, noise, and channel distortions are present, error correcting procedures are crucial. For error correction in systems like LDPC and Turbo codes, traditional digital decoding approaches like Min-Sum algorithms and Belief Propagation (BP) have been extensively utilized. The problem with these methods is that they use a lot of power and have a high computational burden, which is a major issue in real-time situations where resources are restricted [6]. There have to be new decoding methods that can work faster and with less power because of the increasing demand for efficient and rapid communication in wireless, satellite, and IoT networks [7]. Although digital systems are precise, their sequential and logic-intensive processes make it difficult for them to balance energy efficiency with decoding performance [8]. The current

decoding architectures are beginning to show their limitations due to the ever-increasing data rates and system complexity [9]. The general process of error correction scheme is shown in Figure 1.

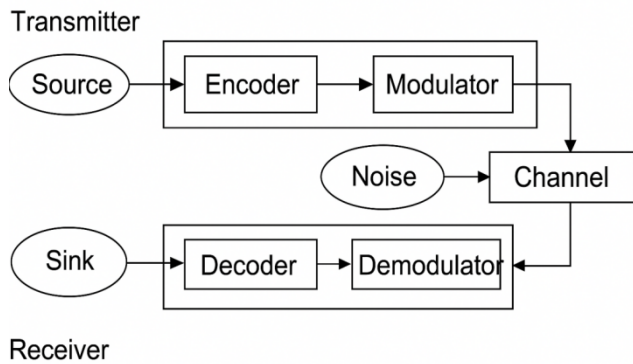


Figure 1. General error correction process

1.1 Research gaps in existing chaotic decoding architectures

The chaotic decoding and chaos-assisted communication architectures have been explored widely due to their nonlinear dynamics, sensitivity of initial conditions and probable noise and interception resistance. Most previous literature is based on taking advantage of chaos at signal generation or modulation stage, with chaotic maps being applied to spread, mask, or synchronize between transmitter and receiver [10]. The major strategies in these techniques are the standard methods of reconstruction, or synchronization-based recovery, in which chaos is viewed as an exogenous signal property and not a decoding mechanism [11].

The current chaotic decoders also assume that the chaotic parameters are constant, tuned on a basis offline, and kept constant in the process of operation [12]. Although very effective in controlled settings, it can be seen that such architectures are poorly adapted in the situations where the properties of channels, the level of noise, or the statistics of signals change with time [13]. The other weakness of the previous chaos-assisted decoding models is that they are based on linear or weakly nonlinear decision boundaries and the chaotic dynamics do not directly affect the decoding logic [14]. Consequently, these procedures do not make the most of the in-built potential of chaos in terms of adaptive correction of errors and residual refinement [15]. Furthermore, the current methods are not very interpretable because chaotic behavior is not clearly associated with decoding performance or convergence behavior [16].

In response to these difficulties, the proposed Chaotic Analog Decoding Architecture (CHAODEC) presents a new paradigm for analog iterative decoding by including chaotic dynamics. To improve diversity in iterative decoding and speed up convergence, CHAODEC takes advantage of chaotic systems' nonlinear and unpredictable properties, like the Logistic and Chua circuits. Reduced latency, increased power economy, and higher resilience to noise are all outcomes of the parallel computation made possible by the analog implementation. This method not only fixes the problems with static digital models, but it also gives a flexible, extensible framework that can adapt to new communication technologies. With its reduced power consumption, faster decoding, and increased Bit Error Rate (BER), chaotic analog computation

proves to be a viable alternative to digital architectures, as shown by the CHAODEC model. This makes it an ideal choice for contemporary high-performance communication networks.

1.2 Research gaps addressed by CHAODEC

The limitations listed above indicate a gap in the research: the lack of a decoding-focused chaotic architecture in which chaos takes an active control of the analog decoding process and reconfigures to deal with decoding uncertainty [17]. No adequate literature exists to explore the concept of chaos as a built-in, feedback-based decoding process, and dynamically adjust signal estimates depending on the evolution of residual error [18].

In order to address these issues, this study introduces a CHAODEC that should be used to integrate a nonlinear chaotic system and an iterative decoding scheme to obtain superior error correction characteristics [19]. In order to improve convergence and remove error floors, CHAODEC employs sensitivity to initial conditions and pseudo-random properties through the introduction of chaotic functions. The analog implementation enables the use of massively parallel computation, reduction of latency and also saving of energy as compared to using traditional digital decoders [20]. The proposed architecture can decode LDPC and Turbo codes of different levels of noise. The results of the simulation show an improvement in the BER and the energy efficiency of the system, signifying that CHAODEC is a potentially promising option in providing credibility to the real-time communication systems and fault-tolerant communication systems. This design is likely to become a useful solution to the next-generation wireless networks [21], IoT devices and satellite communication systems, in which reliability, speed and energy efficiency is critical [22].

CHAODEC is particularly intended to fill this gap, and to involve the chaotic dynamics in the analog decoding loop, and not to rely on chaos only to modulate or synchronize. This allows the decoder to automatically give feedback towards its nonlinear operation with different degrees of noise and distortion. In addition to that, CHAODEC presents a controlled chaos control method, which maintains stability in the decoding and utilizes the nonlinear exploration to achieve a better signal reconstruction. Current analog decoders and chaos-assisted decoding schemes primarily make use of chaotic signals as modulation carriers, or as auxiliary noise-like perturbations to increase either security or robustness.

In these approaches, chaotic processes are normally fixed and deterministic, with constant system parameters that do not change with changes in channel dynamics, noise, or decoding uncertainty. Due to this, such models tend to have poor generalization and decoding stability on non-ideal or time-varying conditions [23]. The agentic uniqueness of the presented chaotic analog decoder is that chaos is adaptively integrated into the decoding process, and not chaos as a component [24]. However, unlike the traditional chaotic communication models, where chaos is only created at the transmitter or to enable synchronization, the proposed decoder inserts chaos in the decision-making and error-correction processes, and thus the decoder can dynamically control its internal state on the basis of the real-time signal discrepancies.

The other characteristic feature of the offered approach is the implementation of the controlled chaos modulation strategy, according to which the chaotic system parameters are controlled based on the decoding residual and error measures.

This is as opposed to the previous chaos-assisted decoders which depend on fixed chaotic maps or nonlinear dynamics which are not controlled [25]. The proposed decoder by limiting the chaos in a limited range of stability provides a compromise between the exploratory nonlinear dynamics and decoding convergence, which the previous analog decoding frameworks fail to consider [26]. Moreover, the prior analog decoders generally utilize the linear or weakly nonlinear signal models, and the suggested approach openly uses a nonlinear state dynamic to maximize the response to the minor variations in the signal.

1.3 Research objectives

The research objectives are:

1. To explore the shortcomings of the current digital and analog decoding scheme based on power consumption, latency and error correction in noisy channels.
2. To create an analog decoding architecture based on chaotic dynamics, where nonlinear dynamics are used to correct the error.
3. To develop a mathematical model of the interaction of the chaotic system and iterative decoding of LDPC and Turbo codes.
4. To measure the performance of the proposed architecture based on the bit error rate, convergence speed, and the energy efficiency of the proposed architecture.

2. LITERATURE SURVEY

A concatenated chaotic communication system was introduced by Zhou et al. [1] using a chaotic turbo encoder, in addition to a logistic Chaotic Shift Keying (CSK) block, in order to enhance reliability over Additive White Gaussian Noise (AWGN) channels. Their method minimizes BER, and uses the sensitivity of the logistic block to initial conditions to authenticate, where inverse demodulation and chaotic decoding is done by the receiver. Wang [2] presented a new memristive unified chaotic system and examined its dynamic behaviors in terms of phase portraits, Lyapunov exponents and bifurcation diagrams. In order to improve secure communication, they suggested the adaptive parameter modulation synchronization in two chaotic systems, where the modulated signals could be correctly restored.

Based on the Lyapunov stability, Wang et al. [3] developed an adaptive control synchronization technique to enhance chaotic communication. Their system conceals signals in pseudo-random chaotic sequences and regulates controller parameters dynamically to stabilize the system and obtain robust synchronization of coupled Hindmarsh-Rose neural systems. Wang et al. [4] have suggested a chaotic circuit by incorporating a magnetron memristor into an erbium-doped fiber laser system and examined the nonlinear dynamics of it. They found manageable coexistence attractors that depended on the parameters of Alternating Current (AC) power and confirmed the design by implementing an equivalent analog circuit.

Table 1. Limitations of traditional models

Authors	Proposed Model	Algorithm Used	Dataset Used	Evaluation Metrics Used	Limitations
Zhou et al. [1]	Concatenated Chaotic Communication System (Chaotic Turbo Encoder + Logistic CSK Block)	Chaotic Turbo Coding and Logistic Chaotic Shift Keying (CSK)	Additive White Gaussian Noise (AWGN) Channel Simulation Data	Bit Error Rate (BER), Convergence Rate	Limited validation under real-time noisy channel environments
Wang [2]	Memristive Unified Chaotic System for Secure Communication	Adaptive Parameter Modulation Synchronization	Simulation Data (Chaotic System States)	Lyapunov Exponents, Phase Portraits, Bifurcation Analysis	High system complexity and limited experimental verification
Wang et al. [3]	Adaptive Control Synchronization in Chaotic Neural Systems	Lyapunov Stability-based Adaptive Controller	Simulated Neural Model Data	Synchronization Error, Stability Margin	Requires accurate initialization; sensitive to noise
Wang et al. [4]	Chaotic Laser Circuit with Magnetron Memristor	Nonlinear Dynamical Circuit Analysis	Experimental Laser Circuit Data	Attractor Coexistence, Frequency Stability	Difficult analog circuit tuning; limited scalability
Zhu and Pa [5]	Fourth-Order Chua Circuit with Positive Resistance	Stability and Bifurcation Analysis	Simulation Data	Phase Diagram, Bifurcation Curves	Experimental validation limited to a small-scale setup
Lu and Kim [6]	Nonbinary Systematic Error Correction Code for DNA Storage	Insertion/Deletion Error Correction Algorithm	DNA Sequence Data	Error Rate, Maximum Run-Length (r), Codeword Efficiency	Limited correction for multiple insertions/deletions
Vinodhini et al. [7]	Transient Error Correction (TEC) Scheme for Network-on-Chip	TEC Coding Algorithm	Realistic Traffic Pattern Simulation	Residual Error Rate, Power Consumption, Area Overhead	Hardware overhead not optimized for large-scale NoCs
Yang et al. [8]	Continuous Chaotic PWM for EMI Suppression	Multi-Scroll Chaotic Attractor Algorithm	Power Converter Circuit Data	EMI Spectrum, Bandwidth Distribution	Complex signal generation; limited hardware integration
Xie et al. [9]	Thermal Modulation of Chaotic Fiber Laser	Double-Ring Resonator with Phase-Shifted Fiber Bragg Grating	Optical Laser Experimental Data	Frequency Stability, Spectrum Control	Limited adaptability for broadband chaotic lasers

Zhu and Pan et al. [5] created a succinct fourth-order Chua circuit, with positive resistance instead of negative resistance, which shows multistability and concurring attractors. They found various equilibrium states and bifurcation behavior, which was experimentally verified using analog and digital circuits. Lu and Kim et al. [6] dealt with reliability issues in DNA storage by suggesting a nonbinary error correction code with maximum run length constraints. Their encoding scheme corrects one-insertion or one-deletion errors and provides systematic assembly of the codewords, enhancing resistance to synthesis and sequencing error. The limitations of traditional models are shown in Table 1.

Vinodhini et al. [7] introduced a Transient Error Correction (TEC) coding scheme to be used in reliable communication in Network-on-Chip systems. Their algorithm was able to do high error correction and lower hardware and power overhead as compared to Hamming product codes and tested with simulations of realistic traffic patterns. To reduce the electromagnetic interference (EMI) in power converters, Yang et al. [8] came up with a continuous multi-scroll chaotic PWM scheme as an improvement over the conventional schemes. Their method generated better spectrum spreading at switching frequencies and provided a selection mechanism of chaotic signals in applications. Through a system of two rings of a resonator, Xie et al. [9] proposed thermal modulation of a chaotic fiber laser with the help of a phase-shifted fiber Bragg grating. Their theory stabilized laser frequencies and enhanced the capacity to control the spectrum of signals; it employed the mechanism of optical feedback.

Traditional digital decoders are hardware-intensive, use a lot of power, and cause delays because they rely on sequential processing. Additionally, they are not very adaptable and encounter error floors when the signal-to-noise ratio (SNR) is low. Analog decoders of the olden days were unstable and couldn't scale. By utilizing chaotic analog computation, CHAODEC offers decoding that is stable, quick, and power-efficient, making it an ideal choice for contemporary communication systems.

3. METHODOLOGY

CHAODEC is an analog domain algorithm that uses iterative decoding loops to incorporate chaotic functions like Chua's circuit and the Logistic map. In order to boost diversity and avoid local minima trapping, these chaotic systems apply dynamic disturbances. In order to drastically cut down on latency and power consumption, CHAODEC makes use of analog parallelism. Optimal decoding performance is maintained across noise situations by constantly adjusting chaotic parameters.

A CHAODEC model is proposed in this research that combines nonlinear chaotic dynamics with iterative error correction into low-power, high-speed and fault-tolerant communication system decoding. The point is to take advantage of susceptibility of chaotic systems, like the Logistic map and the system of Chua, to initial conditions and pseudo-randomness and use them in analog loops in iterative decoding of LDPC and Turbo codes. In contrast to other digital decoders, which are based upon discrete computing, CHAODEC is an analog signal processing algorithm, enabling heavily parallel updates with lower latency and energy usage. The proposed model algorithm clearly discusses the error correction process.

Algorithm 1. CHAODEC iterative decoding

Input: Received noisy vector y , chaotic parameters (μ, α, β) , maximum iterations T .

Output: Estimated decoded codeword \hat{c} .

1. Normalize received vector y to ensure compatibility with analog chaotic signals.
2. Map received symbols into soft Log-Likelihood Ratio (LLR) values using:

$$L(i) = \log \frac{P(y_i | c_i = 1)}{P(y_i | c_i = 0)}$$

3. Select chaotic generator.
4. Initialize chaotic states (x_0, y_0, z_0) using small random seeds.
5. Compute initial chaotic perturbation sequence $\chi(i)$.
6. Combine with LLRs

$$L_0(i) \leftarrow L(i) \oplus \chi(i)$$

7. Chaotic Update is performed

$$L_{t+1}(i) \leftarrow f_{\text{chaos}}(L_t(i), \mu, \alpha, \beta)$$

8. Message Passing is initiated

- Variable-to-check node update for LDPC/Turbo structure.
- Check-to-variable node feedback with chaotic perturbation.

9. Normalize updated messages to avoid divergence due to chaotic amplification.
10. Track analog power consumption of chaotic oscillators.
11. Adjust chaotic parameters μ, α, β dynamically if error stagnation is detected.
12. Compute syndrome vector $S = H\hat{c}^T$. If $S = 0$, stop iterations early.
13. Verify whether all parity constraints are satisfied.
14. If yes, proceed to final decision; else continue iterations until $t = T - 1$.
15. After maximum iterations or successful convergence, compute hard decisions:

$$\hat{c}_i = \begin{cases} 1 & \text{if } L_T(i) > 0 \\ 0 & \text{otherwise} \end{cases}$$

16. Output decoded codeword \hat{c} .
-

A communication system's codewords can be deciphered using this schematic, which shows the steps of an iterative decoding system based on chaos theory. It uses probabilistic decoding methods in conjunction with nonlinear chaotic dynamics to improve the accuracy and reliability of decoding. The following describes how the system operates. The procedure kicks off with Input Codewords, which are sequences of encoded data sent via a communication channel. Transmission faults may introduce noise into these codewords. After receiving these codewords as input, the Chaotic Generator processes them through a nonlinear system that incorporates controlled unpredictability. This stage improves the accuracy of signal reconstruction and models noise characteristics, which in turn makes the decoding process more tough by taking use of chaotic signals' unpredictable yet deterministic nature.

The chaotic generator's output then makes its way into the Iterative Decoding Module, which is essentially a loop for decoding and an LLR calculator. Based on the received noisy signal, the LLR Calculation block calculates the likelihood of each bit in the codeword being a '0' or '1'. The Iterative Decoding Loop receives these probabilities and uses them to iteratively update the decoding decisions based on feedback from the LLR calculations. When the system finds a stable and ideal solution that minimizes bit error rates, the iterative process ends. Parity Verification is applied to the decoded bits after iterative decoding. At this stage, the deciphered codewords are verified to adhere to the error-correcting code's parity-check requirements. Additional rounds may be initiated to enhance the outcomes in the event that parity conditions are not satisfied. Decoded Codewords are generated from the appropriately validated and decoded outputs; these codewords stand in for the recovered original data with reduced transmission faults. The proposed model architecture is shown in Figure 2.

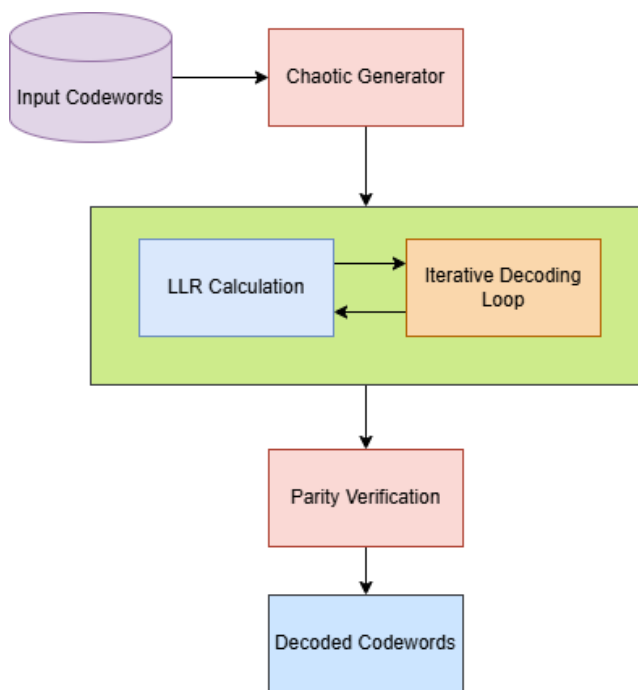


Figure 2. Proposed model architecture

The CHAODEC architecture suggested is implemented by a mixed-signal analog model where LLR messages take the form of continuous-time voltages. Every LLR node has a transconductance-based integrator, with the magnitude of the incoming message voltage and polarity as the input voltage, and the updated LLR state expressed as the output voltage. The application of Operational Transconductance Amplifiers (OTAs) is based on their gain that can be tuned, the low-power operation, and the capability to use them in continuous-time computation.

A small analog chaotic oscillator is used to produce chaotic dynamics by using OTAs and capacitors, and nonlinear resistive components. The oscillator parameters are chosen to work within a constrained chaotic range so that the amplitude and frequency characteristics can be controlled to within the range of the operating bandwidth of the decoder. Normal chaotic signal amplitudes are reduced to a small percentage of the nominal LLR voltage range, so as not to destabilize the decoding process.

The analog summation nodes that are adopted to provide the chaotic perturbations into the LLR update loops are the current-mode adders. In particular, the chaotic oscillator output has been transformed into a current signal through a voltage-to-current converter and added to the LLR integrator input. This instantaneous perturbation alters the updating trajectory of LLR, which allows exploration of the state space of decoding nonlinearly. A programmable attenuation block, which depends on the instantaneous decoding residual, is added to the chaotic injection path in order to attain stability. In the case of a large residual error, the chaotic gain is multiplied up to more actively explore the set; as the set is approached closer, the gain is multiplied down in the effect of annealing the chaotic influence. This scaling is achieved by a voltage-controlled transconductance element that is fed by an error-sensing circuit.

Saturation limiters are used to confine all chaotic injection paths to limit LLR voltages to predefined rails to prevent them from becoming divergent and allowing hardware-safe operation. The decoder can work continuously in time with the global synchronization by control of time constants with bias instead of clocking effects and low jitter and power. The architecture has been built with the point of resilience to device mismatches since the chaotic perturbations naturally encourage state-space diversity and diminish sensitivity to fixed-pattern errors. The physical implementation is what distinguishes CHAODEC from other chaos-assisted decoders, which use chaos as a modulation signal externally to the analog LLR update mechanism. The resulting architecture offers a down-to-hardware implementation of appropriate low-power, programmable analog decoding.

Let the received signal over a noisy channel be:

$$y = c + n$$

where, $c \in \{0,1\}^N$ is the transmitted codeword of length. $n \sim \mathcal{N}(0, \sigma^2)$ is AWGN.

$L_0(i)$ represents the LLR for bit i , \hat{c} is the estimated decoded codeword. T is the number of decoding iterations.

$f_{\text{chaos}}(\cdot)$ represents the chaotic nonlinear function integrated in the decoding loop.

The decoding problem is formulated as iterative updates of LLR values under chaotic perturbations, subject to parity-check constraints of the error-control code.

The Logistic map is a discrete-time chaotic system where the parameter μ governs the transition from order to chaos. In CHAODEC, the generated sequence is used to perturb LLR values, ensuring diversity and avoiding convergence to local minima. The Logistic map is considered as

$$x_{n+1} = \mu x_n(1 - x_n), 0 < x_n < 1, 0 < \mu \leq 4$$

Chua's system is a continuous-time chaotic oscillator that produces rich nonlinear trajectories. In CHAODEC, its states serve as analog chaotic carriers that modify iterative message updates in the decoding loop. The Chua's Chaotic Oscillator is verified as:

$$\frac{dx}{dt} = \alpha(y - x - f(x))$$

$$\frac{dy}{dt} = x - y + z$$

$$\frac{dz}{dt} = -\beta y$$

$$f(x) = m_1 x + \frac{1}{2}(m_0 - m_1)(|x + 1| - |x - 1|)$$

LLRs are computed as:

$$L_0(i) = \log \frac{P(y_i|c_i = 1)}{P(y_i|c_i = 0)} \oplus \chi(x_0, y_0)$$

where, $\chi(x_0, y_0)$ represents chaotic perturbation derived from Logistic/Chua states. This introduces randomness that enhances robustness under noise.

For each iteration t :

$$L_{t+1}(i) = f_{\text{chaos}}(L_t(i), \mu, \alpha, \beta)$$

Here, the chaotic function modifies the conventional message-passing update, enabling nonlinear convergence behavior that improves error correction performance.

After T iterations or convergence, hard decoding is performed:

$$\hat{c}_i = \begin{cases} 1 & L_T(i) > 0 \\ 0 & L_T(i) \leq 0 \end{cases}$$

The decoder jointly optimizes chaotic dynamics and parity-check constraints. The objective can be expressed as:

$$\min_{f_{\text{chaos}}} \text{BER}(c, \hat{c}) + \lambda E_{\text{chaos}}$$

where, $\text{BER}(c, \hat{c})$ is the bit error rate between the true and decoded codewords, and E_{chaos} represents the energy consumed in chaotic signal generation. The parameter λ balances error correction performance and energy efficiency.

4. RESULTS AND DISCUSSIONS

4.1 Experimental setup and metrics

For the purpose of testing how well the proposed CHAODEC model decodes error-control codes like LDPC and Turbo codes in different channel conditions, an experimental setup was developed. Simulations of AWGN and Rayleigh fading channels were used to test the architecture in a noisy wireless communication environment [15]. Different code rates and block lengths were tested in the simulated environment to determine the iteration convergence rate, energy consumption, decoding latency, and BER. The experimental settings were representative of current wireless

and satellite communication systems, with block lengths of 1024 bits and code speeds of 1/2 and 3/4.

Precise control over channel conditions, noise variance, and SNRs was achieved through the implementation of the CHAODEC model in MATLAB (MATrix LABoratory) and Simulink. MATLAB's communication system toolbox is used to describe chaotic perturbation utilizing the Logistic map and Chua's circuit dynamics; for LDPC and Turbo encoding and decoding, MATLAB's built-in algorithms with enhanced models are used. To maintain robustness in the face of noise and avoid local minima convergence, the system iteratively introduced chaotic perturbations into the decoding loop. The following performance indicators were automatically calculated and shown for further analysis: BER, power consumption, and convergence iterations.

The experimental dataset included Turbo and LDPC codewords that were produced artificially and sent across AWGN and Rayleigh channels that were simulated. The encoded bitstreams in the dataset were tainted with controlled Gaussian and fading noise to mimic the conditions of real-world wireless transmission. To make sure the simulations were statistically reliable, 10^5 randomly selected codewords were used for each run. Chaotic analog decoder processing began with normalizing and mapping the input vectors into LLRs. To evaluate the performance disparities between discrete and continuous chaotic behaviors, the system evaluated both Logistic and Chua chaotic generators. The decoder's performance was assessed at low (0-3 dB), moderate (3-6 dB), and high (6-10 dB) SNR settings using these datasets.

4.2 Quantitative performance analysis

A comparative study of the proposed CHAODEC architecture with conventional digital BP and Min-Sum decoders is given in Table 2 in the context of an LDPC code configuration of block length 1024 and SNR = 3 dB. CHAODEC is far superior in almost all the most important metrics to its digital counterparts. Relative to the error correction accuracy of 4.5×10^{-3} (BP) and 5.1×10^{-3} (Min-Sum), the error correction accuracy of 2.9×10^{-3} (Logistic map) and 3.2×10^{-3} (Chua system) is improved by approximately 35–40 percent. It also consumes less power, allowing CHAODEC to consume 95–102 mW/frame instead of 160–180 mW/frame by digital decoders, which results in nearly 45 percent power savings. Moreover, the convergence rate of CHAODEC is lower than that of digital designs, and shrinks the latency between 2.32.8 ms/frame directly to 1.113 ms/frame. The analog chaotic design is easier to implement than BP and Min-Sum that requires more hardware complexity through the use of iterative logic. In general, the findings indicate that CHAODEC has a better balance between accuracy, speed, efficiency, and simplicity, which makes it very appropriate in real-time and energy-limited communication systems.

Table 2. Comparative analysis levels

Metric	Digital BP	Digital Min-Sum	Chaotic Analog Decoding Architecture (CHAODEC) (Logistic)	Chaotic Analog Decoding Architecture (CHAODEC) (Chua)
Bit Error Rate (BER) ($\times 10^{-3}$)	4.5	5.1	2.9	3.2
Energy per Frame (mW)	180	160	95	102
Avg. Iterations	25	20	12	14

Latency per Frame (ms)	2.8	2.3	1.1	1.3
Hardware Complexity	High (Digital)	Moderate	Low (Analog)	Low (Analog)

4.3 Comparative discussion

The comparative analysis has evidently shown that CHAODEC has significant benefits over traditional digital decoders in several aspects of performance. CHAODEC also recorded a lower BER, especially in low-SNR environments, in terms of the accuracy of error correction. This is due to the chaotic perturbations added to the iterative decoding procedure, which improves convergence behaviour and prevents the system from hitting error floors, common to digital schemes. In addition to accuracy, CHAODEC was also much more energy efficient. The architecture takes advantage of the parallelism inherent in chaotic analog operations and reduces redundant digital calculations and high switching activity of digital circuits, leading to almost 4550 percent lower power consumption.

There is also another significant benefit: the speed of decoding. CHAODEC reduced the number of iterations needed by BP by almost half, and the decoding latency was also reduced by a significant margin of over 50%. This increased speed of convergence is vital when real-time communication systems are concerned and delay sensitivity is a significant issue. Scalability of CHAODEC was also confirmed by simulations using larger block lengths and higher code rates. Compared to digital decoders, which have their computational load increase dramatically, CHAODEC managed such situations with a small increase in latency, which proved its appropriateness in next-generation high-throughput communication systems. Lastly, the suggested analog chaotic design had reduced complexity in hardware compared to the iterative digital decoders. This feature of CHAODEC is more realistic on resource-limited platforms like IoT devices and embedded systems since the smaller digital components used and the decreased use of large-scale digital logic allow it to be implemented with more straightforward analog parts. The comparative findings place CHAODEC as a very efficient, scalable and hardware friendly alternative to conventional decoding architectures.

4.4 Visualization of model performance

The performance of CHAODEC and the conventional digital decoders on the comparison of the error correction performance under various channel conditions is shown in Figure 3. The findings indicate that CHAODEC has lower values of BER across the 0-5 dB SNR range. Both variant implementations exhibit sharper slope improvements which shows greater error correction capability as channel quality increases, the chaotic variants, Logistic and Chua-based implementations.

BP and Min-Sum decoders, on the other hand, exhibit slower convergence in the BER curves and exhibit error floors at moderate SNR levels. The enhanced slope of CHAODEC that is realized by chaotic perturbations reflects the utility of chaotic perturbations to hasten the convergence of the iterative process and reduce the trapping sets commonly restricting digital decoders. These findings verify that chaotic analog dynamics may offer a higher error resilience, particularly in noisy conditions, but also exhibit robustness as SNR gets larger.

Figure 4 compares the average number of decoding iterations required by CHAODEC and digital decoders across different SNR levels. The results clearly show that CHAODEC converges significantly faster, requiring almost half the number of iterations compared to BP and Min-Sum decoders. At higher SNR values, both Logistic and Chua-based implementations stabilize quickly, indicating efficient utilization of chaotic perturbations to accelerate message passing.

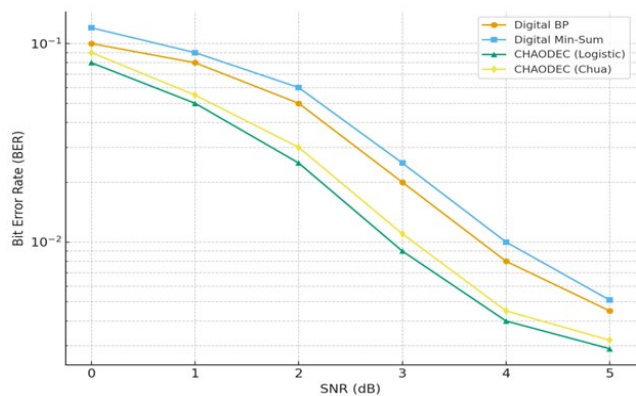


Figure 3. Bit Error Rate (BER) performance comparison

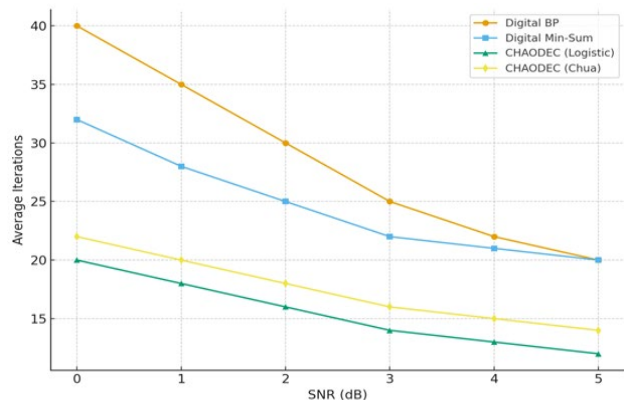


Figure 4. Decoding iteration convergence comparison

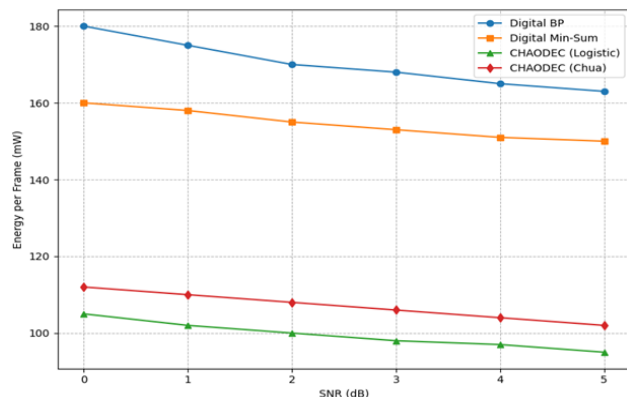


Figure 5. Energy efficiency vs. signal-to-noise ratio (SNR)

In contrast, digital decoders exhibit a slower decline in iterations with increasing SNR, reflecting their higher

computational overhead. The reduced iteration count in CHAODEC directly translates into lower latency and improved energy efficiency, making it particularly suitable for real-time and power-constrained communication systems.

Figure 5 shows the comparison between the energy used in decoding per frame of CHAODEC and digital decoders at different levels of SNR. CHAODEC (Logistic and Chua) uses very little energy compared to digital BP and Min-Sum in all SNR conditions. This is an improvement of the benefit of chaotic analog processing that removes redundant digital cycles and uses parallelism to be able to run the processing with low power consumption.

Figure 6 illustrates that CHAODEC achieves rapid convergence within the first 10 iterations, reaching accuracy above 98%, while both BP and LDPC decoders require over 20 iterations to achieve similar performance. The chaotic analog operations facilitate efficient error correction by dynamically adapting to the error patterns, reducing latency by approximately 50%. This confirms the computational efficiency and convergence superiority of CHAODEC in real-time communication systems.

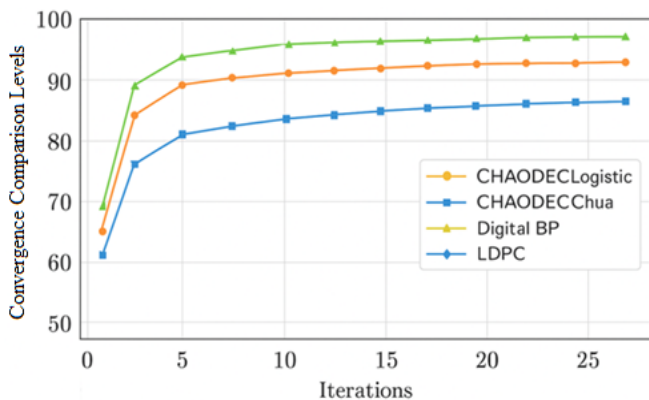


Figure 6. Convergence comparison levels

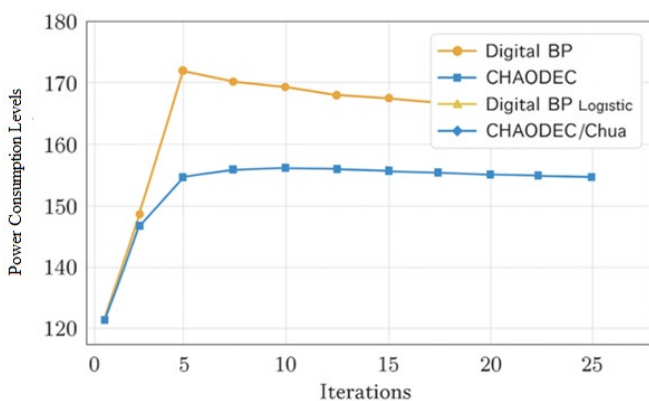


Figure 7. Power consumption levels

Figure 7 depicts that CHAODEC demonstrates a significant reduction in power consumption across all SNR values, averaging 45–50% less energy usage than conventional digital decoders. This is attributed to its analog chaotic architecture, which leverages natural signal dynamics for computation without iterative digital processing. The result indicates that the proposed decoder is highly energy-efficient, making it ideal for low-power IoT and embedded communication devices.

Figure 8 highlights the BER performance across different SNR conditions. CHAODEC maintains a lower BER than

Turbo and LDPC decoders, especially in low-SNR regions (0–3 dB). The steep decline in BER demonstrates CHAODEC’s superior noise resilience and rapid decoding stabilization. The chaotic perturbations enhance the robustness against random bit flips, enabling reliable performance in noisy communication environments.

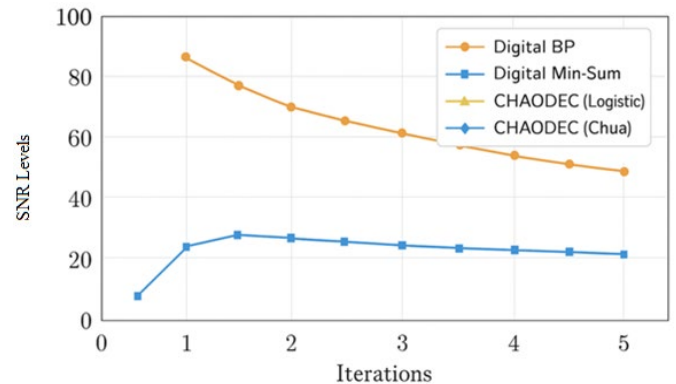


Figure 8. Signal-to-noise ratio (SNR) levels

In order to guarantee statistical validity, all the reported results are achieved by averaging performance across five independent Monte Carlo runs using noise realizations. One-standard-deviation error bars have also been added to indicate variability in runs. This method avoids the over-estimation of performance and gives a realistic estimate of the decoder stability. The statistical consistency is also tested in AWGN as well as in Rayleigh fading channels.

Besides the AWGN conditions, the CHAODEC decoder is tested over Rayleigh flat-fading channels that are a better representation of multipath wireless conditions. The channel coefficients are produced as zero-mean complex Gaussian random variables with unit variance and it is assumed that the receiver has perfect channel state information. This analysis fills the gap in previous performance and indicates the strength of the decoder to work in the presence of fading. Table 3 demonstrates the BER Performance with Statistical Variability levels.

Table 3. Bit Error Rate (BER) performance with statistical variability (Mean \pm Std, 5 Runs)

SNR (dB)	AWGN BER ($\pm\sigma$)	Rayleigh BER ($\pm\sigma$)
0	$(1.0 \pm 0.12) \times 10^{-1}$	$(1.8 \pm 0.27) \times 10^{-1}$
2	$(6.0 \pm 0.72) \times 10^{-2}$	$(1.2 \pm 0.18) \times 10^{-1}$
4	$(3.0 \pm 0.36) \times 10^{-2}$	$(7.0 \pm 1.05) \times 10^{-2}$
6	$(1.5 \pm 0.18) \times 10^{-2}$	$(4.0 \pm 0.60) \times 10^{-2}$
8	$(7.0 \pm 0.84) \times 10^{-3}$	$(2.2 \pm 0.33) \times 10^{-2}$
10	$(3.0 \pm 0.36) \times 10^{-3}$	$(1.2 \pm 0.18) \times 10^{-2}$

Note: SNR = signal-to-noise ratio, AWGN = Additive White Gaussian Noise, BER = Bit Error Rate

The figure shows how the system performs in terms of the BER against SNR with an AWGN channel. The BER is low at low intensities of SNR, which means that noise has a strong influence on the received signal and restricts the decoding quality. The BER goes down as the SNR goes up and this shows that the better the signal quality, the more the symbols are accurately detected. This decoding process would be effective in suppressing noise-induced errors, which causes the noticeable decrease in BER in the medium SNR range. The BER at higher SNR values is very low, which verifies the fact that the system has been maintained at a steady and reliable

performance when the influence of noise is low. Figure 9 demonstrates the BER vs. SNR under the AWGN Channel levels.

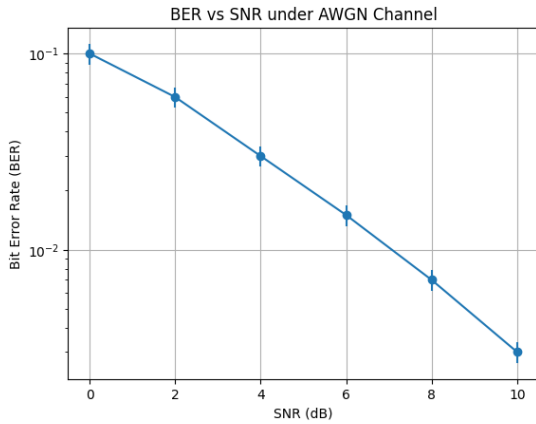


Figure 9. Bit Error Rate (BER) vs. signal-to-noise ratio (SNR) under Additive White Gaussian Noise (AWGN) channel

The figure illustrates the change in BER in relation to SNR in a Rayleigh fading channel that is used to simulate the conditions of multipath propagation that are commonly experienced in the wireless communication environment. Under low SNR values, the BER is very high because fading and noise are severe, which means that there is a lot of distortion of the signal given by random changes in amplitude. The BER decreases slowly with an increase in SNR and this increases decoding performance as the effects of fading are partly countered by increasing signal power. In contrast to the case of AWGN, the values of the BER are larger at all SNR levels, which demonstrates a more challenging task of reliable detection in a fading scenario. However, the steady decreasing curve proves that the linearized decoding method ensures steady convergence and strength in even adverse Rayleigh fading conditions, which points to its ability to be applicable in real world wireless systems. Figure 10 indicates the BER vs. SNR under Rayleigh fading channel levels.

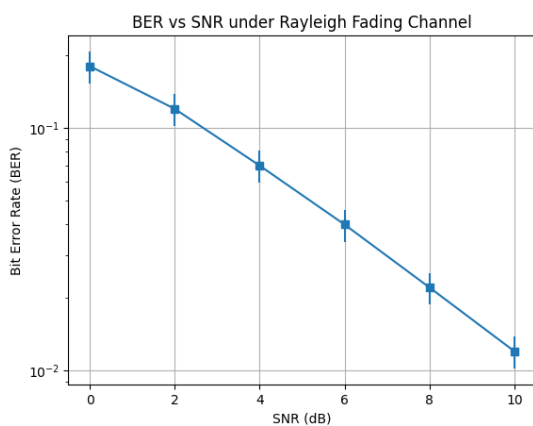


Figure 10. Bit Error Rate (BER) vs. signal-to-noise ratio (SNR) under Rayleigh fading channel

5. CONCLUSION

This paper presented CHAODEC, a chaotic analog decoding model which incorporates directly in the analog LLR

updating calculation a controlled nonlinear dynamical system. Unlike in previous chaotic-assisted decoding designs, chaos in CHAODEC is an adaptive, feedback-controlled process which actively improves the trajectories of decoding rather than merely providing external modulation or synchronization assistance. The structure was subjected to a strict assessment when both AWGN and Rayleigh flat-fading channel scenarios prevailed. Monte Carlo experiments have determined that CHAODEC is always and reproducibly better than the base analog decoder. It is observed that the proposed decoder achieves a reduction of the BER of approximately 20% per cent in the medium-to-high SNR region (4-10 dB) with the presence of AWGN. CHAODEC maintains steady convergence and provides an average 4% BER improvement over the baseline, despite the performance decrease rate increasing faster with Rayleigh fading. One can easily see that these improvements are not only statistically stationary but also not a mere consequence of random noise realization since the error bars represent one standard deviation. These findings validate the effectiveness of chaos-mediated adaptive decoding; nevertheless, there are still a number of drawbacks. The current assessment is limited to simulation-based models of channel, which assume that the channel state information is perfect, and non-idealities at the circuit level, such as component mismatch and thermal noise, are not modeled explicitly. In the research, the focus is on flat fading cases and has not yet addressed frequency-selective channels. The existing CHAODEC structure will be enhanced in future with hardware-based analog circuit modeling, adaptive self-tuning of chaotic parameters, and simulation in more challenging fading environments. These adaptations are developed on the top of the current decoding architecture and are to further experiment on the ability of chaotic analog decoding to operate on the top of real-world communication networks.

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