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Comprehensive Analysis of Sliding Mode Control for Multicell Converter-Based STATCOM Used in Power Distribution Systems

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ABSTRACT

The present article focuses on the effectiveness of the synchronous static compensator (STATCOM) based on a seven-level multi-cell converter (in Flying capacitor series or stacked), with sliding mode control, for reactive power compensation, power factor correction, and elimination of voltage dips and surges in distribution networks. The utilization of multi-cell converters confers several advantages, including the capacity to augment the number of output voltage levels, mitigate voltage stresses on the power switches, and enhance the harmonic content of the output voltage. This, in turn, facilitates the generation of high-quality waveforms. Furthermore, the sliding mode control method, which has gained renown for its speed and robustness, serves to enhance the dynamic performance of the distribution network. The STATCOM model with the proposed control was simulated under the MATLAB/Simulink environment for a range of case studies. The simulation results obtained demonstrate the capability of the proposed control system to stabilize the voltage at the Point of Common Coupling (PCC). Furthermore, the system has been shown to compensate for reactive energy and enhance the power factor by acting on the reactive energy it supplies or absorbs.

1. INTRODUCTION

In the contemporary context of electrical power distribution and transmission networks, a multitude of power quality issues have been identified, including but not limited to low power factor, voltage dips and surges, harmonic distortion, unbalanced voltages, reactive and active power control, and optimal power flow. These issues are attributed to various factors, such as non-linear loads, unbalanced loads, internal faults, and external disturbances [1, 2]. In the face of mounting demand for power transmission capacity, the construction of new transmission lines has been identified as a potential solution. Nevertheless, this solution is frequently impractical and economically unviable [3]. Furthermore, conventional control methodologies, such as electromechanical devices (e.g. choke coils, circuit-breaker switched capacitors or phase-shifting transformers), have been employed. However, conventional solutions have been shown to become inefficient and too slow to respond adequately to the rapid disturbances occurring in power systems [4].

In order to respond effectively to the challenges posed by reactive power flows and dynamic disturbances in electricity networks, flexible alternating current transmission systems (FACTS) have been developed. These devices facilitate the flexible and rapid management of network parameters, thereby enhancing stability, transmission capacity, and the quality of the power supply. These static devices, which are based on power electronics, are designed to provide effective control of power flow in electricity networks. The primary function of these components is to ensure that voltage remains within the authorized limits. They also serve to minimize energy losses and enhance the transfer capacity of existing transmission lines. Furthermore, they make a significant contribution to supporting network stability and maintaining normal operation [5, 6].

FACTS systems can connect to the network in a series, shunt, or combined series-series or series-shunt configuration. The nature of their connection dictates the behavior of these system components. In the case of a parallel connection, they act as current sources, whereas in a series connection, they function as voltage sources. In a passive state, these systems exchange solely reactive energy with the network, thereby assuming behavior akin to impedances [3, 6-8]. Conversely, during periods of activity, these devices have the capacity to exchange both active and reactive energy with the network [6, 7]. Depending on the power component used, FACTS systems are classified into two generations according to their technological characteristics. The first generation is based on the use of Thyristor converters, such as the Static Var Compensator (SVC), the Thyristor Controlled Series Compensator (TCSC), the Thyristor Controlled Series Reactor (TCSR) and the TSSC. The second generation employs voltage source converters (VSCs), incorporating more sophisticated devices such as the Unified Power Flow Controller (UPFC), the

Static Synchronous Compensator (STATCOM) and the Synchronous Series Static Compensator (SSSC) [2, 9, 10]. It is evident that among the most widely utilized FACTS compensators, the STATCOM equipped with a voltage source converter is held in high esteem by researchers on account of its considerable flexibility and ease of control [10]. In modern power systems, reactive power compensation enhances voltage support and improves power factor [11]. In recent years, multilevel converters have increasingly replaced conventional two-level STATCOM converters [12].

These multilevel STATCOMs are widely adopted due to their significant advantages, including a substantial reduction in output voltage THD (Total Harmonic Distortion), increased efficiency, and improved power quality.

Multilevel STATCOMs are widely adopted because they offer significant advantages, such as reduction of output voltage THD, higher efficiency, improved power quality, lower converter losses, and decreased electromagnetic interference resulting from reduced dv/dt in the system [13].

In the context of STATCOM applications, two fundamental topologies of multilevel converters are predominantly employed: the Neutral Point Clamped converter (NPC) topology and the Cascaded H-Bridge (CHB) [14]. However, as the number of voltage levels increases, these topologies necessitate the use of a greater number of capacitors and power elements. Multi-level NPC converters necessitate a substantial quantity of clamping diodes and intricate control mechanisms to regulate the voltage of the DC link capacitors. In a similar manner, CHB converters necessitate isolated transformer windings, a feature which complicates the process of energy recovery [15]. In addition to the two classic multilevel converter topologies, other classic multilevel structures, such as the series multi-cell converter with floating capacitors, present many interesting properties for STATCOM applications. These include their ability to operate without a transformer, reduce voltage stresses on power components and the ability to naturally maintain floating capacitor voltages at their target operating levels [16]. Another option that merits consideration is the stacked multicell converter (SMC). The stacked multicell topology (SMC) was proposed in 2001 [17].

This converter is an improved version of the series multicellular converter, characterized by multiple cells and stages. Its topology enables the generation of numerous voltage levels across several switches, reducing both capacitor nominal voltage and switches [18, 19]. The lower energy stored in the capacitors allows the use of smaller, lower-power devices, thereby reducing costs and space requirements. Moreover, this topology increases the number of possible combinations required to achieve a given voltage level, thus introducing beneficial redundancy [20].

The employment of forced-switching static converters necessitates the utilisation of sophisticated control methodologies to enhance their performance across diverse operating modes. In this context, a robust non-linear control technique based on the sliding mode method is proposed. This technique ensures that the control system performs optimally in terms of stability and reference tracking, despite uncertainties in the parameters and environmental disturbances [21]. The model delineates two distinct phases: the approach phase and the slip phase [22]. The sliding mode control theory postulates the delineation of an imaginary slip surface, along which error signals are compelled to evolve, thereby ensuring that the system dynamics or state trajectories adhere to the stipulated references [21]. Moreover, it has been demonstrated that the system's simplified structure renders it a suitable replacement for the conventional proportional integral (PI) controller. The determination of PI controller gains becomes redundant, harmonics are reduced, and the system demonstrates robustness to large load variations.

In this paper, a sliding mode control for a seven-level STATCOM is proposed. This control is based on a multi-cell converter (Flying capacitor series or stacked) and is designed to compensate for disturbances (voltage dips, overvoltage and load variation) in a distribution network. The control method under discussion facilitates the provision or absorption of reactive power by STATCOM. This, in turn, ensures the stabilization of the voltage profile at the Point of Common Coupling (PCC). This process serves to mitigate fluctuations between the source-side voltage and the load-side voltage, with the objective of attaining a power factor that approximates unity. A series of simulation studies was conducted utilizing the MATLAB/Simulink platform. The outcomes of these studies are presented herein in order to validate the proposed topology and the associated control method.

2. SYSTEM DESCRIPTION

2.1 System configuration

The system under scrutiny is depicted by the equivalent circuit in Figure 1. The circuit under consideration consists of a three-phase voltage source, developed and built to simulate two types of voltage disturbance (dips and surges) at the PCC, linear loads or non-linear loads, and a multi-cell STATCOM compensator. The compensator is constituted by a multi-cell converter (Flying capacitor series or stacked) connected to the mains using a three-phase inductor with an internal resistor, and high-capacity capacitors connected to the DC link.

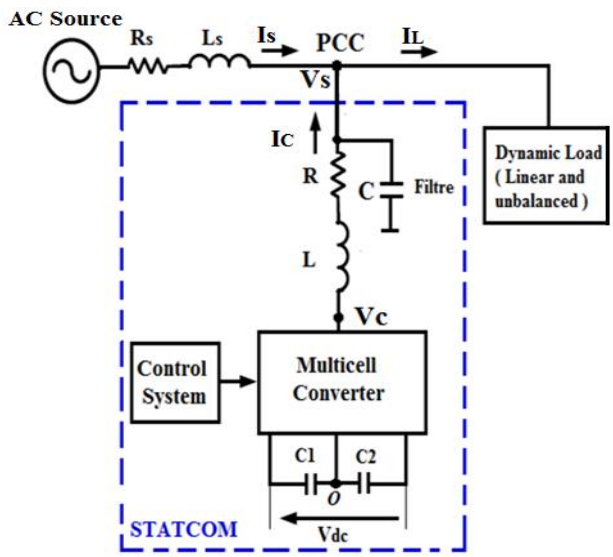


Figure 1. The schematic structure of a STATCOM with a multicell converter

The STATCOM regulates the voltage at the PCC by injecting reactive power. The amplitude of the converter's

output voltage is synchronized with the network voltage control this exchange. When the voltage difference becomes zero, no current flows through the inductor, and thus no reactive power is exchanged. In instances where this value is less than Vs, the STATCOM functions in an inductive manner, thereby absorbing reactive power from the mains. Conversely, if the voltage exceeds the threshold, the inverter transitions into capacitive mode, thereby injecting reactive power into the network [23, 24].

2.2 Mathematical model of STATCOM

Figure 1 shows the schematic circuit of the STATCOM with the multicell converter.

In this power system, V_{sabc}, V_{cabc} and I_{cabc} represent, respectively, the three-phase network voltages at the PCC, the three-phase voltages at the converter output, and the three-phase output currents of the STATCOM. Additionally, L is the coupling filter inductance of each arm, and R is the resistance in series with the sum of the coupling filter winding's resistance losses and the conduction losses of the converter.

The instantaneous voltage per phase at the PCC is given by:

$$V_{sa} = V_M \cos(\omega t) \tag{1}$$

$$V_{sb} = V_M \cos(\omega t - 2\pi/3) \tag{2}$$

$$V_{sc} = V_M \cos(\omega t - 4\pi/3) \tag{3}$$

According to Kirchhoff's law of voltages, the relationship between the voltage at the PCC, the converter output voltage, and the currents is as follows [3, 24, 25]:

$$V_{sabc} = V_{cabc} + RI_{cabc} + L\frac{dI_{cabc}}{dt} \tag{4}$$

Using the Park transformation (abc-dq), Eq. (4) can be rewritten as follows:

$$V_d = V_{cd} + RI_d + L\frac{dI_d}{dt} - L\omega I_q \tag{5}$$

$$V_q = V_{cq} + RI_q + L\frac{dI_q}{dt} + L\omega I_d \tag{6}$$

where, I_d and I_q the d- and q-axis currents corresponding to I_{ca}, I_{cb} and I_{cc}; ω is the synchronized angular velocity of rotation of the voltage vector; V_d and V_q represent the d- and q-axis voltages corresponding to V_{sa}, V_{sb} and V_{sc}.

According to the instantaneous power theory, the active and reactive power exchanged between the network and the STATCOM can be calculated in the d-q reference frame as follows:

$$P = \frac{3}{2}\left(V_d I_d + V_q I_q\right) \tag{7}$$

$$Q = \frac{3}{2}\left(V_q I_d - V_d I_q\right) \tag{8}$$

In the synchronized rotary reference frame, $V_s = V_d$ and $V_q = 0$, the instantaneous active and reactive powers can be written as follows:

$$P = \frac{3}{2}V_d I_d \tag{9}$$

$$Q = -\frac{3}{2}V_d I_q \tag{10}$$

2.3 Multicell converters model

2.3.1 Flying capacitor multicell converter model

The Flying capacitor multicell structure is made up of a series of complementary switches, known as cells, with floating voltage sources between them, using capacitors. Each phase consists of p switching cells, separated from each other by $(p-1)$ floating capacitors.

Each cell has two bidirectional switches (an Insulated Gate Bipolar Transistor (IGBT) with an antiparallel diode), controlled in a complementary manner to avoid short-circuiting the voltage sources. There are $(p+1)$ voltage levels available at the output of each arm, depending on the binary states of each cell [26-29].

The binary state S_{ki} of the switching cell i (i =1, 2, 3, ...p) of arm k (k = a, b, c) corresponds to the state of the top switch in the cell: 1 for the closed state, 0 for the open state.

The output voltage of the inverter can be expressed as a function of the control commands S_{ki}:

$$V_{kO} = \frac{V_{dc}}{p}\left(\sum_{i=1}^{p} S_{ki} - \frac{p}{2}\right) \tag{11}$$

At steady state, the cell voltages are equal:

$$V_{Cellki} = V_{dc}/p \tag{12}$$

This condition holds when the voltage across each cell's floating capacitors satisfies the following equation:

$$V_{Cki} = \frac{i \times V_{dc}}{p} \tag{13}$$

With p switching cells, the serial multistage converter generates a number of output levels N such that:

$$N = p + 1 \tag{14}$$

Table 1 presents the per-phase characteristic quantities of the p switching cells.

Table 1. Definition of the per-phase characteristic parameters of the Flying Capacitor Multicell Converter (FCMC)

Number of associated cells	p
Number of associated capacitors	$p-1$
Number of possible states	2^p
Number of output voltage levels	$p+1$
Main supply voltage value	V_{dc}
Cell voltage source value *i*	$(i \times V_{dc})/p$

In the special case where $p = 6$ cells, this converter is called a seven-level multicell series converter. Figure 2 shows the structure of one arm of this converter, made up of twelve switches forming six series switching cells and five

floating capacitors. The input DC bus includes two capacitors (C1 and C2) connected in series, form a midpoint denoted as (O).

The output voltages of the converter measured with respect to the neutral point (O) of the DC bus, can be expressed by the following equation [29]:

$$V_{kO} = (S_{k6} - 0.5) \times V_{dc} + (S_{k5} - S_{k6}) \times V_{ck5} + (S_{k4} - S_{k5}) \times V_{Ck4} + (S_{k3} - S_{k4}) \times V_{ck3} + (S_{k2} - S_{k3}) \times V_{ck2} + (S_{k1} - S_{k2}) \times V_{ck1} \quad (15)$$

For a balanced three-phase system, the sum of the three phase voltages is zero;

$$V_{ca} + V_{cb} + V_{cc} = 0 \quad (16)$$

The relationship between the voltages V_{ck} and V_{kO} is given by Eq. (17):

$$V_{ck} = V_{kO} - V_{nO} \quad (17)$$

$$\text{Avec: } V_{nO} = (V_{aO} + V_{bO} + V_{cO})/3 \quad (18)$$

From Eq. (17), we express V_{ca}, V_{cb} and V_{cc} as a function of V_{aO}, V_{bO} and V_{cO}:

$$\begin{bmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \times \begin{bmatrix} V_{aO} \\ V_{bO} \\ V_{cO} \end{bmatrix} \quad (19)$$

where, V_{aO}, V_{bO} and V_{cO} determined by Eq. (15).

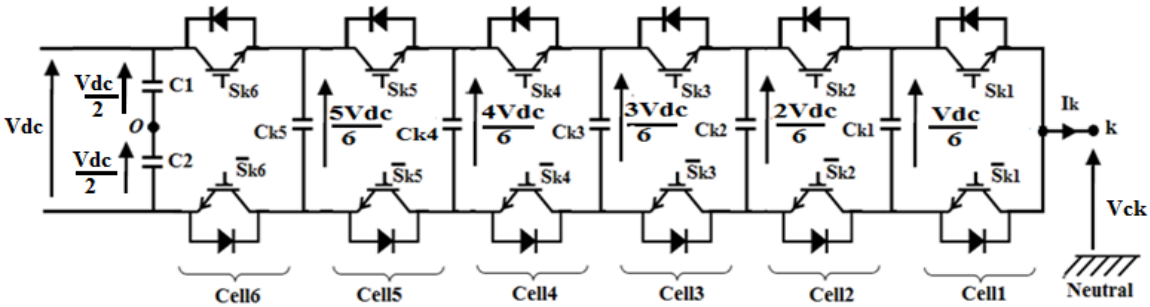


Figure 2. Configuration of seven-level flying capacitor multicell converter

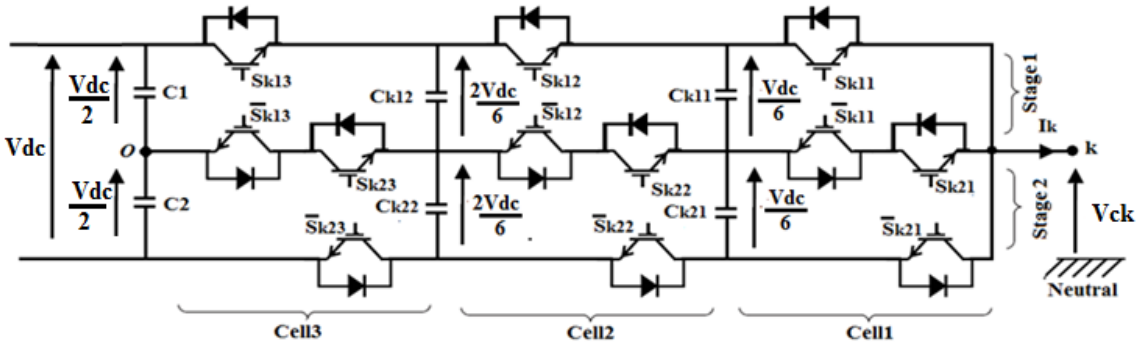


Figure 3. Configuration of seven-level SMC

2.3.2 SMC model

The SMC is a hybrid association of elementary switching cells [15, 18, 30-31]. The $(p \times n + 1)$ level $SMC\ p \times n$ converter is composed of $(2 \times p \times n)$ bidirectional switches (IGBT, with an antiparallel diode) forming p cells and n stages, i.e., n × p nested switching cells and $(p - 1) \times n$ floating capacitors. Each switching cell consists of two pairs of switching transistors S_{kij} and $\bar{S}_{kij}$, where the subscript $k = a, b, c$ is used for phase identification, and i, j designate the number of the switch corresponding to a particular cell, with $i = 1,2,3$ for the cell and $j = 1,2$ for the stage.

Switch control functions can take two values $S_{kij} = 1$; $S_{kij} = 0$, where 0 and 1 correspond to the switch being off and on respectively. The pairs of switches in each phase arm operate in a complementary manner.

Each voltage across these floating capacitors is then equal to:

$$V_{Ckij} = \frac{i \times V_{dc}}{n \times p} \quad (20)$$

With V_{dc} the input voltage of the converter.

The previous method can be generalized to a $SMC\ p \times n$ converter. The characteristic quantities per phase of this converter are defined in Table 2.

Table 2. Definition of the per-phase characteristic parameters of the SMC $p \times n$

Number of associated cells	p
Number of associated stages	n
Number of associated capacitors	$(p - 1) \times n$
Number of possible states	$(n + 1)^p$
Number of output voltage levels	$(p \times n) + 1$
Value of main supply voltage	V_{dc}
Value of cell voltage source *i*	$(i \times V_{dc})/(n \times p)$

In the special case where $p = 3$ cells and $n = 2$ stages.

This converter is called $C\ 3 \times 2$. Figure 3 shows the structure of one arm of the seven-stage $SMC\ 3 \times 2$ converter. It consists of eleven switches forming six nested switching cells and four floating capacitors. The upper and lower floating capacitors in each phase C_{k11}, $C_{k12,}$ C_{k21} and C_{k22}, as well as the DC bus capacitors C1 and C2, play an essential role in this system. The input DC bus is composed of two capacitors (C1 and C2) connected in series, forming a midpoint referred to as (O).

The output voltages of the converter, measured with respect to the neutral point (O) of the DC bus, are estimated using the following equation [18]:

$$\begin{aligned} V_{kO} &= (S_{k11} - S_{k12}) \times V_{Ck11} + S_{k13} \times (V_{dc}/2) \\ &+(S_{k12} - S_{k13}) \times V_{Ck12} + (S_{k21} - S_{k22}) \times V_{Ck21} \\ &+(S_{k22} - S_{k23}) \times V_{Ck22} - (1 - S_{k23}) \times (V_{dc}/2) \end{aligned} \quad (21)$$

The relationship of the converter output voltages V_{ck}, (k=a, b, c), to the voltages V_{kO} given by Eq. (19).

3. STATCOM CONTROL STRATEGY

The overall block diagram of the STATCOM control strategy using the sliding mode approach is shown in Figure 4 [32, 33]. The synchronous dq frame transformation is used to convert time-varying voltage and current parameters into continuous quantities. To determine the phase of the grid voltage (θ), a Phase Locked Loop (PLL) is used. This simplifies the implementation of conventional proportional-integrator (PI) controllers. The overall control consists of three parts: dq reference current generation, internal current control and Pulse-Width Modulation (PWM) generator. In the first part, through Park transformation, the output compensation currents I_{cabc} are converted into two components: the active component I_d and the reactive component I_q. Similarly, through Park transformation, the grid voltage at the PCC V_{sabc} is converted into V_d and V_q. The variable V_{rms} represents the measured magnitude of the AC voltage at the PCC, calculated from the V_d and V_q components of the three-phase voltage vector, as $V_{rms} = \sqrt{V_d^2 + V_q^2}$.

The error signal between the measured root mean square (RMS) value of the AC voltage V_{rms} and the reference value of the RMS AC voltage V_{rmsref} is transmitted to a PI regulator, which generates a reference current I_{qref}. Similarly, the DC bus reference voltage V_{dcref}, is compared with the measured DC side voltage V_{dc}, and the resulting error is passed to the PI controller to generate the reference current I_{dref} [22, 25, 32, 33].

The second part, namely the internal current loop, takes the phase voltages, phase currents, and DC bus voltage as input to generate the reference voltage values using sliding mode control.

The configuration of sliding mode control encompasses two distinct phases. Primarily, the establishment of a sliding surface is requisite, subsequently accompanied by the determination of an opposite control law based on the system's dynamic equations. The process commences from an imposed initial condition, follows the state trajectory towards the sliding surface, and then asymptotically tends towards an equilibrium point.

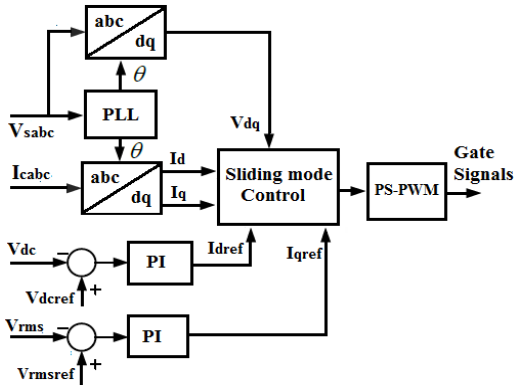


Figure 4. Block diagram of the control system for the multicell converter-based STATCOM

In the control strategy, STATCOM is driven using sliding mode control to regulate the STATCOM currents (I_d and I_q) [22, 34].

The following equation is to be considered:

$$V_d = V_{cd} + RI_d + L\frac{dI_d}{dt} - \omega LI_q \quad (22)$$

$$V_q = V_{cq} + RI_q + L\frac{dI_q}{dt} + \omega LI_d \quad (23)$$

The equations of state (24) and (25) are expressed as follows:

$$\frac{dI_d}{dt} = -\frac{R}{L}I_d - \frac{1}{L}V_{cd} + \omega I_q + \frac{1}{L}V_d \quad (24)$$

$$\frac{dI_q}{dt} = -\frac{R}{L}I_q - \frac{1}{L}V_{cq} - \omega I_d + \frac{1}{L}V_q \quad (25)$$

With:

$$V_d = V_{d\_eq} + V_{dcr} \quad (26)$$

$$V_q = V_{q\_eq} + V_{qcr} \quad (27)$$

The implementation of sliding mode control is initiated by the selection of sliding surfaces:

$$S_d = I_{dref} - I_d \quad (28)$$

$$S_q = I_{qref} - I_q \quad (29)$$

After derivation, we obtain:

$$\begin{aligned} \dot{S}_d = \dot{I}_{dref} - \dot{I}_d = \dot{I}_{dref} + \frac{R}{L}I_d \\ -\omega I_q + \frac{1}{L}V_{cd} - \frac{1}{L}V_d \end{aligned} \quad (30)$$

$$\dot{S}_q = \dot{I}_{qref} - \dot{I}_q = \dot{I}_{qref} + \frac{R}{L}I_q + \omega I_d + \frac{1}{L}V_{cq} - \frac{1}{L}V_q \quad (31)$$

And to check Lyapunov stability criterion $\dot{S}_i \times S_i$<0 we must have:

$$\dot{S}_d = -k_d \times sign(S_d) \quad (32)$$

$$\dot{S}_q = -k_q \times sign(S_q) \quad (33)$$

where, k_d, k_q are design parameters chosen according to the desired performance in closed loop.

$$\dot{I}_{dref} + \frac{R}{L} I_d - \omega I_q + \frac{1}{L} V_{cd} - \frac{1}{L} V_d = -k_d \times sign(S_d) \quad (34)$$

$$\dot{I}_{qref} + \frac{R}{L} I_q + \omega I_d + \frac{1}{L} V_{cq} - \frac{1}{L} V_q = -k_q \times sign(S_q) \quad (35)$$

This gives us the following expression for the V_d and V_q commands:

$$L\dot{I}_{dref} + RI_d - \omega LI_q + V_{cd} + L \times k_d \times sign(S_d) = V_d = V_{d\_eq} + V_{dcr} \quad (36)$$

$$L\dot{I}_{qref} + RI_q + \omega LI_d + V_{cq} + L \times k_q \times sign(S_q) = V_q = V_{q\_eq} + V_{qcr} \quad (37)$$

We obtain the following order and correction terms:

- Equivalent commands terms

$$V_{d\_eq} = L\dot{I}_{dref} + RI_d - \omega LI_q + V_{cd} \quad (38)$$

$$V_{q\_eq} = L\dot{I}_{qref} + RI_q + \omega LI_d + V_{cq} \quad (39)$$

- Correction terms

$$V_{cdr} = L \times k_d \times sign(S_d) \quad (40)$$

$$V_{cqr} = L \times k_q \times sign(S_q) \quad (41)$$

In the practical implementation using MATLAB/Simulink, the chattering phenomenon was mitigated by replacing the discontinuous sign (S) function with the Saturation block. This modification provides a smoother control action around the sliding surface while preserving the robustness and stability of the sliding mode control controller.

Once you have completed the third part, you will receive the control laws that have been generated from the sliding mode design V_{dref} and V_{qref}. These will then be transformed into the stationary reference frame (a, b, c) and compared with triangular carriers, in order to generate the control pulses for the converter semiconductors.

A wide range of modulation strategies are at your disposal. Please note that some of these can be adapted to all types of multilevel converters, while others are specific to a given converter structure. In this study, we utilize the Phase-Shifted Pulse-Width Modulation (PS-PWM) technique to generate the control pulses. This method is straightforward to implement in comparison with other PWM techniques, and it achieves a low level of total harmonic distortion (THD) in the converter output voltage, whatever the value of the modulation index, while naturally ensuring voltage balancing [35, 36].

In multicell converters such as FCMC and SMC, each PS-PWM carrier signal is associated with a specific power cell or pair of switches.

In the case of a general seven-level FCMC, control is achieved using a global modulating signal and a set of carriers, offset from each other by an angle of $\pi/3$ as shown in Figure 5. Figure 6 shows a sinusoidal reference signal and the carriers used in PS-PWM modulation applied to a seven-level FCMC. In this converter, PS-PWM requires six carrier signals of equal amplitude and frequency, oscillating between +1 and -1, and phase-shifted with respect to each other by a constant angle $\pi/3$ between consecutive carriers. A sinusoidal reference signal, normalized to the interval [-1, 1] in linear modulation mode, is compared with these six carriers to generate the control pulses. Each comparison provides a binary output: equal to 1 when the reference signal is exceeds or equal the carrier signal, and 0 otherwise [18, 37].

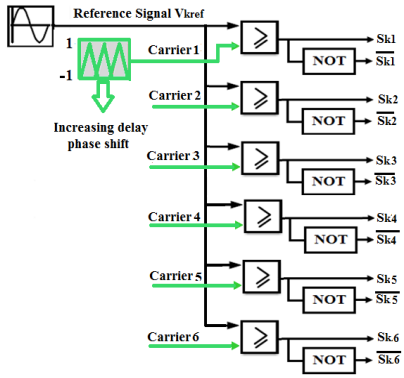


Figure 5. Schematic diagram of the PS-PWM control of a flying capacitor multicell converter

Thus, SMC control is achieved using a global modulating signal and two sets of carrier signals offset from each other by an angle of $2\pi/3$, as shown in Figure 7. Figure 8 shows a sinusoidal reference signal and the carriers used in PS-PWM modulation for a seven-level SMC.

In this converter, PS-PWM requires six carrier signals. The three upper carriers, which oscillate between 0 and 1, are phase-shifted by a constant angle of $2\pi/3$ between consecutive carriers and are compared with the reference signal, normalized to the interval [-1, 1], in order to generate the control pulses for the first-stage cells. At the same time, the three lower carriers, which oscillate between 0 and -1, are also phase-shifted by an identical angle of $2\pi/3$ between consecutive carriers and compared with the same reference signal to produce the control signals for the second-stage cells. Each comparison produces a binary output: 1 if the reference signal is greater than or equal to the carrier signal, and ' otherwise [18, 29, 30, 38].

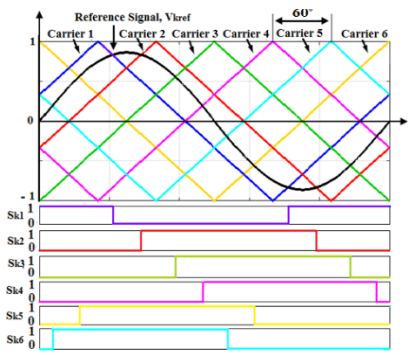


Figure 6. PS-PWM and states of power switches for 7-level FCMC

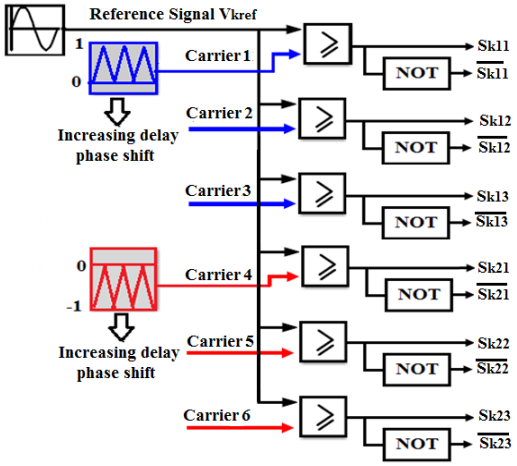


Figure 7. Schematic diagram of the PS-PWM control of a SMC

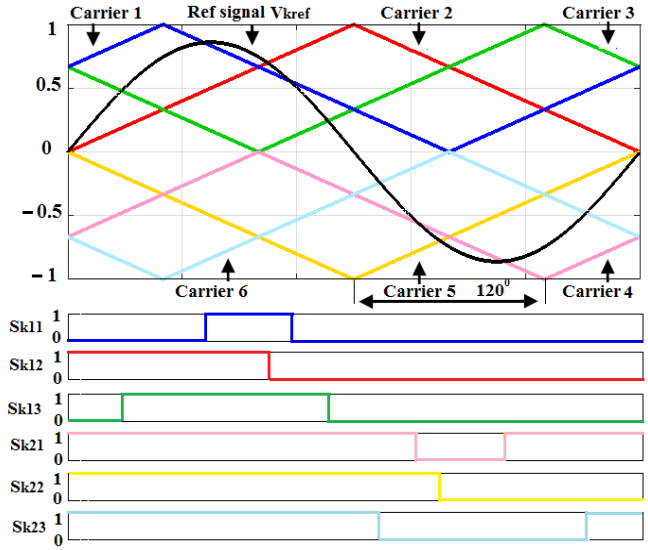


Figure 8. PS-PWM and states of power switches for 7-level SMC

4. SIMULATIONS AND RESULTS ANALYSIS

In order to demonstrate the performance of the STATCOM in reactive power compensation, power factor improvement, and voltage regulation in low-voltage distribution networks, simulations were carried out using series multicell converters with floating capacitance or stacked multicell converters, based on sliding-mode control.

In order to achieve this end, the results of the simulation will be presented, including voltage dips and over voltages, at the source in symmetrical form, as well as the connection of additional balanced inductive or capacitive loads. The system under consideration is simulated in MATLAB/Simulink, with the following model parameters for STATCOM being of particular note [39]: The expected reactive power compensation capacity is $\pm 100\ kVar$; the power network operates at $381\ V$, $2\ MVA$, $50\ Hz$, the Source resistance is $R_s = 7.3\ m\Omega$, the source inductance is $L_s = 0.23\ mH$, the coupling inductance $L = 0.7\ mH$; capacitor filter $C = 4.5\ mF$ the DC bus capacitors $C = 4000\ \mu F$; and the reference voltage on the DC side $V_{dcref} = 750\ V$. The model incorporates three distinct categories of load: A fixed load of $100kW$, and two dynamic loads of $+50\ kVar$ and $-50\ kVar$. The sampling frequency of the PS-PWM has been set to $2\ kHz$.

Case 1: Performance evaluation under voltage Sag/swell of main source

In this case, the source voltage exhibited symmetrical overvoltages of 6% with respect to nominal voltage during the interval from 0.1 s to 0.22 s, followed by symmetrical voltage dips of 6% with respect to nominal voltage during the interval from 0.32 s to 0.42 s.

As illustrated in Figure 9, the root mean square (RMS) voltage per phase V_{sa} at the common connection point (PCC) of the network is depicted in the absence of STATCOM. As demonstrated by the figure, the voltage amplitude at the PCC exhibits an increase of 6% compared with the fundamental voltage during the interval spanning from 0.1 s to 0.22 s. Subsequently, a reduction of 6% in the voltage amplitude at the PCC is observed during the subsequent interval from 0.32 s to 0.42 s, in comparison with the fundamental voltage.

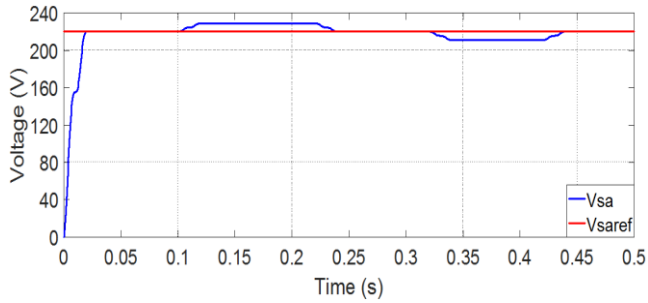


Figure 9. RMS voltage phase at PCC without STATCOM under voltage sag/swell

Figure 10 illustrates the three-phase voltage at the PCC without the STATCOM, showing the variation in the source voltage.

Figure 11 shows the RMS voltage per phase V_{sa} at the PCC with STATCOM. As can be seen, the STATCOM compensator with the proposed control adequately and effectively corrects the voltage drop and voltage dip created at the PCC, with remarkable performance.

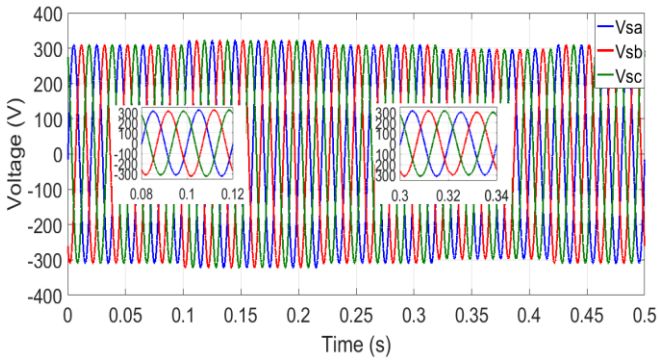


Figure 10. 3-phase voltage (abc) at PCC without STATCOM under voltage sag/swell

Figure 12 shows STATCOM's behavior in terms of reactive power injection into the grid at the PCC. It can be seen that STATCOM supplies reactive power during the interval 0.1 s to 0.22 s and absorbs reactive power during the interval 0.32 s to 0.42 s. This exchange of reactive power is

controlled by the amplitude of the voltage produced at the converter output V_c, which is in phase with the grid voltage V_s. During the interval 0.1 s to 0.22 s, when the voltage V_s is lower than V_c, the STATCOM supplies reactive power at the PCC of the network. In this operating condition, the compensator operates in capacitive mode, and the compensator current I_c leads the voltage at the PCC V_s by $\pi/2$. In the interval 0.32 s to 0.42 s, when the voltage V_s is greater than V_c, the STATCOM absorbs a quantity of reactive power; in this case, the compensator operates in inductive mode, and the compensator current I_c lags the voltage V_s by $\pi/2$, as shown in Figure 13.

Figure 14 shows the three-phase voltages (V_{sabc}) at the PCC with STATCOM action as the source voltage varies. It can be seen that the voltage waveforms reach the desired values.

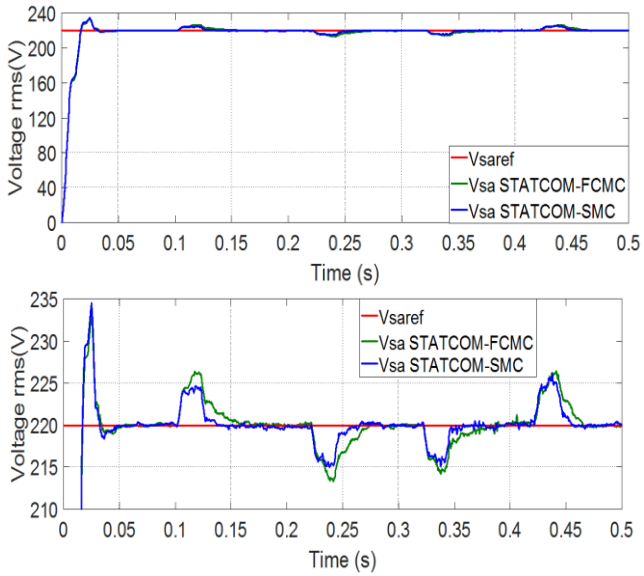


Figure 11. RMS voltage phase at PCC with STATCOM under voltage sag/swell

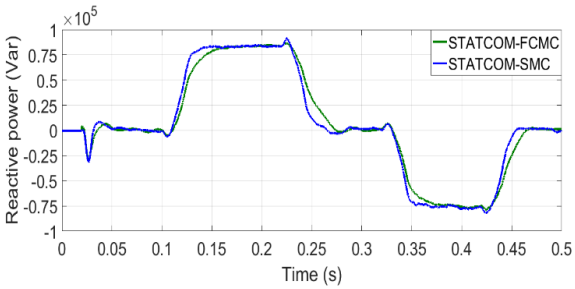
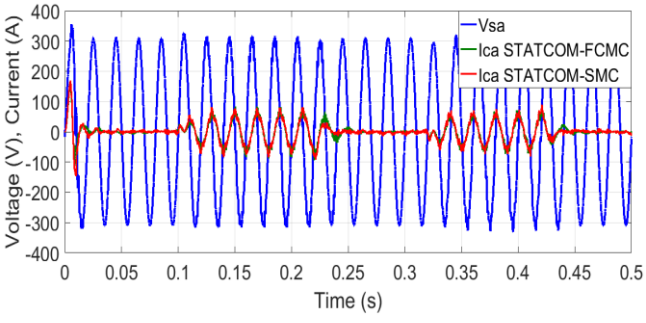


Figure 12. Reactive power injected or absorbed by the STATCOM under voltage sag/swell conditions



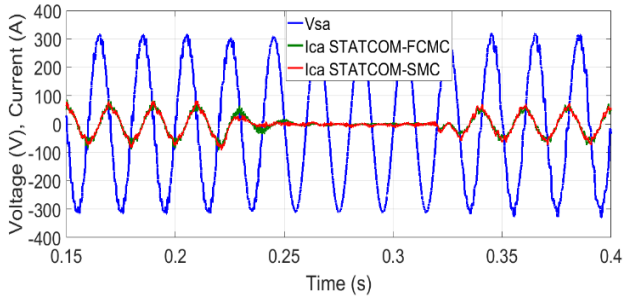


Figure 13. Phase voltage at PCC and STATCOM current under voltage sag/swell conditions

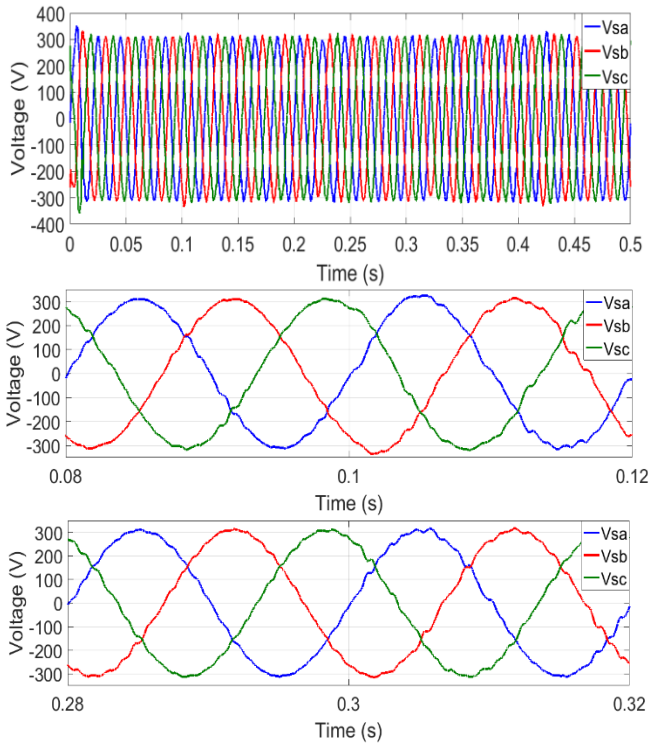


Figure 14. 3-phase voltage (abc) at PCC with STATCOM under voltage sag/swell conditions

As illustrated in Figure 15, the STATCOM DC bus voltage is displayed. It is evident that the DC voltage regulation block is highly effective in maintaining a constant DC-side voltage, with a rapid response, minimal overshoot, and a reduced settling time.

Figure 16 shows the voltage (V_{caO}) at the converter output between phase a and the midpoint O of the DC bus, which can assume seven possible values: 0, $\pm 375\,V$, $\pm 250\,V$ and $\pm 125\,V$. Figure 17 shows the phase-to-phase voltage (V_{cab}) at the converter output.

Figure 18 shows the harmonic spectrum obtained from the phase voltage (V_{sa}) at the PCC, using the FFT block for the two STATCOM FCMC and STATCOM SMC structures when the source voltage varies. Table 3 shows the total harmonic distortion (THD) of the phase voltage (V_{sa}) at the PCC for the two structures.

Table 3. Comparative analyses under voltage sag/swell

Phase Voltage V_{sa}		
	THD(%)	FD (V)
STATCOM-FCMC	5.12	310.1
STATCOM-SMC	4.31	310.2

From Table 3, we observe that the two structures yield almost identical fundamental voltage values. However, the STATCOM SMC structure provides better performance in terms of THD. Nevertheless, the THD values of both structures remain in compliance with the IEEE Std. 519-1992 [40].

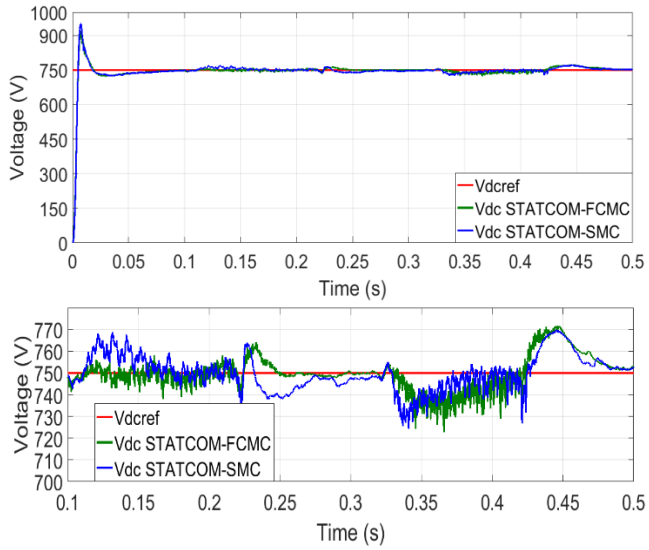


Figure 15. STATCOM DC bus voltage under voltage sag/swell

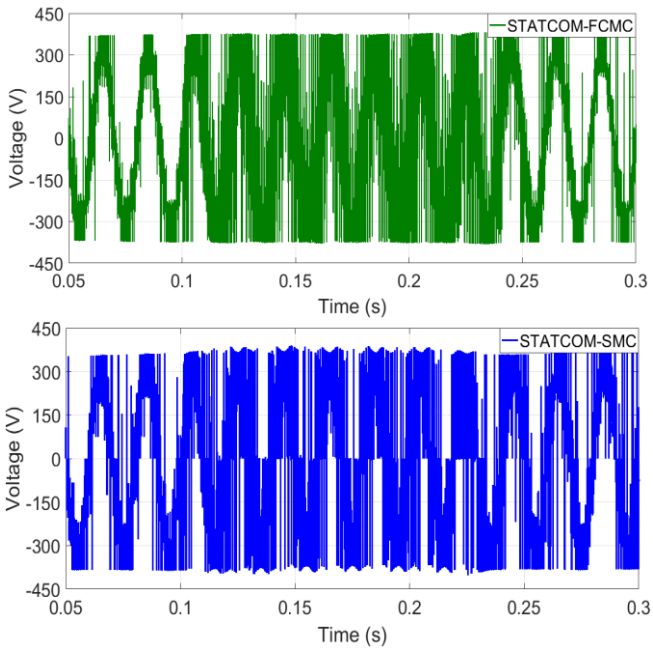
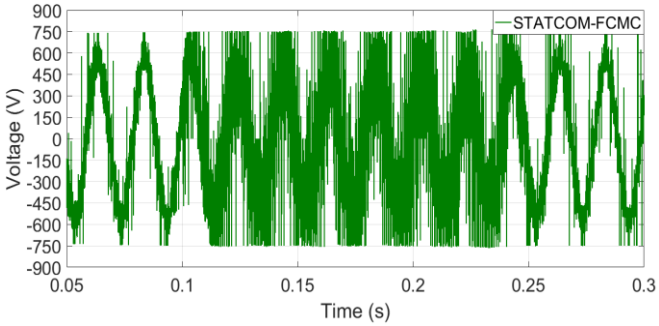


Figure 16. Output voltage phase (V_{caO}) of the STATCOM converter under voltage sag/swell



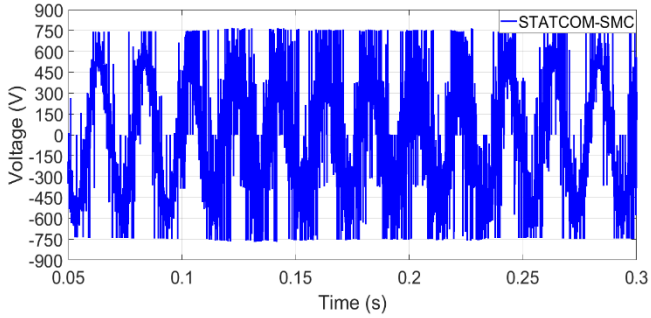


Figure 17. Output voltage between phases of the STATCOM Converter (V_{cab}) under voltage sag/swell

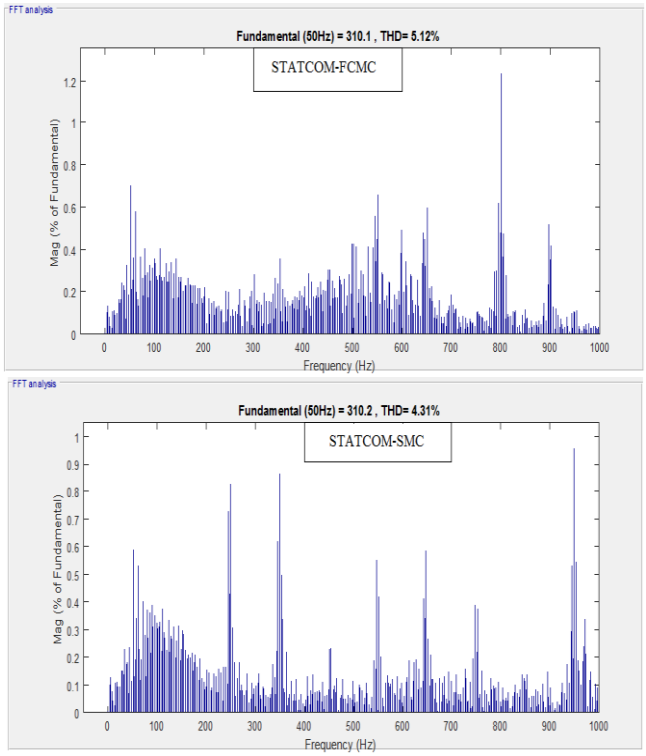


Figure 18. Harmonic spectrum of phase voltage at PCC (V_{sa}). under voltage sag/swell

Case 2: Performance evaluation under balanced reactive load conditions

In this test scenario, the dynamic performance of the STATCOM with a balanced reactive load is illustrated. Figure 19 shows the evolution of the RMS voltage per phase V_{sa} at the PCC, without any STATCOM action, with the connection of balanced capacitive and inductive loads. As illustrated in Figure 19, the connection of balanced capacitive loads results in an approximately 5% in the PCC voltage above its nominal value during the interval from 0.1 s to 0.2 s. conversely, in the 0.3 s to 0.4 s interval, inductive loads cause a voltage dip, degrading the power quality of the network.

As illustrated in Figure 20, the three-phase voltages at the PCC are depicted in the absence of STATCOM, in scenarios where balanced capacitive and inductive loads are present. As illustrated in Figure 21, the voltage and current for each phase at the PCC are clearly displayed. It is evident that, during the interval from 0.1 s to 0.2 s, the current precedes the voltage by a specific angle, a consequence of the

integration of the capacitive load with the mains. Conversely, between 0.3 and 0.4 seconds, the current lags the voltage by an angle, a consequence of the inductive load's connection to the grid. It should be noted that the system power factor is not equal to 1.

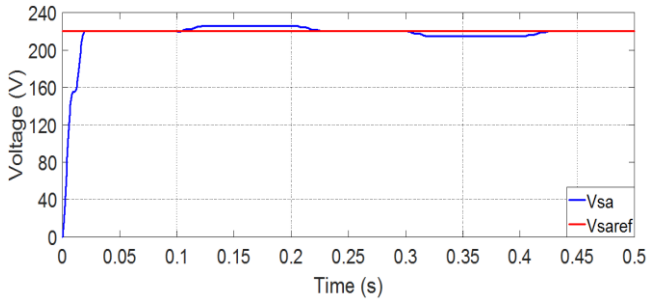


Figure 19. RMS voltage phase at PCC without STATCOM under balanced reactive load conditions

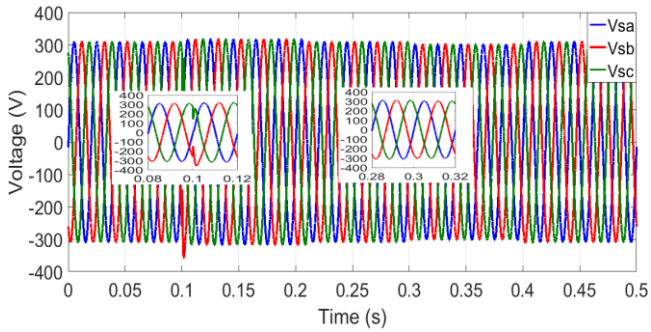


Figure 20. 3-phase voltage (abc) at PCC without STATCOM under balanced reactive load conditions

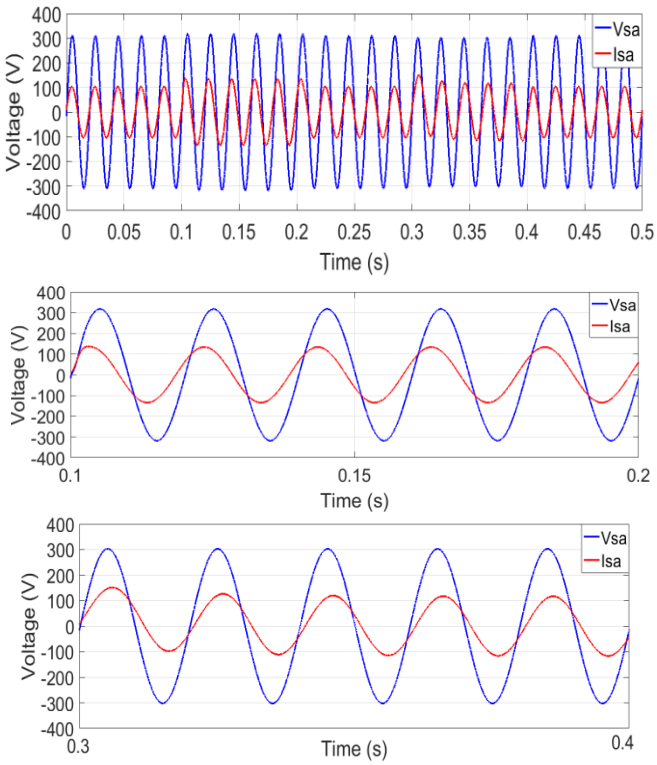


Figure 21. Voltage and current of phase A at the PCC without STATCOM action under balanced reactive load conditions

To ensure stable and efficient operation of the network, the use of a STATCOM is therefore essential.

Figure 22 shows the evolution of the voltage per phase V_s at the PCC, with STATCOM action and the connection of balanced capacitive and inductive loads. It can be observed from this figure that the waveform of the RMS voltage per phase V_s at the PCC reaches its reference value, exhibiting a fast dynamic response, minimal overshoot, and reduced settling time.

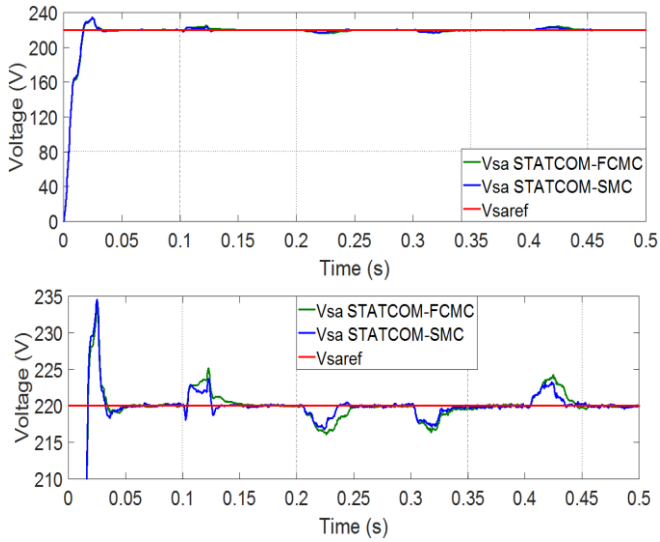


Figure 22. RMS voltage phase at PCC with STATCOM under balanced reactive load conditions

Figure 23 shows the behavior of the STATCOM in terms of reactive power injection into the distribution network. It can be seen that STATCOM absorbs reactive power from the network during the 0.1 s to 0.2 s interval, to compensate for the overvoltage created by the capacitive loads, and injects reactive power into the network during the 0.3 s to 0.4 s interval, to compensate for the voltage dip created by the inductive load.

This transfer of reactive power occurs through the coupling leakage inductance, which helps smooth the compensator current I_c, lagging or leading the voltage V_s at the PCC, as shown in Figure 24.

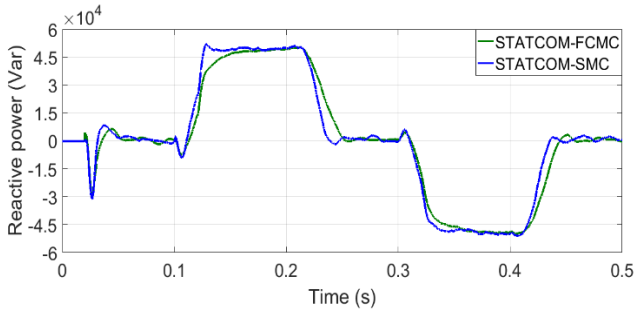


Figure 23. Reactive power injected or absorbed by the STATCOM under balanced reactive load conditions

Figure 25 also shows the voltage V_s and current I_s of one phase at the PCC with the STATCOM in operation. It can be seen that the current I_s and voltage V_s are almost perfectly in phase, which means that a unity power factor has been achieved.

As demonstrated in Figure 26, the DC bus voltage is

shown when balanced, capacitive and inductive loads are connected. It is evident that the DC voltage control loop is demonstrating its efficacy in maintaining the DC-side voltage at a consistent level, with minimal fluctuations.

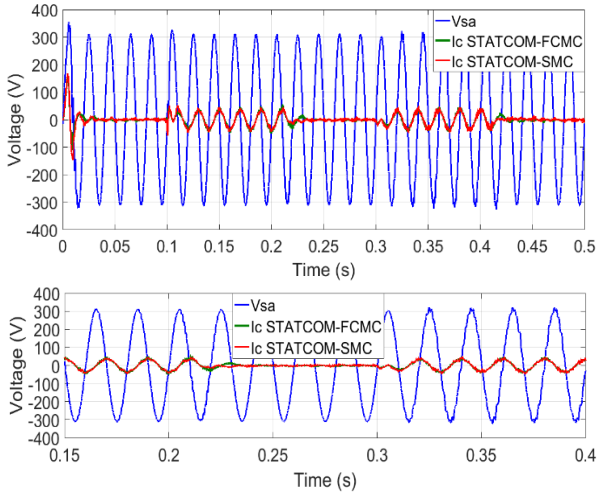


Figure 24. Source voltage and current of STATCOM output under balanced reactive load conditions

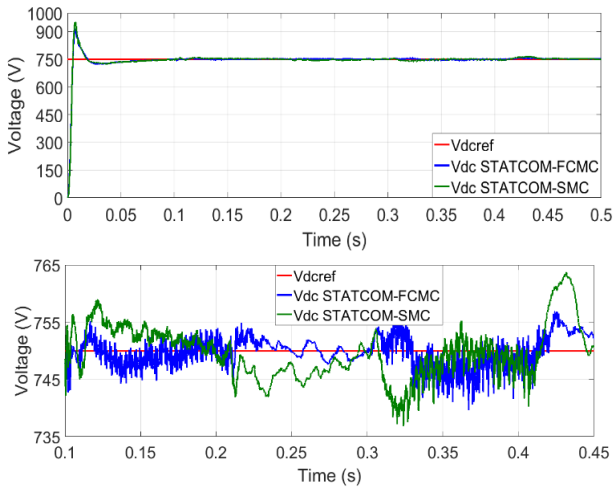
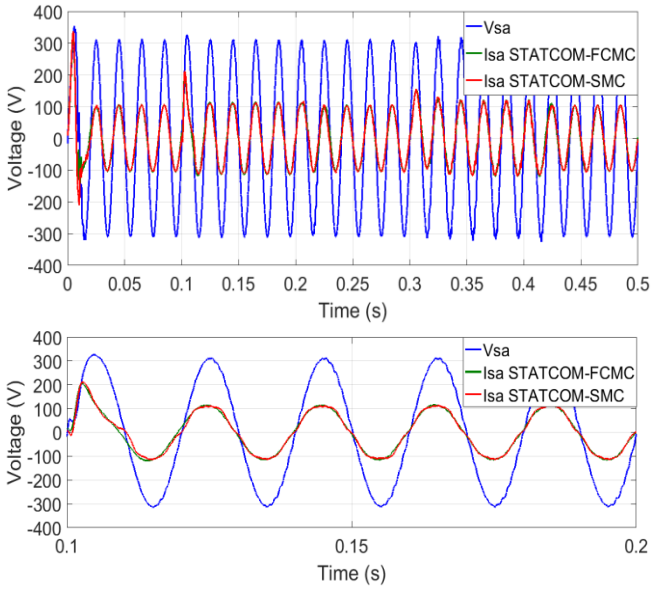


Figure 25. STATCOM DC bus voltage under balanced reactive load conditions



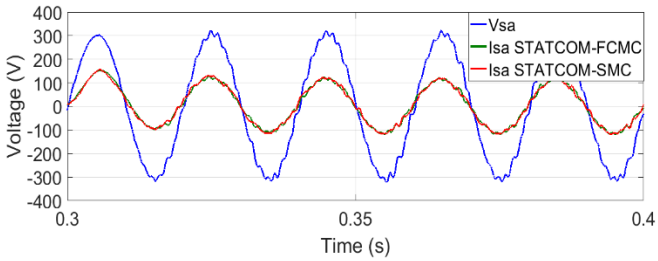


Figure 26. Voltage and current of phase a at the PCC with STATCOM action under balanced reactive load conditions

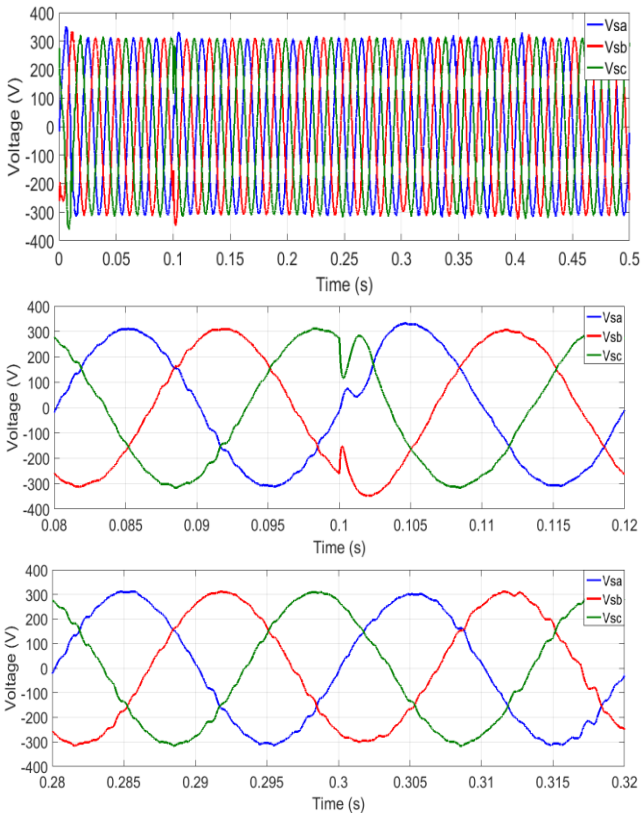


Figure 27. 3-phase voltage (abc) at PCC with STATCOM under balanced reactive load conditions

Table 4. Comparative analyses under balanced reactive load conditions

Voltage Vsan		
	THD(%)	FD(V)
STATCOM-FCMC	3.95	310.2
STATCOM-SMC	3.56	310.2

5. CONCLUSIONS

In this paper, a performance analysis of two seven-level multicell converter structures: the floating capacitor multicell converter (FCMC) and the SMC, has been presented in the context of STATCOM applications for a low-voltage network. Both structures are controlled by a sliding mode control strategy in order to enhance the dynamic performance of the STATCOM in terms of reactive power compensation, voltage regulation, and power factor improvement. A comprehensive mathematical model of the STATCOM system integrating both converters was developed to evaluate the impact of the compensators and the proposed control

strategies on the overall behavior of the electrical network. The PS-PWM modulation technique highlighted significant differences between the two structures in terms of configuration, performance, and control complexity. Simulation results obtained using MATLAB/Simulink demonstrated that both structures are capable of maintaining a stable voltage at the PCC with a fast dynamic response, through the rapid injection or absorption of reactive power, even under network disturbances such as load variations, voltage fluctuations, overvoltages, and voltage sags. In addition, the voltage THD obtained at the PCC, under different disturbance conditions, is well within the IEEE-519 standard (5%) for both structures, with the STATCOM structure based on an SMC offering better performance in terms of THD.

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NOMENCLATURE

D	The direct axis
F	The frequency (Hz)
I	The current (A)
L	The inductance (H)
P	The number of cell
P	The current active power (Ω)
Q	The Reactive power (Var)
R	The Resistance (Hz)
V_s	The Voltage source (V)

V_c	The Voltage componsator (V)
Q	The quadrature axis
N	Number of stacked

Greek symbols

θ	The phase of the grid voltage

Subscripts

CHB	Cascade H-bridge
FACTS	Flexible Alternative Current Transmission System
FC	Flying capacitor
FFT	Fast Fourier Transform
IGBT	insulated-gate bipolar transistor
NPC	Neutral point clamped
PCC	Point of common connection
PLL	Phase-locked loop
PS-PWM	Phase-Shifted Pulse Width Modulation
RMS	Root Mean Square
SMC	Stacked multicell converter
SSSC	static synchronous series compensator
STATCOM	Synchronous static compensators
SVC	Static Var Compensator
TCSC	thyristor-controlled series capacitor
THD	Total harmonic distortion
UPFC	Unified Power Flow Controller
VSC	Voltage Source Converter