



Hardware-in-the-Loop Simulation and FPGA Implementation of a Single-Phase PFC Controller

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<https://doi.org/10.18280/jesa.580918>

ABSTRACT

Received: 5 August 2025

Revised: 10 September 2025

Accepted: 24 September 2025

Available online: 30 September 2025

Keywords:

discrete-time control, FPGA, HIL, Power Factor Correction, resonant converter, Xilinx System Generator

Rapid growth of smart appliances, computers, telecom equipment, cloud servers, EVs has significantly increased the demand for high power quality from the utility grid. However, the integration of non-linear loads adversely affects the Power Factor (PF), resulting in degraded power quality, reduced energy efficiency, voltage regulation issues, and potential damage to connected equipment. This work presents a discrete-time control strategy for PF correction, implemented on reconfigurable FPGA platform. A case study is conducted using an active boost converter driving resonant inverter topology for 300 V to 120 V DC-DC conversion. The phase-locked loop continuously tracks grid voltage and provides frequency reference for Dead-beat current controller, which ensures stable DC bus voltage and improved PF. Hardware-in-the-Loop simulation is carried out using MATLAB-Simulink, with control logic developed in Xilinx System Generator for real-time implementation on Zynq-XC7Z020-1clg484 FPGA. Controller tracks set DC bus voltage within four grid cycles (80 ms) and maintains sinusoidal line current in-phase with grid voltage, achieving unity PF. FPGA power dissipation is 0.307 W, with timing analysis confirming scope for higher-speed operation. Experimental validation on 3 kW converter prototype verifies FPGA-based PF controller's fast dynamic response, efficient tracking, and robustness, ensuring feasibility for integrated applications including EV chargers, telecom, and server power applications.

1. INTRODUCTION

Electrical systems and equipment draw power from the utility grid, and Power Factor (PF) is a key measure of how efficiently this power is utilized. When PF drops below acceptable levels (e.g., below 0.92), a significant amount of power is converted into harmonics, which is reflected back into the utility grid, causing harmonic distortion [1]. The rapid adoption of Electric Vehicles (EVs), smart appliances, telecom equipment, and renewable energy sources such as fuel cells, solar photovoltaic, and wind energy are exacerbating this issue. This rising integration of renewable energy sources, coupled with the growing complexity of modern power systems, has posed significant challenges to maintaining high power quality. As a result, maintaining power quality at the utility grid is becoming a challenge for utility companies [2].

To address these challenges, IEEE standards have been established to regulate harmonic distortion and ensure improved PF across all devices connected to the utility grid [3,

4]. In this work, a Power Factor Correction (PFC) control system is developed to enhance PF, improve power quality, and reduce the strain on electrical distribution networks. The proposed solution is developed on Field-Programmable Gate Array (FPGA) platform due to its unique advantages, such as high speed, parallel processing capability, re-programmability, and re-configurability. These features make FPGAs ideal for implementing real-time control systems. The FPGA-based hardware design offers design flexibility, low latency, and the potential to develop Application Specific Integrated Circuits (ASICs). This approach provides a cost-effective and efficient solution that can be readily used as a pre-stage for appliances and electrical systems connected directly to the utility grid. The proposed system not only enhances energy efficiency and lowers electricity costs but also mitigates the risks of equipment instability and failure, while increasing the load-handling capacity of existing electrical infrastructure [5].

In the development of control strategy, testing is a critical step that enables thorough validation of functionality, stability,

reliability, and performance of the control system. Recently, the Hardware-in-the-Loop (HIL) simulation has emerged as a powerful technique for closed-loop validation of control strategies prior to physical prototyping of any system. By enabling real-time investigation of control systems, HIL simulation protects physical systems from potential damage during the early design phases. Additionally, it reduces development costs, accelerates design timelines, and shortens time-to-market, making it a widely adopted approach in the design, development, and testing of industrial systems and various other applications [6-11].

1.1 Motivation

The increasing integration of renewable energy sources, rapid adoption of EVs, and the growing use of smart appliances have significantly increased the complexity of modern power systems, posing challenges to maintaining high power quality and grid stability. PF is critical in improving energy efficiency and mitigating harmonic distortion, which, if unaddressed, can lead to grid instability, equipment failures, and increased operational costs. However, the development and validation of PFC systems require robust, real-time testing platforms to ensure performance and reliability. FPGA-based HIL simulation offers an ideal solution, enabling precise, real-time evaluation of PFC systems while reducing development costs, minimizing risks, and accelerating design timelines. By leveraging the speed, parallelism, and re-programmability of FPGAs, this study addresses the need for efficient and reliable PFC units that enhance power quality and support the evolving demands of modern power systems. Also, ASIC can be developed as PFC is recommended front-end for all utility grid connected equipment.

1.2 Literature review

PFC units can be implemented using various topologies, broadly classified as active and passive PFC topologies [12]. Passive PFC topologies are primarily used in low-power (approximately 100 W) and cost-sensitive applications, employ low-pass filters and capacitor banks [13, 14]. However, active PFC topologies are widely adopted due to their superior performance. Active PFC circuit utilizes high frequency switching devices to synchronize the current phase with the input voltage, shaping the current wave closer to a sine wave. This improves the PF and reduces harmonic distortion [12, 15]. The commonly used PFC topology is the conventional boost topology, that includes a front-end full-bridge rectifier (diode) followed by a boost converter. This method is well-suited for applications in the low to medium power range. At high power levels, diode bridge plays a crucial role in the application, necessitating effective management of heat dissipation within a confined surface area [16, 17]. Recently, many bridgeless topologies were also used in high-power applications. These bridgeless PFC circuits lower the conduction loss by minimizing the semiconductor component count in the current path, thereby enhancing efficiency [18-20]. Though they result in better efficiency, their operating range is limited. Also, these topologies can work well at high load conditions (60%-100% load) but fail at light load conditions. Some bridgeless topologies use auxiliary circuits with simple control schemes along with the conventional converter, to improve efficiency at light load conditions [21-23]. In this research, a versatile bridgeless active boost converter topology is adopted to

support PF correction and harmonic compensation, offering improved efficiency.

Further, in the literature, various types of current controllers have been discussed for active filtering applications. The synchronous reference frame-based current controller is widely used due to its popularity in various applications; but it has limited bandwidth and requires extensive transformation computations [24]. Input voltage-based current reference control methods are another common choice but often suffer from harmonic distortion, requiring modifications or hybrid control schemes [25, 26]. The hysteresis current controller is simple to implement but operates with a variable switching frequency. Although modified hysteresis methods achieve constant switching frequency, they are complex and less suitable for fully digital implementations.

The Dead-Beat Current Control (DBCC) technique, a digital control method, is widely adopted in power converter applications such as active rectifiers, power filters, and Pulse Width Modulation (PWM) rectifiers [27]. DBCC offers constant switching frequency, high control bandwidth, and straightforward digital implementation, making it an ideal choice for this work. While alternative controllers like Predictive Current Control (PCC) and Sliding Mode Control (SMC) are also effective for PFC applications, PCC demands intensive computation that challenges real-time FPGA execution, whereas SMC often introduces chattering that increases EMI and can interfere with soft-switching in resonant stages. In contrast, DBCC ensures fast dynamic tracking with minimal computational burden, deterministic FPGA implementation, and negligible disturbance to the resonant stage, making it the most practical and effective choice for the proposed system. Digital controllers for PFC systems can be implemented on various hardware platforms, including FPGAs, DSPs, microcontrollers and microprocessors [28-31]. Microprocessors and microcontrollers are popular for their accessibility, low cost, and ease of use. However, these platforms execute control functions sequentially, leading to low computational speeds [32]. DSPs, optimized for mathematical computations, demand substantial processing power and a robust system architecture to manage complex control systems. Additionally, since DSPs rely on software-based execution, they are less suited for high-speed control algorithms requiring rapid response. FPGAs, in contrast, offer quick response time, parallel architecture, high speed, and re-programmable and re-configurable capabilities, making them ideal for fast and reliable implementations [33-35].

Despite their advantages, FPGAs have yet to gain widespread acceptance in power electronics control applications. This is primarily due to key limitations, including the high cost of firmware development, the need for specialized HDL programming expertise, and the relatively higher cost of FPGA boards compared to other control platforms. Additionally, the complexity of HDL programming presents a significant challenge in developing fully digital control systems for power converter applications. Designing discrete-time equations and implementing them onto an FPGA platform remains a bottleneck for researchers and developers in this domain.

Now, for controller validation, HIL simulation has emerged as an efficient and versatile approach that supports mixed-system simulation and real-time performance evaluation. The literature highlights various HIL simulation environments, such as MATLAB-Modelsim, MATLAB-Simulink-XSG

(Xilinx System Generator), MATLAB-Simulink-DSP Builder, Opal-RT, dSPACE, e-Tap, Typhoon HIL, Plexim RT Box, NI HIL, and Speedgoat HIL [8, 36-38]. Many of these platforms are proprietary and expensive, making them suitable for large-scale or high-power applications such as automotive systems, aerospace systems, and other industrial systems where physical system verification is costly or hazardous for the operator. Other HIL platforms integrate MATLAB with DSPs, microprocessors, FPGAs, or custom platforms for the development of applications like power filters, photovoltaic systems, distributed generators, delta inverters etc. In all these applications, HIL platforms are used for development, testing, and performance evaluation of systems in closed-loop environments.

Despite extensive research on HIL approaches, the application of FPGA-based HIL simulation for single-phase PFC systems remains underexplored. Furthermore, the potential for leveraging FPGA's parallel processing capabilities to achieve real-time accuracy and implementation flexibility in PFC control needs further investigation. To address these gaps, in this work, a HIL simulation test-bench is developed using MATLAB-Simulink-XSG software integrated with Xilinx VIVADO Design Suite. This setup facilitates closed-loop testing and hardware implementation of the control system on a reconfigurable FPGA platform [33, 39-41]. All system blocks are discretized, and their discrete-time equations are implemented on the FPGA, allowing evaluation of the controller's tracking and transient performance under dynamic operating conditions. This approach ensures efficient and accurate validation of the complete digital controller for a DC-DC converter with a front-end PFC stage, a configuration widely recommended for all utility grid-connected systems, and also supports future ASIC development.

The core novelty of this work lies in the unified FPGA-based implementation of a single-phase PF correction controller integrated with a resonant inverter-based DC-DC converter. Unlike prior studies [33, 42], which primarily focused on HIL validation platforms, this work extends the concept to a fully functional FPGA realization that simultaneously executes both the Dead-beat current control

(for the PFC stage) and hybrid control of the DC-DC converter on a single digital platform. Discrete-time control equations for both stages are formulated and implemented, enabling seamless coordination and real-time execution within FPGA constraints. This integrated architecture enhances hardware efficiency, reduces controller redundancy, and provides a direct pathway toward ASIC development. Furthermore, while [33] primarily employs HIL-based validation for an Induction heating system, which has linear load characteristics, the present work validates a controller for a system with non-linear load behavior. In addition, it advances the approach by combining HIL-based verification with experimental validation of the integrated architecture on an FPGA platform, thereby demonstrating both feasibility and reliability in practical operation.

This paper is organized as follows: The power converter system for single-phase PFC is covered in Section 2. Design of control system considering resonant load is covered in Section 3. Section 4 covers simulation results with different parametric conditions as well as the experimental results, followed by conclusions in Section 5.

2. PFC CIRCUIT WITH RESONANT CONVERTER SYSTEM

The AC to DC converter is an essential part of many power electronic systems and can be designed traditionally using diode rectifier or thyristor rectifier, to produce either fixed or variable DC bus output voltage, respectively. These rectifiers behave as non-linear loads and hence the current drawn by them contains fundamental as well as harmonic components. This distorts the mains voltage and subsequently, the other loads connected to the grid also receive distorted voltage. Hence, in this research we have used a PWM rectifier (boost converter) which draws near sinusoidal current from the mains, regulates the DC bus output voltage and also improves the input PF. This section presents the power circuit of the single-phase PFC with LCC resonant converter system (a DC-DC converter).

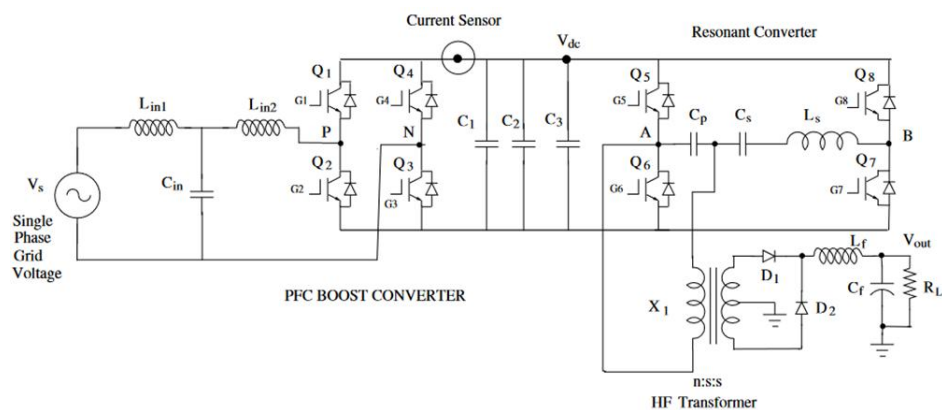


Figure 1. Power circuit of single-phase PFC with resonant converter system

The complete power circuit diagram of single-phase PFC with DC-DC converter system using PWM rectifier is shown in Figure 1. At first, 230 V, 50 Hz grid voltage (V_s/V_{grid}) is passed through a LCL ($L_{in1} - C_{in} - L_{in2}$) filter, in order to filter out harmonics in the grid current and reduce the total harmonic distortion. The front-end active rectifier (i.e. PFC boost converter) is designed using 4-IGBT switches ($Q1-Q4$).

It regulates the DC bus voltage and maintains the input PF close to unity, using an efficient DBCC technique, as discussed in Section 3. DC bus capacitor ($C1$) and IGBT snubber capacitors ($C2$ and $C3$) are connected across DC bus to ensure a more stable DC bus voltage (V_{dc}) and protect the preceding converter stage from the transient voltage spikes, surges and electromagnetic interference. This bus voltage is

effectively modulated and rectified. Modulation is achieved through H-bridge converter consisting of four IGBT switches (Q5 to Q8), and a series-parallel ($L_s - C_s - C_p$) resonant load. In this circuit, each switch operates at a 50% duty cycle, with complementary control applied to switches in the same leg, incorporating a 180° phase shift and a dead-time interval to avoid cross-conduction. A phase shift controlled by pulse-width modulation is applied between the two opposing legs. This modulation stage is linked to a rectifier bridge and load (R_L) via a high-frequency transformer, providing both electrical isolation and voltage or current scaling. Further, the high-frequency AC waveforms across parallel resonant capacitor (C_p), is transformed into a unidirectional voltage by a diode rectifier (D1, D2). Here, the high-frequency ripples generated by rectifier are attenuated by $L_f - C_f$ output filter and stable DC output (V_{out}) is maintained across load, R_L . This design achieves improved power quality by reducing harmonic distortion, maintaining a stable DC bus voltage, and ensuring high PF. It provides an efficient solution for modern power electronic applications requiring robust, high-performance AC-to-DC conversion systems.

3. DISCRETE-TIME CONTROL SYSTEM

The PFC boost converter receives grid voltage and proportionally generates the DC bus voltage for the connected resonant converter system (DC-DC converter). Here, input current wave-shape is always maintained sinusoidal, in phase with input grid voltage and DC bus voltage is regulated simultaneously using an efficient PFC control strategy. Further, in converter systems, the resonant tank ($L_s - C_s - C_p$) between the modulation and rectification stage provides the resonant inverter with an inherent input-output gain that depends on the excitation frequency and PWM duty ratio. By controlling these two parameters, the system effectively regulates both output voltage and load current, as they influence the rectifier's input under varying load conditions. An efficient resonant converter control strategy enables simultaneous adjustment of the PWM duty cycle and switching frequency in response to load variations. Accordingly, the main functions of the proposed controller are: (i) To maintain input PF near unity, (ii) To regulate DC bus voltage at set reference value, (iii) To regulate output voltage, and (iv) To maintain Zero Voltage Switching (ZVS) of the resonant converter at all load conditions. These functions are achieved using FPGA controller, consisting of two major control units: PFC control unit and resonant converter control unit. The controller generates control pulses for both the front-end active rectifier (AC-DC converter) and resonant converter respectively, concerning the received feedback signals, as shown in Figure 2. Here, based on the received input and feedback signals, the PFC control unit continuously modifies the switching control pulses (G_1 – G_4) and ensures that the input PF is always maintained close to unity and the output DC bus voltage is regulated to the set reference voltage level, even though the electrical grid source voltage fluctuates. Similarly, the load parameters are continuously sensed by FPGA controller, and appropriate switching control pulses (G_5 – G_8) are generated and supplied to the LCC resonant converter such that the load current and terminal voltage are always controlled as per the custom load specifications, with respect to the present load. By using the high-speed and accurate control capabilities of FPGA technology, the

combined functionality of these control units ensures efficient and reliable operation of the power converter system. This not only enhances power quality and adaptability to load changes but also improves overall energy efficiency, making the system suitable for diverse power electronics applications.

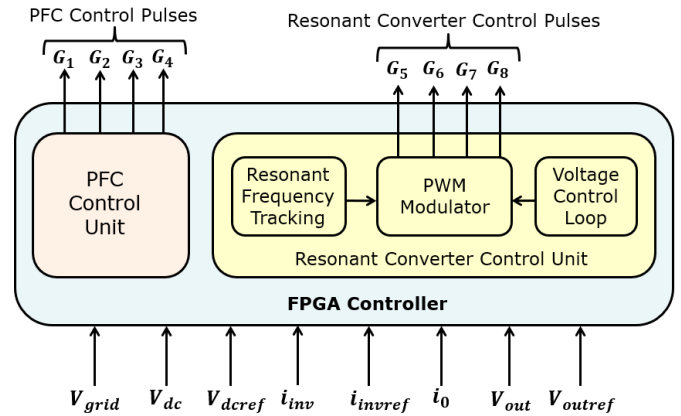


Figure 2. Controller block diagram

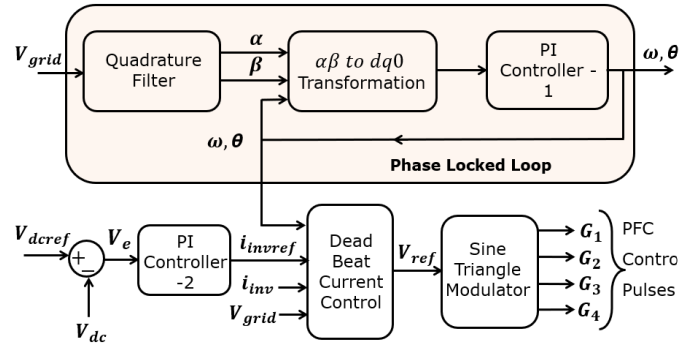


Figure 3. Block diagram of single-phase PFC control unit

A block diagram of discrete-time PFC control unit is shown in Figure 3. Here, a Phase Locked Loop (PLL) block continuously tracks the input grid voltage (V_{grid}) and generates frequency-feedback reference signal (ω) for the implementation of current controllers in the grid connected systems. The synchronous reference frame based PLL is preferred in this design, because it handles grid disturbances, harmonics and noise effectively over other PLL implementation methods. Further, it aligns directly to the fundamental frequency component of even the distorted grid signal and also performs better in the presence of unbalanced conditions. Here, first the quadrature filter generates the stationary frame quadrature components (α and β) of input V_{grid} . This quadrature filter is basically cascade of two low-pass filters that introduces total phase shift of 90° . The discrete-time equation of single stage filter is as given in Eq. (1):

$$y(n) = y(n-1) + \frac{\omega \cdot T_s}{2} [x(n) + x(n-1)] \quad (1)$$

Here, T_s represents discrete-time system's sampling time, n denotes the present time step and ω is the angular frequency. These quadrature components of V_{grid} ($\alpha - \beta - 0$ signals) need to be converted into rotating reference frame ($d - q - 0$), for which $\alpha - \beta - 0$ to $d - q - 0$ transformation is carried out using Park transformation as in Eq (2):

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta & 0 \\ -\sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \quad (2)$$

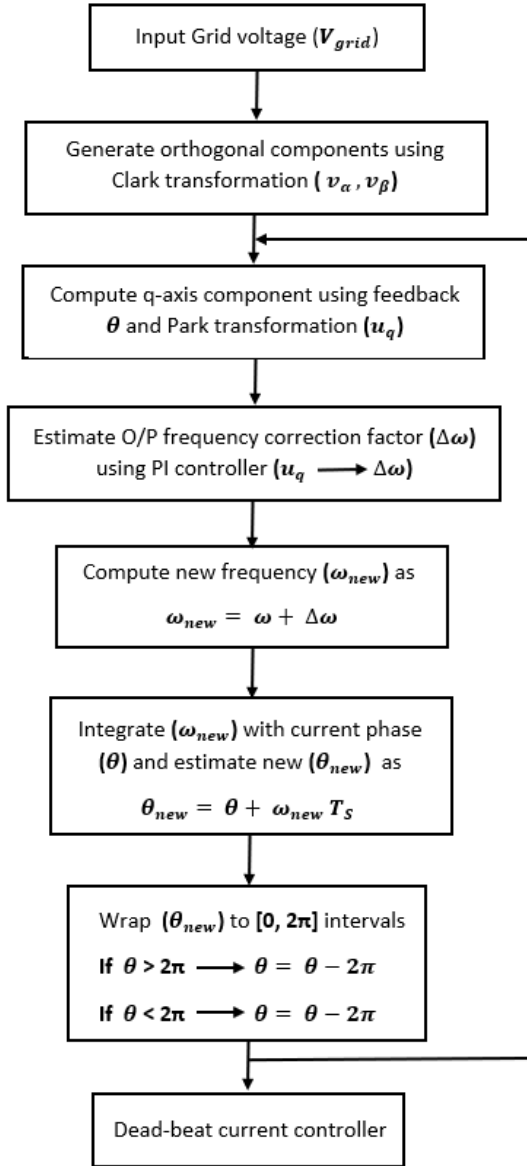


Figure 4. Flowchart - Phase tracking loop in PLL

In this equation, v_α, v_β and v_0 are stationary frame components, θ is estimated phase angle, u_d, u_q and u_0 are rotating frame components of the grid voltage. This transformation requires sinusoidal signals with instantaneous phase angle (θ), which is fed back from the PLL block, to ensure that loop remains locked to the input grid signal. The q-axis component of this transformation (u_q), directly represents the phase error. If value of $u_q = 0$, means the input grid signal (V_{grid}) and the estimated PLL output are perfectly synchronized. Otherwise, the PLL iteratively refines its output (ω) to minimize the phase error. The PI controller-1 processes this u_q signal and accordingly modifies the estimated frequency (ω), ensuring that it remains locked to the grid voltage's frequency and phase. The flowchart (Figure 4) illustrates the phase tracking loop within the PLL used in the Dead-Beat PFC controller - a fully digital process that synchronizes the control system with the grid voltage during every control interrupt. The loop begins with the measurement

of grid voltage, which are first transformed into the stationary α - β frame and then into the rotating d-q frame using the previously estimated phase angle (θ) from the last sampling period. The resulting q-axis voltage (u_q) serves as the phase error signal; any nonzero value indicates phase misalignment. This error is processed by a PI controller that generates a frequency correction term ($\Delta\omega$), which is added to the nominal grid frequency. The corrected frequency (ω) is then integrated to produce an updated and synchronized phase angle (θ) for the next sampling step. The updated θ is fed back into the Park transformation for the next iteration and simultaneously supplied to the DBCC block. This ensures that the d-q transformations and voltage/current reference calculations remain precisely aligned with the grid, enabling accurate and fast PF correction.

Overall, the entire current control loop remains synchronized with the grid through this PLL mechanism, ensuring that the input current is always in phase with the grid voltage - a fundamental objective of PFC. The loop operates continuously, adaptively adjusting both ω and θ to maintain phase lock and provide a stable, real-time reference for the DBCC controller.

For generation of the sinusoidal signals ($\sin \theta$ and $\cos \theta$) required in Park transformation, Harmonic Oscillator (HO) block is used. The discrete-time equations of HO, obtained using Hybrid discretization method are,

$$x(n+1) = x(n) + h \cdot y(n) \quad (3)$$

$$y(n+1) = y(n) - h \cdot x(n+1) \quad (4)$$

In these equations, consider initial conditions as $x(0) = 0$ and $y(0) = 1$. The constant h is defined as $h = \omega \cdot T_s = 2\pi f T_s$, where f is the desired oscillation frequency, and T_s represents time interval of discrete-time samples. The frequency of sinusoidal outputs (i.e. $x(n+1)$ and $y(n+1)$) is decided by a constant h . Its implementation is carried out in a similar manner as discussed in the study [42].

The PLL block's output, θ is fed back as an input to this HO block. Accordingly, it generates the required frequency $\sin \theta$ and $\cos \theta$ signals that are used in the above stationary to rotating reference frame transformation. In all, the reference frame d-q-0 rotates at an angular speed of ω , where $\omega = 2\pi f$, f is the fundamental frequency of the input grid voltage and iteratively locks the PLL output to the grid voltage. Now to regulate the DC-bus voltage, the measured bus voltage (V_{dc}) is compared with set reference voltage (V_{dcref}) and an error signal (V_e) is generated. This error is processed by the voltage PI controller (PI controller-2), which generates the reference current (i_{invref}) used to shape the input current. The z-domain representation of PI controller is given in Eq. (5):

$$H(z) = K_p + \frac{K_i \cdot T_s}{2} \frac{(z+1)}{(z-1)} \quad (5)$$

This PI controller's discrete-time equation is obtained using bilinear transformation and given as,

$$i_{invref}(n) = i_{invref}(n-1) + \left(K_p + \frac{K_i T_s}{2} \right) V_e(n) + \left(\frac{K_i T_s}{2} - K_p \right) V_e(n-1) \quad (6)$$

In this equation, K_p and K_i represent proportional and integral gains, T_s is sampling time, $V_e(n)$ is voltage error and

iinvref is the final output of the PI controller-2. Here, the proportional and integral gains (K_p and K_i) of the PI controllers were determined using MATLAB's System Identification Toolbox and PID Tuner. For the PFC control unit, the open-loop system behavior was first analyzed in the simulation domain, and input-output data were collected. Mainly, for the PLL loop (PI Controller-1), the relationship between frequency error and phase angle was evaluated, while for the DC bus regulation loop (PI Controller-2), the duty ratio versus DC bus voltage characteristics were obtained. These datasets were processed using the System Identification Toolbox to derive the estimated transfer function models of both plants. The identified models were then supplied to MATLAB's PID Tuner, which computed optimal K_p and K_i values by shaping the closed-loop frequency response to achieve the desired gain and phase margins. The obtained gains were subsequently validated and fine-tuned in the simulation domain and then used for FPGA implementation.

These outputs of the voltage PI controller and PLL block along with other inputs received are processed by an efficient DBCC block. A digital DBCC technique is chosen here because of its advantages, including constant switching frequency, higher control bandwidth suited for active rectifiers, fast dynamic response, high accuracy and ease of digital implementation. This DBCC scheme achieves PF correction by ensuring that the current drawn from input grid is always synchronized with the grid voltage. To achieve this, first the reference current waveform is generated, which is in phase with the input grid voltage and its amplitude is proportional to the connected load power demands. Then the actual grid current is measured and compared with the reference current, and an error signal is calculated. This error signal is further used to compute the reference control signal for the PWM modulator. The generalized discrete-time equation of DBCC is given in Eq. (7). These discrete-time Eqs. (6) to (8) are derived in detail in Appendix.

$$V_{ref}(n) = -V_{ref}(n-1) + 2.V_{grid}(n) + K_1(i_{invref}(n) - i_{inv}(n-1)) + K_2(i_{invref}(n) + i_{inv}(n-1)) \quad (7)$$

Here, V_{grid} is input grid voltage, i_{invref} is output of the PI controller, i_{inv} is converter current, K_1 and K_2 are functions of input LCL filter inductance and PI gains. The stability and bandwidth of the proposed DBCC are determined by the placement of closed-loop poles in the z-domain, which is controlled through the coefficients K_1 and K_2 derived from the

converter's discrete-time model. Above DBCC equation relates the present control action to past and present current and voltage samples, enabling a one-step-ahead prediction of the required reference voltage. For stable operation, the closed-loop poles must lie within the unit circle, and this can be achieved by tuning K_1 and K_2 according to the converter dynamics and sampling period. In the ideal dead-beat case, the closed-loop pole is located at the origin, resulting in one-sample current tracking and the highest achievable loop bandwidth, theoretically approaching the Nyquist frequency. Increasing K_p (through K_1) shifts the pole toward the negative real axis, thereby increasing damping and enhancing transient robustness, whereas increasing K_i (through K_2) moves the pole toward the positive real axis, which reduces steady-state error but simultaneously decreases damping and narrows the bandwidth. Proper tuning of these gains ensures a fast dynamic response, minimal steady-state error, and a robust current loop for stable operation under varying grid and load conditions. Detailed pole-placement derivations and numerical analysis have been provided in the Appendix section.

The DBCC processes all these feedback, reference and input signals to generate a final reference signal, V_{ref} for the PWM modulator. The Sine-Triangle modulator block accordingly generates the exact control pulses (G1-G4) for the front-end active rectifier (AC-DC converter), to force the converter current to match the reference current in next 1 or 2 grid cycles and regulate DC bus voltage. Thus, the converter current is always in phase with input grid voltage and the DC bus voltage is also regulated. In all, the PF as well as DC bus voltage is regulated by this PFC control unit.

To regulate the DC-DC converter output voltage (V_{out}), the controller has to dynamically change the PWM duty ratio. Here, if the switching frequency remains unchanged then the ZVS is lost. Therefore, real-time tracking of the resonant frequency and corresponding duty ratio regulation are essential. These objectives are achieved by modifying PWM based on output voltage demand while simultaneously adjusting the converter's switching frequency to maintain soft switching conditions. To fulfil these requirements, a control strategy is designed comprising of two primary loops: resonant frequency tracking and output voltage regulation. The resonant frequency tracking loop includes a phase shifter and attenuator stage, a comparator, and an integrator block, as detailed in the study [33]. In this method, the load current $i_o(t)$ is sampled and passed through the phase shifter and attenuator block to produce an output signal $V_{psa}(t)$. The corresponding discrete-time equation is formulated using the Euler's explicit integration method and is presented in Eq. (8).

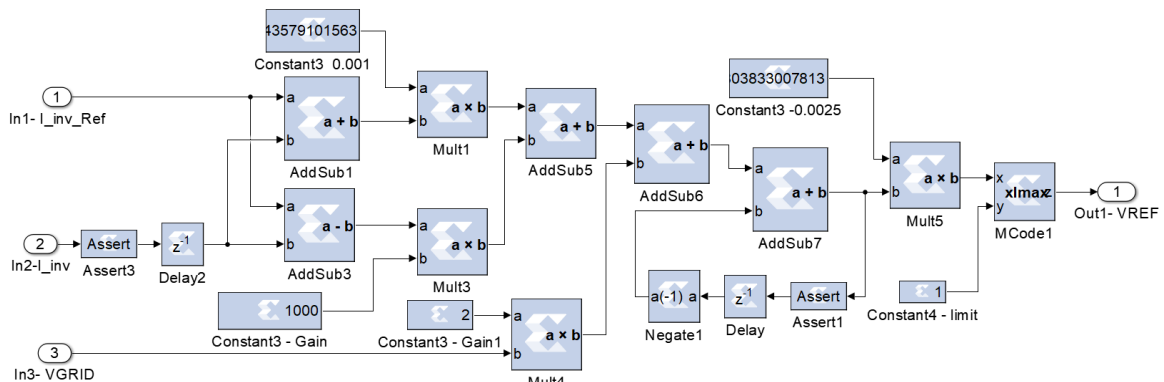


Figure 5. Dead-beat current control using XSG block sets

$$V_{psa}(n) = K_A \left(V_{psa}(n-1) + \frac{T_s}{\tau} [i_0(n) - V_{psa}(n-1)] \right) \quad (8)$$

Here, n is the current time step, K_A is an attenuation factor and τ is a time constant. This τ is a function of IGBT's output capacitance, switching frequency and peak load current. The output (V_{psa}) is further compared with load current, and a square wave is generated. This square wave has frequency, same as load current, but it always leads the load current and thus ensures ZVS of the resonant converter. The integrator stage processes this square wave and generates a ramp signal for the preceding PWM modulator block. Dynamic slope compensation logic discussed in the study [33] is implemented here to improve the performance of the resonant converter system.

In designing the voltage control loop, the output voltage (V_{out}) is initially measured and compared with a reference voltage (V_{ref}), generating an error signal (V_e). This voltage error is then processed and corrected using a discrete-time PI controller to maintain the desired output. Gains of the PI controller are tuned accordingly, using PID tuning methods discussed in the study [33] to achieve a required control action. Further, the PI output modifies the phase shift duty ratio of resonant converter using a PWM modulator block. The output from the PI controller is continuously compared with a ramp signal generated by the frequency tracking loop within the PWM modulator block. This comparison produces phase-shifted control pulses (G5-G8), which are then used to drive the corresponding switches (Q5-Q8) of LCC resonant converter.

Implementing entire control architecture on FPGA platform is challenging and time consuming, requiring skilled programming. Further, as the control complexity grows, even the experienced programmers face difficulties. To overcome these challenges, this work uses XSG, a model-based design technique, to generate HDL code for FPGA deployment. This approach offers several key benefits: (i) it facilitates rapid prototyping of control systems on FPGA, thereby reducing development cycles and accelerating time-to-market; (ii) it offers an integrated environment for both simulation and real-time testing on a single platform; (iii) simplifies design using XSG even for developers with basic HDL knowledge.

The implementation of DBCC controller using XSG blocks is depicted in Figure 5. In the same manner, quadrature filter, $\alpha\beta$ -dq0 transformation, PI-controller and all other blocks of resonant converter control unit (Figure 2) are implemented

using XSG block sets. In the overall design various logical, arithmetic, relational, DSP, control, mathematical operations, registers etc. are used. Here, MCode block is programmed so that the generated V_{ref} signal remains in the acceptable limits. For declaring user defined sample rates in delay and register blocks, the Assert blocks are used. To convert Boolean output into fixed-point data required by arithmetic blocks, cast block is used. Gateway-in and Gateway-out blocks are used to interface Simulink blocks with XSG blocks.

4. RESULTS AND DISCUSSION

To validate the functionality of the control strategy, the entire control system consisting of PFC control unit as well as resonant converter control unit is developed using XSG block sets. Simultaneously, the power converter stage for single-phase system (Figure 1) was developed in MATLAB-Simulink. Further, real-time testing and validation of control system is carried out by HIL simulation, as shown in Figure 6. In this setup, the power system model in MATLAB-Simulink is interfaced with control system developed in XSG, and via JTAG co-simulation interface the controller is implemented on FPGA board, i.e. Zynq-XC7Z020-1clg484 development board. In this case, the Simulink simulation environment with its XSG blocks, internally evokes the Vivado design suite software to generate HDL code (bit stream), which is indicated as JTAG co-simulation. Here, Xilinx JTAG co-simulation interface is used for HIL simulation due to its ease in implementation over the alternate point-to-point Ethernet co-simulation platform [39]. The JTAG interface enables seamless communication between the MATLAB-Simulink power system model and the FPGA-based control system, allowing accurate real-time testing and validation.

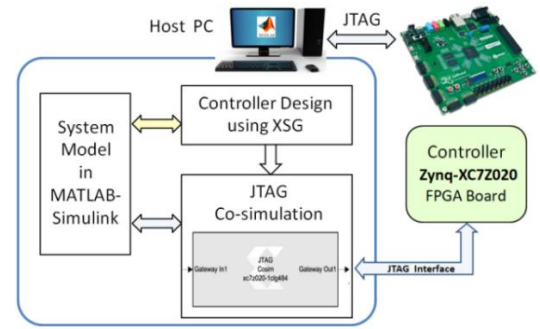


Figure 6. Schematic view of HIL simulation

Table 1. Specifications for the system under consideration

S. No.	Parameters	Values
1	Grid input specifications	230 V +/- 15% 50 Hz, AC, 15A
2	Input LCL filter parameters	Lin1 = Lin2 = 500 μ H, Cin1 = 100 μ F
3	IGBT rating	1.2 kV, 150 A
4	DC link capacitor	C1 = 100 μ F, 700 V
5	LCC Resonant Converter	Np/Ns = 4.0; Ls = 370 μ H; Cs = 0.22 μ F; Cp = 0.22 μ F; f0 = 25-30 kHz
6	Output Power Pmax	3000 W

Table 2. FPGA resource utilization

Resources	Hardware Cosim Wrapper and Interface	PFC Control Unit	DC-DC Converter Control Unit	Available	Utilization
BRAMs	2	0	0	140	2 (1.4%)
DSPs	0	168	44	220	212 (96.3%)
LUTs	1440	9839	2337	53200	13616 (25.6%)
Registers	1900	1407	1527	106400	4834 (4.5%)

This approach ensured rigorous testing of control system for both, PFC and resonant converter units in a simulated environment. The integration of MATLAB-Simulink, XSG blocks, and Vivado Design Suite streamlined the design, testing, and validation process, confirming the controller's functionality and robustness for real-world conditions. The PFC and resonant converter's power circuit specifications and parameters considered during HIL simulation are listed in Table 1. Here, input LCL filter values are designed to block higher order harmonics in the grid supply. Resonant converter's L and C are designed for resonating frequency in the range 25-30 kHz. IGBTs and DC bus capacitor ratings are kept on higher side to ensure safe operation for 3kW systems.

In all simulations, sampling time is set as $T_s = 0.1 \mu s$, FPGA clock frequency is 100 MHz, and maximum XSG blocks are set with fixed-point representation. This allows the interfacing and functioning of all sub-systems in the desired manner. The FPGA resources used for this implementation are summarized in Table 2. Here, it is observed that PFC controller needs more resources than the DC-DC converter controller. Further, the interface gateways are found to utilize 1900 registers, 1440 Look-up Tables (LUT) and 2 Block RAMs (BRAMs). It is also noted that, from the total available resources, 1.4% BRAMs, 96.3% DSPs, 25.6% LUTs, and 4.5% registers are used. Here, the current DSP utilization of 96.3% is indeed high and may pose potential risks such as limited scalability, reduced flexibility for feature expansion, timing challenges, and increased power and thermal stress. High resource usage can constrain future design extensions (e.g., adding control loops or monitoring functions) and make it difficult for the place-and-route tool to meet timing requirements, potentially leading to implementation failures. Although the present design performs reliably, future scalability can be improved through several optimization strategies: (i) HIL hierarchy optimization – it allows partitioning computational tasks by offloading less critical functions to the FPGA's soft-core processor while reserving DSPs for high-speed arithmetic operations. Additionally, implementing selected functions using LUTs and registers (fabric-based multiplication) can release DSP resources. (ii) Implementation optimization – by applying resource sharing and time-division multiplexing techniques to reuse DSP blocks efficiently. (iii) Algorithmic optimization – by simplifying complex mathematical operations with DSP-efficient logic formulations. These approaches can significantly reduce DSP utilization and enhance the design's scalability and reliability for future extensions. In all, the resource utilization summary ensures that the practical system with combined control of PFC and resonant converter can be implemented within a single FPGA board, Zynq-XC7Z020-lclg484.

The timing and power analysis report gives total power dissipation as 0.307 W, worst negative slack as 2.1 ns, hold slack as 0.073 ns and pulse width slack as 3.3 ns. The reported power dissipation (0.307 W) was obtained using Vivado's Power Analyzer tool, which estimates total power consumption based on the FPGA's resource utilization, clock frequency, and I/O switching activity. This includes both static and dynamic power components, and is generated post-synthesis and implementation. The estimation accounts for the actual FPGA architecture, routing, and real-time behavior of the designed controller, providing an accurate representation of its practical power performance. The timing analysis results ensure that the FPGA can be operated at increased speeds or frequencies without significant performance bottlenecks.

Moreover, by using the optimized XSG blocks in combination with customized IP cores, additional reductions in delays can be achieved. This level of optimization and performance enhancement is challenging to achieve with alternative hardware platforms, such as DSPs, microcontrollers and CPU based systems, making FPGA an ideal choice for this application.

To validate the functionality of the current control loop in PFC controller, the grid voltage and converter current drawn from the grid is monitored at rated load conditions. Here, the HIL simulation results demonstrate that the line current remains consistently in phase with the grid voltage, indicating proper synchronization between the two. Also, the line current wave shape is proper sinusoidal, as shown in Figure 7. This ensures that the unity PF is achieved. Achieving unity PF is important in power electronic systems, as it minimizes reactive power flow, improves system efficiency, and reduces losses in the power distribution network. The sinusoidal current waveform also indicates that the controller minimizes harmonic distortions and adheres to the grid compliance standards. This functionality is crucial for applications that need accurate power control and better power quality in grid-connected systems.

Further, to assess the dynamic performance of the PFC controller, a step change in the input grid voltage is applied, as illustrated in Figure 8. Here, the grid voltage is increased from standard 230 Vrms to 280 Vrms and DC bus voltage regulation was monitored at rated load condition. It was observed that, sudden increase in grid voltage overshoots the DC bus voltage from 300 V to 375 V. However, the system quickly stabilized, with the DC bus voltage returning to steady-state level of 300 V within just four grid cycles (80 ms), as shown in Figure 8.

This rapid settling time demonstrates the controller's effectiveness in handling voltage surges. Similarly, a sudden decrease in grid voltage showed momentary drop in DC bus voltage and settled down to set steady state level of 300 V in a few input cycles. These results ensure that the system remains stable and operational under dynamic grid conditions. Also, the observed response time is acceptable as the practical systems response time requirement is around 300 ms. This validates the robustness and efficiency of the PFC controller in maintaining voltage regulation and ensuring stable operation under transient grid events. Such performance is crucial for maintaining reliability in applications that require a stable DC bus voltage, even when the grid voltage fluctuates.

Further, the dynamic performance under output voltage and load resistance variation conditions is presented here to demonstrate the controller's effective voltage regulation and fast transient recovery under varying load scenarios. At first, the dynamic response of the proposed controller was evaluated under multiple step changes in the reference voltage, as shown in Figure 9. Initially, the reference was set to 60 V, and the controller successfully tracked this value, reaching steady state within 12 ms. At around 18 ms, the reference voltage was increased from 60 V to 120 V. The controller responded promptly, adjusting the duty ratio and smoothly elevating the output voltage to the new reference, achieving regulation with minimal overshoot and a short settling time (6 ms). Subsequently, at 30 ms, the reference was stepped down from 120 V to 30 V. Once again, the controller quickly adapted and brought the output voltage to the new steady state without oscillations in 10 ms. These results confirm the ability of the proposed controller to handle abrupt reference variations with fast transient recovery and stable steady-state performance.

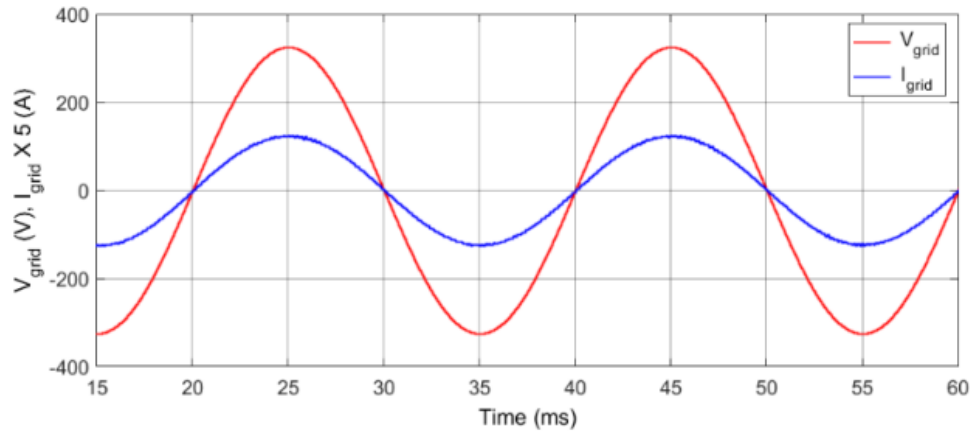


Figure 7. Single-phase grid voltage and line current wave shapes

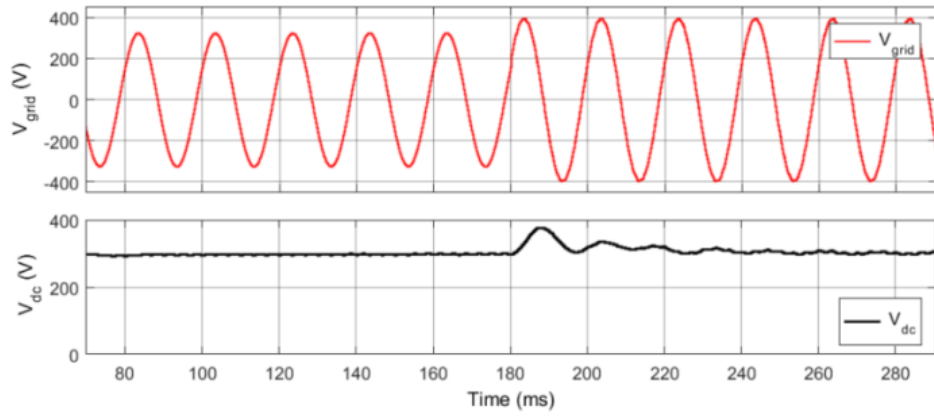


Figure 8. Performance evaluation of the control system under step transient at $V_{rms} = 280$ V

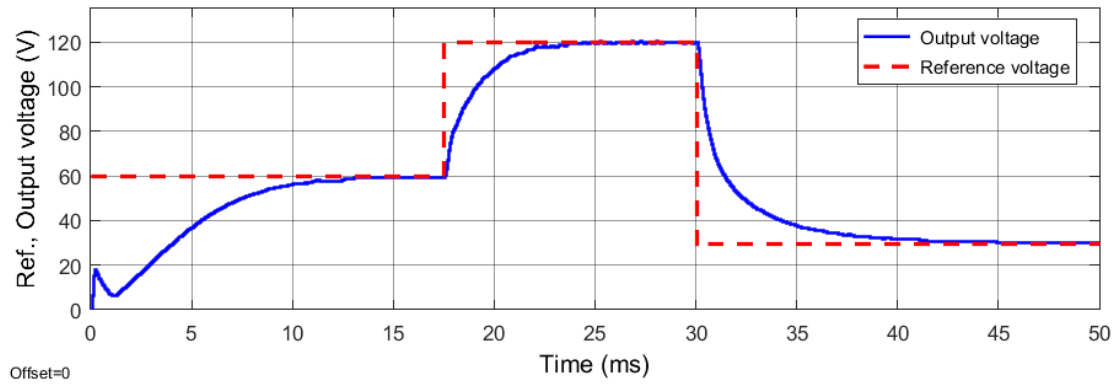


Figure 9. Output voltage response under step changes in reference voltage

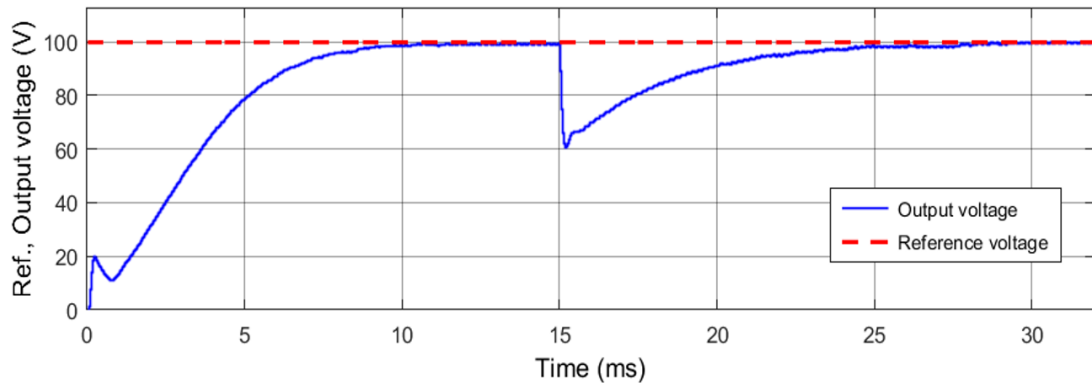


Figure 10. Output voltage response under load resistance variation

Further, the dynamic performance of the proposed controller was evaluated by subjecting the system to a sudden change in load resistance, while maintaining a constant reference voltage of 100 V. As shown in Figure 10, the controller initially tracks the reference, and the output voltage reaches steady state within 10 ms. At around 15 ms, the load resistance was abruptly varied, causing the output voltage to dip significantly below the reference (60 V). In response, the controller adjusted the duty ratio and restored the output voltage back to the reference 100 V within 12 ms. This demonstrates the controller’s ability to maintain regulation under abrupt load changes, ensuring stable output voltage recovery with minimal steady-state error.

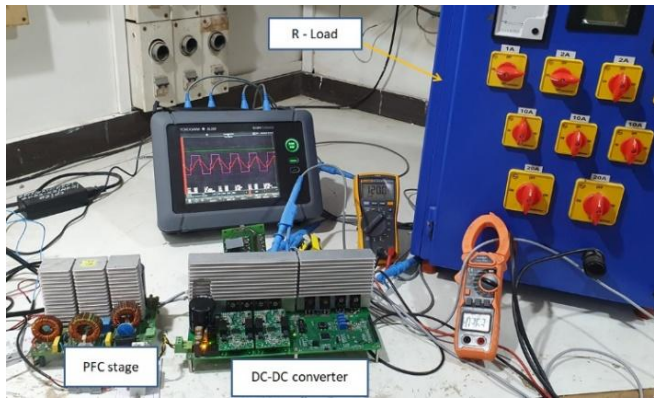


Figure 11. Laboratory testing set-up

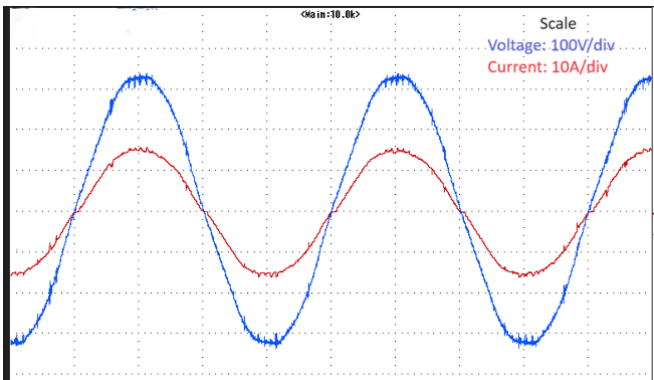


Figure 12. PFC input voltage and current waveforms at $P_{out}=3\text{ kW}$

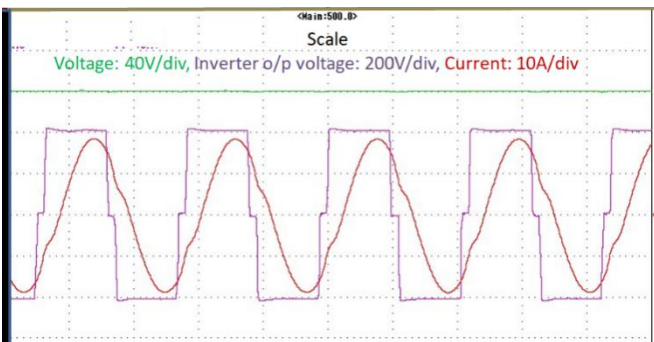


Figure 13. Resonant converter voltage and current waveforms and DC output voltage

To evaluate the functionality of the control system, a laboratory prototype of single-phase PFC stage driving a LCC resonant inverter based 300 V-120 V DC-DC converter is

developed, as illustrated in Figure 11. The system comprises an IGBT-based PFC boost converter, followed by an IGBT-based H-bridge DC-DC converter, a synchronous rectifier, an output filter, and a resistive load. Designed for a power rating of 3 kW, its detailed specifications are provided in Table 1. Here, the IGBT gating pulses generated from controller are passed through the level translator stage to obtain amplified 15V pulses needed by gate drivers. Also, the power section ground is electrically isolated from the controller and oscilloscope grounds using an isolator, safeguarding both the controller and oscilloscope against high-voltage transients and surge currents. Figure 12 shows the input AC voltage and current of the PFC boost converter at full loading condition. Here, the current wave shape is sinusoidal and in-phase with the input voltage wave shape, this justifies that a unity PF is achieved. Further, Figure 13 presents the output voltage and current waveforms of the resonant inverter at 3 kW power. Here, sinusoidal current lags the inverter output voltage, thus ensures ZVS. At the reduced output power level, the PWM duty ratio is reduced proportionally.

The HIL simulation and experimental results validate the practicality of the proposed control strategy and demonstrates the efficiency of its FPGA-based implementation. Moreover, with appropriate modifications to the isolation transformer turns ratio, PI controller parameters, and DC bus capacitance, the same design can be extended and validated for operation at higher output power levels.

5. CONCLUSIONS

The proposed PF correction control system has been developed and validated on reconfigurable FPGA board for the resonant inverter-based DC-DC converter application. This approach integrates both, PF correction and DC-DC converter control on a single digital platform (Zynq-XC7Z020-1clg484 FPGA), eliminating the need for two separate controllers, and thereby enhancing the reliability of the controller hardware. HIL simulation result shows that the DBCC technique has effectively maintained the input PF close to unity and regulated the DC bus voltage even in the fluctuating source conditions. Moreover, stable output voltage is maintained during dynamic load and voltage variations with fast transient recovery and minimal steady-state error. Timing and power analysis for implementation on Zynq board observed a total power dissipation of 0.307 W, with a worst negative slack of 2.1 ns, hold slack of 0.073 ns, and pulse width slack of 3.3 ns. These results ensure that the FPGA can be operated at an increased speed whereas the resource utilization table ensures that the practical system can be implemented using low-cost FPGA boards. This HIL simulation platform enables rapid prototyping and efficient hardware implementation of the controller on FPGA, thereby significantly reducing the overall time required for control strategy design and testing. The experimental results are comparable with the HIL simulation results; this demonstrates the effectiveness and reliability of the proposed control strategy. Moreover, this approach—featuring control strategy with inbuilt PF correction mechanism can be readily used with minor modifications, for identical DC-DC converter applications such as EV/Hybrid EV charging, telecom rectifiers, server power supply, and photovoltaic systems.

Future work will focus on extending the proposed controller to multi-phase and three-phase PFC systems for higher power

levels, implementing the design in a custom ASIC or SoC to enhance integration and efficiency, and validating the approach through full-scale hardware testing to demonstrate its scalability for industrial applications.

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APPENDIX

Eq. (6) – DC bus voltage regulation (PI controller-2)

Continuous time transfer function of PI controller is,

$$H(s) = K_p + \frac{K_i}{s}$$

Here, K_p & K_i are proportional and integral gains. Its Z domain representation using bilinear transformation is,

$$\begin{aligned} H(z) &= K_p + \frac{K_i T_s}{2} \frac{1+z^{-1}}{1-z^{-1}} \\ &= \frac{K_p (1-z^{-1}) + \frac{K_i T_s}{2} (1+z^{-1})}{1-z^{-1}} \end{aligned}$$

$$= \frac{\left(K_p + \frac{K_i T_s}{2}\right) + \left(-K_p + \frac{K_i T_s}{2}\right) z^{-1}}{1 - z^{-1}}$$

Now PI controller's input is $V_e(n)$ and output is $I_{invref}(n)$ therefore,

$$H(z) = \frac{I_{invref}(z)}{V_e(z)}$$

Taking inverse Z-transformation gives,

$$i_{invref}(n) - i_{invref}(n-1) = \left(K_p + \frac{K_i T_s}{2}\right) v_e(n) + \left(-K_p + \frac{K_i T_s}{2}\right) v_e(n-1)$$

$$i_{invref}(n) = i_{invref}(n-1) + \left(K_p + \frac{K_i T_s}{2}\right) v_e(n) + \left(\frac{K_i T_s}{2} - K_p\right) v_e(n-1)$$

Eq. (7) - Discrete-time equation of DBCC

For boost PFC converter, the inductor current dynamics are given by,

$$L \frac{di_{inv}(t)}{dt} = V_{ref}(t) - V_{grid}(t)$$

Here,

L is the input filter inductance,

$i_{inv}(t)$ is the inductor (input) current,

$V_{ref}(t)$ is the converter output (modulator reference),

$V_{grid}(t)$ is the input grid voltage.

Using the bilinear transformation,

$$s = \frac{2}{T_s} \frac{1-z^{-1}}{1+z^{-1}}$$

The transfer function from $(V_{ref} - V_{grid})$ to i_{inv} is,

$$G(s) = \frac{1}{Ls} \xrightarrow{\text{Bilinear}} G(z) = \frac{T_s}{2L} \frac{1+z^{-1}}{1-z^{-1}}$$

$$i_{inv}(z) = \frac{T_s}{2L} \frac{1+z^{-1}}{1-z^{-1}} [V_{ref}(z) - V_{grid}(z)]$$

Multiplying both sides by $(1 - z^{-1})$ gives the difference equation in time domain:

$$i_{inv}(n) - i_{inv}(n-1) = \frac{T_s}{2L} [V_{ref}(n) - V_{grid}(n) + V_{ref}(n-1) - V_{grid}(n-1)]$$

Evaluating above equation at index $(n+1)$ gives,

$$i_{inv}(n+1) - i_{inv}(n) = \frac{T_s}{2L} [V_{ref}(n+1) - V_{grid}(n+1) + V_{ref}(n) - V_{grid}(n)]$$

Enforce dead-beat target $i_{inv}(n+1) = i_{invref}(n)$ and solve for $V_{ref}(n+1)$:

$$V_{ref}(n+1) = -V_{ref}(n) + 2V_{grid}(n+1) + \frac{2L}{T_s} [i_{invref}(n) - i_{inv}(n)]$$

Relabel indices $n+1 = n$ for notation simplification and align measurements so the measurable past $i_{inv}(n-1)$ is used in computation. The base dead-beat term then becomes,

$$V_{ref}(n) = -V_{ref}(n-1) + 2V_{grid}(n) + \frac{2L}{T_s} [i_{invref}(n) - i_{inv}(n-1)]$$

Now to add a discrete corrective term, implement a discrete PI on the current error $e(n) = i_{invref}(n) - i_{inv}(n)$ using the trapezoidal rule. This incremental PI output to be added to V_{ref} is,

$$\Delta u_{PI}(n) = K_p e(n) + K_i \frac{T_s}{2} (e(n) + e(n-1)),$$

Here, K_p and K_i are the PI gains. Writing $\Delta u_{PI}(n)$ in terms of i_{invref} and i_{inv} gives,

$$\Delta u_{PI}(n) = K_p (i_{invref}(n) - i_{inv}(n)) + \frac{K_i T_s}{2} ((i_{invref}(n) - i_{inv}(n)) + (i_{invref}(n-1) - i_{inv}(n-1)))$$

Now considering both, implementation approximations $i_{inv}(n) \approx i_{inv}(n-1)$ for the most recent measurable current (one-sample computation delay), and approximate $i_{invref}(n-1) \approx i_{invref}(n)$ as the reference is computed earlier in the control chain. With these, the PI increment simplifies to a form depending on $i_{invref}(n)$ and $i_{inv}(n-1)$:

$$\Delta u_{PI}(n) \approx K_p (i_{invref}(n) - i_{inv}(n-1)) + \frac{K_i T_s}{2} (i_{invref}(n) + i_{inv}(n-1))$$

Now combining both, the base dead-beat term and above PI correction give,

$$V_{ref}(n) = [-V_{ref}(n-1) + 2V_{grid}(n) + \frac{2L}{T_s} (i_{invref}(n) - i_{inv}(n-1))] + [K_p (i_{invref}(n) - i_{inv}(n-1)) + \frac{K_i T_s}{2} (i_{invref}(n) + i_{inv}(n-1))]$$

By grouping the like terms on the differences and the sum gives,

$$V_{ref}(n) = -V_{ref}(n-1) + 2V_{grid}(n) + K_1 (i_{invref}(n) - i_{inv}(n-1)) + K_2 (i_{invref}(n) + i_{inv}(n-1))$$

Here,

$$K_1 = \frac{2L}{T_s} + K_p \text{ and } K_2 = \frac{K_i T_s}{2}$$

In this equation, sum term arises explicitly from trapezoidal integration of the PI action – it is the discrete integral contribution $\frac{K_i T_s}{2} (e[n] + e[n-1])$ and becomes $\frac{K_i T_s}{2} (i_{invref}(n) + i_{inv}(n-1))$ after timing approximations. The difference term contains both the plant inversion factor $\frac{2L}{T_s}$ (dead-beat) and the PI proportional action K_p . The approximations $i_{inv}(n) \approx i_{inv}(n-1)$ and $i_{invref}(n-1) \approx i_{invref}(n)$ reflect typical one-sample computation delays.

Z-Domain Stability Analysis –

Continuous inductor dynamics,

$$L \frac{di_{inv}(t)}{dt} = v_{ref}(t) - v_{grid}(t)$$

Bilinear discretization of the plant (Z-domain) is,

$$I(z) = \frac{T_s}{2L} \frac{1+z^{-1}}{1-z^{-1}} [V(z) - V_{grid}(z)]$$

Rearranged to express V in terms of I gives,

$$V(z) = \frac{2L}{T_s} \frac{1-z^{-1}}{1+z^{-1}} I(z) + V_{grid}(z)$$

Taking Z-transform of DBCC equation with V_{grid} kept separate,

$$(1+z^{-1})V(z) = (K_1 + K_2)I_{ref}(z) + (K_2 - K_1)z^{-1}I(z) + 2V_{grid}(z)(1+z^{-1})/2$$

For small-signal closed-loop pole analysis, set $V_{grid}(z) = 0$ and $I_{ref}(z) = 0$ (for the homogeneous equation.) then left-hand side simplifies as,

$$(1+z^{-1})V(z) = \frac{2L}{T_s} (1-z^{-1}) I(z).$$

Collect terms in $I(z)$ (homogeneous case $I_{ref} = 0$):

$$\left(\frac{2L}{T_s} (1-z^{-1}) - (K_2 - K_1) z^{-1} \right) I(z) = 0$$

The characteristic equation (set bracket = 0). Multiply by z to remove negative powers,

$$\frac{2L}{T_s} (z-1) - (K_2 - K_1) = 0.$$

Closed-loop pole p is therefore

$$p = z = 1 + \frac{K_2 - K_1}{2L/T_s} = 1 + \frac{T_s}{2L} (K_2 - K_1)$$

By substitute $K_1 = \frac{2L}{T_s} + K_p$ and $K_2 = \frac{K_i T_s}{2}$, the closed form of p simplifies to

$$p = \frac{K_i T_s^2}{4L} - \frac{K_p T_s}{2L}$$

Ideal dead-beat corresponds to choosing the plant-inverse term only (no extra PI): $K_p = 0$, $K_i = 0 \Rightarrow K_1 = \frac{2L}{T_s}$, $K_2 = 0$. Substituting into above equation gives

$$p = 0$$

i.e. the pole is at the origin and the closed-loop mapping from reference to current is a pure one-sample delay (exact dead-beat).

Stability condition - The discrete closed-loop is stable when the pole lies strictly inside the unit circle:

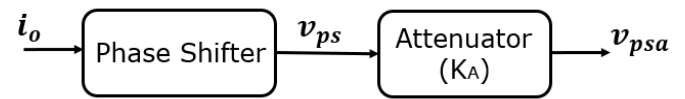
$$|p| < 1 \Rightarrow \left| \frac{K_i T_s^2}{4L} - \frac{K_p T_s}{2L} \right| < 1$$

This inequality gives the allowable region for K_p, K_i (for given T_s, L values).

Eq. (8) - Phase shifter and attenuator stage

Phase shifter is a basic RC network with single pole, and its transfer function is written as,

$$G(s) = \frac{1}{\tau s + 1}$$



Phase shifter's input is load current (i_o) and it generates phase shifted output (v_{ps}), therefore continuous time transfer function is,

$$G(s) = \frac{V_{ps}(s)}{I_o(s)} = \frac{1}{\tau s + 1}$$

Taking inverse Laplace transform,

$$\tau \frac{dv_{ps}(t)}{dt} + v_{ps}(t) = i_o(t)$$

Rearranging and discretizing using Euler's explicit integration gives,

$$\frac{v_{ps}(n) - v_{ps}(n-1)}{T_s} = \frac{i_o(n) - v_{ps}(n-1)}{\tau}$$

Here, use input sample $i_o(n)$ and previous output $v_{ps}(n-1)$ on the righthand side of equation,

$$v_{ps}(n) = v_{ps}(n-1) + \frac{T_s}{\tau} \{i_o(n) - v_{ps}(n-1)\}$$

Here, n – current time step

T_s – sampling time

τ – time constant of phase shifter block

The attenuation block has attenuation factor K_A , therefore final output (v_{psa}) is,

$$v_{psa}(n) = K_A v_{ps}(n)$$

$$v_{psa}(n) = K_A \left(v_{psa}(n-1) + \frac{T_s}{\tau} \{i_o(n) - v_{psa}(n-1)\} \right)$$