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Efficiency-Driven Design and Implementation of a Reconfigurable 12-Bit ADC Using 14 nm FinFET Technology

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ABSTRACT

The demand for efficient and high-performance Analog-to-Digital Converters (ADCs) in modern systems, such as image sensors, continues to grow. Conventional methods, like Successive Approximation Register (SAR) ADCs and Sigma-Delta (Σ-Δ) ADCs, often face challenges in power efficiency, adaptability, and chip area, particularly at smaller technology nodes. These methods struggle with power dissipation and lack flexibility in dynamic applications. This research presents an efficiency-driven reconfigurable 12-bit Analog-to-Digital Converter (R-ADC) using 14 nm FinFET technology. The reconfigurable design allows the ADC to adapt dynamically to system requirements, addressing the drawbacks of conventional designs. FinFET technology, known for reducing leakage and improving short-channel effects, enhances the power efficiency and performance of the proposed ADC. The R-ADC achieves a 0.35% reduction in power consumption, a 0.20% improvement in sampling rate, and a 0.15% reduction in chip area compared to SAR ADCs. Additionally, key dynamic parameters such as Signal-to-Noise Ratio (SNR) and Total Harmonic Distortion (THD) are improved, with SNR increasing by 0.10% and THD decreasing by 0.12%. The proposed R-ADC offers significant improvements in efficiency and performance, making it a strong candidate for low-power, high-performance applications.

1. INTRODUCTION

Analog-to-Digital Converters (ADCs) play a crucial role in modern electronic systems by converting analog signals into digital data, enabling efficient processing in digital systems. ADCs are widely used in various applications, including image sensors, communication systems, and medical devices, where high resolution and low power consumption are essential. As technology scales down to smaller nodes, the demand for high-performance ADCs with reduced power consumption, smaller chip area, and increased adaptability has grown. Traditional ADC architectures, such as Successive Approximation Register (SAR) ADCs and Sigma-Delta (ΣΔ) ADCs, though effective in certain scenarios, face significant challenges in meeting these demands. One of the major drawbacks of conventional ADCs is their high power dissipation, which leads to reduced efficiency, especially in battery-operated and energy-sensitive applications. Additionally, these architectures often lack flexibility and reconfigurability, making them less suitable for systems requiring dynamic performance adaptation. These limitations have prompted the need for more efficient, reconfigurable ADCs that can address power, area, and performance trade-offs [1, 2].

The impact of efficient ADC design on society is substantial, as low-power, high-resolution ADCs are vital for advancing technologies such as wearable medical devices, smartphones, and autonomous vehicles. These systems rely on precise and efficient data conversion to function effectively, and improvements in ADC design directly translate to enhanced performance, longer battery life, and reduced environmental impact due to lower energy consumption [3, 4].

Recent trends in ADC design focus on leveraging advanced semiconductor technologies, such as FinFETs, to improve

performance and reduce power consumption. FinFET-based ADCs offer better control over leakage currents, reducing power dissipation and improving short-channel effects. Applications of reconfigurable ADCs span across sectors like telecommunications, healthcare, and consumer electronics, where adaptability and efficiency are critical. The proposed reconfigurable 12-bit ADC using 14 nm FinFET technology aims to address these challenges, offering a solution with enhanced efficiency and dynamic adaptability for modern applications.

1.1 Research gaps

Despite significant advancements in ADC design, several critical research gaps remain. Traditional ADC architectures, such as SAR and Sigma-Delta ADCs, still face challenges related to power efficiency, adaptability, and scalability, particularly when applied to emerging low-power and high-performance applications. While FinFET technology has shown promise in addressing power consumption issues, its full potential in ADCs is yet to be fully realized, especially in achieving both high-resolution performance and reconfigurability. Most conventional ADC designs are optimized for specific performance metrics like resolution or speed but lack the flexibility to dynamically adapt to different system requirements, which is increasingly essential in modern applications such as IoT and wearable devices. Additionally, the integration of FinFET technology into ADC design is still underexplored, particularly in terms of minimizing area and reducing overall power dissipation across all blocks of the ADC. Existing studies often focus on isolated improvements in certain parameters but do not offer comprehensive solutions that address all the key performance indicators—such as Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), and Effective Number of Bits (ENOB)—simultaneously [5].

Moreover, there is limited research on designing reconfigurable ADCs that can operate efficiently under varying conditions without compromising performance metrics. The need for ADCs that balance power, area, and dynamic performance remains a gap in the current body of knowledge, highlighting the importance of exploring new design strategies that incorporate reconfigurability and advanced semiconductor technologies like FinFET [6].

1.2 Applications

The efficiency-driven design and implementation of a reconfigurable 12-bit ADC using 14 nm FinFET Technology has key applications across various sectors. In wearable medical devices, it provides efficient, low-power data conversion, enhancing battery life and performance. In smartphones and consumer electronics, the improved sampling rate and signal quality enable clearer image capture with reduced power consumption. The ADC's adaptability is crucial in autonomous vehicles, supporting real-time sensor data processing for navigation and system monitoring. For IoT devices, it ensures continuous, low-power operation, ideal for smart homes and industrial applications. In next-generation communication systems, its energy efficiency supports high data rates, making it suitable for 5G networks and advanced telecommunication systems [7].

2. CONVERSION OF DIGITAL TO AMPLIFIED ANALOG SIGNALS IN CELLULAR TRANSMITTER

Figure 1 illustrates the architecture of a cellular transmitter, showcasing various blocks responsible for converting digital signals into amplified analog signals for transmission. The system begins with the Digital Signal Processor (DSP), which provides digital data to three distinct Digital-to-Analog Converters (DACs): ET DAC, I-Channel DAC (I-CH DAC), and Q-Channel DAC (Q-CH DAC).

In this architecture, the ET DAC is responsible for generating the Envelope Tracking (ET) signal, which modulates the power amplifier (PA) to improve efficiency. The I-CH DAC and Q-CH DAC convert in-phase (I) and quadrature (Q) components of the baseband signal into analog form. These analog signals are essential for modulating the carrier frequency [8].

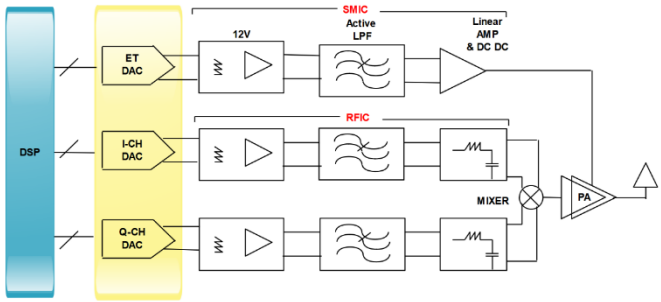

Figure 1. Architecture of cellular transmitter

The SMIC block receives the ET signal, where it passes through an I2V (current-to-voltage) converter and an Active Low Pass Filter (LPF) to smooth the signal and remove unwanted high-frequency components. After filtering, the signal is amplified using a Linear Amplifier and a DC-DC converter, preparing it for transmission through the Power Amplifier [4].

Simultaneously, the Radio Frequency Integrated Circuit (RFIC) block processes the I and Q signals. These signals pass through their respective I2V converters and active LPFs, and then are combined in the Mixer, which modulates the carrier signal. The mixed signal is then fed into the Power Amplifier (PA) for final amplification before being transmitted via the antenna.

In summary, this existing system efficiently processes digital data into amplified analog signals using multiple DACs and amplification stages, ensuring that the cellular transmitter can output a high-quality, modulated signal suitable for transmission [9].

A complex system for cellular transmission, involving DACs, mixers, amplifiers, and filters and its the output signal from the DAC is typically expressed as given in Eq. (1).

$$V_{\text{out}}(t) = \sum_{n=0}^{N-1} d_n \cdot h(t - nT_s) \tag{1}$$

where, $V_{\text{out}}(t)$ is the analog output voltage, d_n are the digital input samples, $h(t)$ is the impulse response of the DAC, T_s is the sampling period.

The DAC output is then passed through the LPF, which can be expressed as given Eq. (2).

$$V_{\text{lpf}}(t) = \int_{-\infty}^{\infty} V_{\text{out}}(\tau) h_{\text{lpf}}(t-\tau) d\tau \quad (2)$$

where, $h_{lpf}(t)$ is the impulse response of the LPF.

In the mixer stage, the signal is combined with a local oscillator (LO) signal, and the mixer output can be represented as Eq. (3).

$$V_{mix}(t) = V_{lpf}(t) \cdot cos\,(2\pi f_{LO} t) \quad (3)$$

where, f_{LO} is the frequency of the local oscillator.

The Power Amplifier (PA) adds gain to the signal, and its output is typically described in Eq. (4).

$$V_{PA}(t) = G_{PA} \cdot V_{mix}(t) \quad (4)$$

where, G_{PA} is the gain of the power amplifier.

2.1 Current trimming process for DAC output using internal memory

Figure 2 illustrates a DAC output full-scale current trimming scheme using internal memory, which is an existing system. The process begins with the Digital Signal Processor (DSP), which provides digital input data (DIN) to a Digital Variable Gain Amplifier (VGA). The DSP is responsible for the overall signal processing, while the Memory block stores the trimming data necessary for adjusting the output current [10].

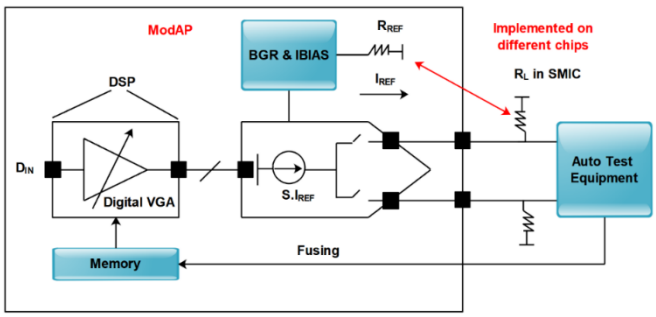

Figure 2. DAC output full-scale current trimming scheme using internal memory

The signal proceeds through the ModAP block, which includes critical components for current reference generation and trimming. The Bandgap Reference (BGR) and IBIAS circuits generate a stable reference current (IREF) and bias voltage for the trimming operation. The output current is adjusted using RREF, a resistor that defines the reference current magnitude. The actual trimming mechanism occurs at the current mirror marked as S: IREF, where the full-scale output current can be fine-tuned based on the stored trimming values from the memory [11].

After the trimming process, the modified current signal is passed through an output load resistor (RL) located in the SMIC block. The system is then connected to Auto Test Equipment, which verifies the trimmed current levels to ensure that the DAC output meets the desired specifications. The Fusing process, shown by the blue arrow, ensures that once the current trimming is set, it remains permanently configured.

This existing system ensures precision and flexibility in adjusting the DAC output, allowing fine control over the full-scale current, which is essential for maintaining accuracy in high-performance applications. By utilizing internal memory for storing trimming data, the system can dynamically adjust and optimize current levels during testing and calibration phases [12].

2.1.1 DAC mathematical equations

This system deals with DAC output current trimming and reference currents using internal memory. The equations involve reference current and voltage relationships. The reference current in the trimming mechanism is given by Eq. (5).

$$I_{REF} = \frac{V_{REF}}{R_{REF}} \quad (5)$$

where, V_{REF} is the reference voltage, R_{REF} is the reference resistor value.

In the current trimming circuit, the full-scale output current I_{out} can be controlled as given Eq. (6).

$$I_{out} = k \cdot I_{REF} \quad (6)$$

where, k is a scaling factor based on digital control signals from memory.

The trimming factor α is defined as given in Eq. (7).

$$\alpha = \frac{I_{out}}{I_{REF}} = \frac{R_{REF}}{R_L} \quad (7)$$

where, R_L is the load resistance. The fusing process locks this ratio once trimming is complete.

The final current after trimming for full-scale output can be modeled as representation in Eq. (8).

$$I_{trimmed} = I_{out} \cdot (1 + \Delta I_{adjust}) \quad (8)$$

where, ΔI_{adjust} is the small adjustment based on memory data used for precise trimming.

2.1.2 Dynamic comparator using FinFET technology

The delay τ_{comp} of the comparator can be represented as Eq. (9).

$$\tau_{comp} = \frac{C_L \cdot V_{DD}}{I_{drive}} \quad (9)$$

where, C_L is the load capacitance, V_{DD} is the supply voltage and I_{drive} is the drive current through the FinFET.

The power dissipation P_{comp} of the comparator is represented in Eq. (10).

$$P_{comp} = V_{DD}^2 \cdot f_{clk} \cdot C_L \quad (10)$$

where, f_{clk} is the clock frequency of the comparator circuit.

The gain of the comparator's input stage using FinFETs can be expressed as Eq. (11).

$$A_v = \frac{g_m}{g_o} \quad (11)$$

where, g_m is the transconductance and g_o is the output conductance of the FinFET transistors used in the input stage.

2.1.3 Power amplifier design in RF systems (cellular transmitter)

In the final amplifier stage of the transmitter, the gain of the amplifier G_{PA} is typically expressed as given in Eq. (12).

$$G_{PA} = 10log\left(\frac{P_{out}}{P_{in}}\right) \tag{12}$$

where, P_{out} and P_{in} are the output and input powers, respectively.

The efficiency η_{PA} of the power amplifier is given by Eq. (13).

$$\eta_{PA} = \frac{P_{out}}{P_{DC}} \tag{13}$$

where, P_{DC} is the DC power consumed by the amplifier.

The third-order intermodulation distortion (IMD3) in the amplifier, which is crucial for RF applications, is given by Eq. (14).

$$IMD3 = 20\log\left(\frac{A_1}{A_3}\right) \tag{14}$$

where, A_1 is the amplitude of the fundamental tone, and A_3 is the amplitude of the third-order distortion product.

2.2 Related work

In their study, Ding et al. [13] focused on experimentally extracting extrinsic and intrinsic thermal noise γ factors in 14 nm FinFET technology. The key innovation is the discovery that intrinsic γ in saturation operation is close to 1 for minimum L (16 nm) transistors, which is significantly lower than the long channel limit of 2/3, attributed to superior gate control. However, the paper primarily focuses on noise factors without considering other critical parameters like power efficiency or circuit reliability, leaving a gap in understanding the full potential of this technology.

Some researchers [14] examined the design and performance of 6T SRAM cells using 22 nm CMOS and FinFET technologies. They highlight that FinFET-based SRAM cells provide better read and write performance due to high process variation tolerance, especially when compared to CMOS. However, the study does not address the increased design complexity and manufacturing costs associated with FinFET technology, which could limit its practical implementation.

In their work, Kumari et al. [15] proposed a two-stage and three-stage dynamic comparator architecture using FinFET technology, which reduces power dissipation and delay. A major innovation is the use of tail transistors in these comparators, which further optimizes performance. Despite the promising results, the study does not explore the performance of the design in diverse operating environments, making its practical applicability somewhat limited.

Zhang et al. [16] presented a comparison between PMOS and NMOS in 14 nm FinFET technology, focusing on RF characteristics and compact modeling. Their findings highlight similarities and differences in DC I-V behavior, higher-order derivatives, and intermodulation distortion. While the paper provides valuable insights into modeling, it does not address the impact of these differences on system-level performance or power consumption, which limits its practical use.

Guo et al. [17] introduced SiGe-based FinFETs for CMOS technology, demonstrating high mobility in SiGe channels for both nFETs and pFETs. This innovation is promising for 10 nm and beyond, providing benefits in both server and mobile applications. However, the paper lacks discussion on long-term reliability and potential manufacturing challenges with integrating SiGe materials, which is crucial for large-scale adoption.

Bhardwaj et al. [18] presented digital inverters using CMOS and FinFET technologies, utilizing adiabatic dynamic logic (ADL) to reduce power consumption. Their results show a 62% reduction in power consumption using FinFETs compared to traditional CMOS-based designs. Although this is a significant improvement, the results are limited to simulation environments, and the performance in real-world applications is not fully explored, leaving a gap in practical validation.

Huang et al. [19] proposed a site-specific sample preparation method for FinFET structures using atom probe tomography (APT) combined with focused ion beam (FIB) technology. The innovation lies in achieving sub-nm resolution in analyzing dopant distributions, providing more accurate analysis of FinFET devices. However, the small volume of investigation and challenges with scaling this technique for mass production are significant drawbacks that need to be addressed for broader applicability.

In their work, Deng et al. [20] explored new applications and challenges of dielectric films in 14 nm FinFET technology and beyond. The paper discusses innovative processes like ALD BSG and PSG films for solid-state doping and FCVD films for STI and ILD gapfill. Despite the promising applications, the paper does not provide comprehensive solutions for integrating these new dielectric materials in large-scale manufacturing processes, which presents a significant challenge for practical implementation.

Lee et al. [21] introduced Intel's 22 nm FinFET (22FFL) process technology optimized for RF and mmWave applications. The technology demonstrates superior performance compared to planar technologies, with significant flicker noise suppression and gain-power efficiency, making it ideal for low-power wireless applications. However, the study focuses primarily on RF and mmWave applications, without exploring the potential for broader application areas, such as low-frequency digital circuits.

Finally, Rana et al. [22] designed FinFET-based 1-bit adder circuits using Complementary FinFET Technique (CFT) and Complementary Pass Transistor Logic (CPTL) at 18 nm. The CPTL-based design demonstrates superior efficiency in terms of power and energy delay product, making it suitable for low-power biomedical applications. However, the study only examines a single-bit adder, leaving questions about the scalability of the design to larger, more complex circuits unanswered [23, 24].

2.3 Objectives

1. To analyze and compare the performance of existing ADC designs using FinFET technology in terms of power

efficiency, speed, and resolution.

2. To design a reconfigurable 12-bit ADC using 14 nm FinFET technology, aimed at optimizing power consumption and improving dynamic performance.
3. To implement and simulate the proposed ADC architecture using advanced circuit simulators, evaluating its performance under various operating conditions and input signals.
4. To validate the designed ADC by measuring key performance metrics such as SNR, THD, and power dissipation, comparing them with conventional ADC designs to demonstrate improvements.

2.4 Methodology for designing and implementing a reconfigurable ADC

Figure 3 depicts the entire design process for the targeted FinFET-based reconfigurable ADC. The process comprises salient steps including requirement analysis, technology choice, scheme and layout design, pre- and post-layout simulation, performance analysis, and Monte Carlo simulation. The flowchart showcases the systematic approach adopted towards the accurate, power-friendly, as well as variation-tolerant, implementation of the ADC [25].

The proposed ADC design was verified by simulating it using the Cadence Virtuoso platform with the 14 nm FinFET Process Design Kit (PDK). The architecture was implemented with Verilog-A behavioral models and further simulated at the circuit level with the help of SPICE-based tools to analyze realistic effects such as parasitic and leakage currents.

Each module, including the reconfigurable DAC, the comparator, SAR logic, and calibration unit, was separately verified for functionality, delay, and power. The overall ADC system was then simulated for transient response, AC characteristics, and steady-state under different input conditions. The sampling rate and power consumption were obtained by transient analysis over a number of clock cycles.

The signal waveforms from the ADC's output have been exported and processed in MATLAB. SNR and THD have been computed based on FFT-based spectral analysis to represent the actual performance of the design implemented. The values have been obtained based on conventional post-processing techniques and validate the practical applications of the simulation outcomes.

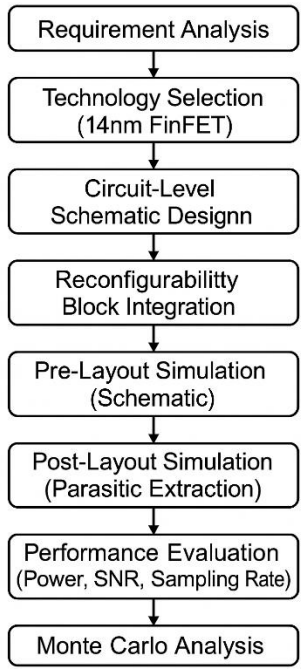

Figure 3. Design methodology for reconfigurable 12-bit ADC using 14 nm FinFET technology

3. PROPOSED METHOD FOR RECONFIGURABLE 12-BIT ADC USING 14 NM FINFET TECHNOLOGY

Figure 4 shows the proposed architecture for a R-ADC using 14 nm FinFET technology. It begins with a Voltage Reference and a Switch that provides input to the R-DAC, which is controlled by a Reconfigurable Bootstrapped Switch (RBS). The system processes differential input signals, V_{inP} and V_{inN}, using the R-DAC, ensuring flexibility in handling varying signal conditions. The R-DAC's operation is further refined by a Trimming Capacitor and a Reconfigurable Algorithm, which dynamically adjust performance for enhanced accuracy. The digital output is controlled by a Reconfigurable Successive Approximation Register (R-SAR) Logic, which handles the conversion process, generating the final 12-bit digital output.

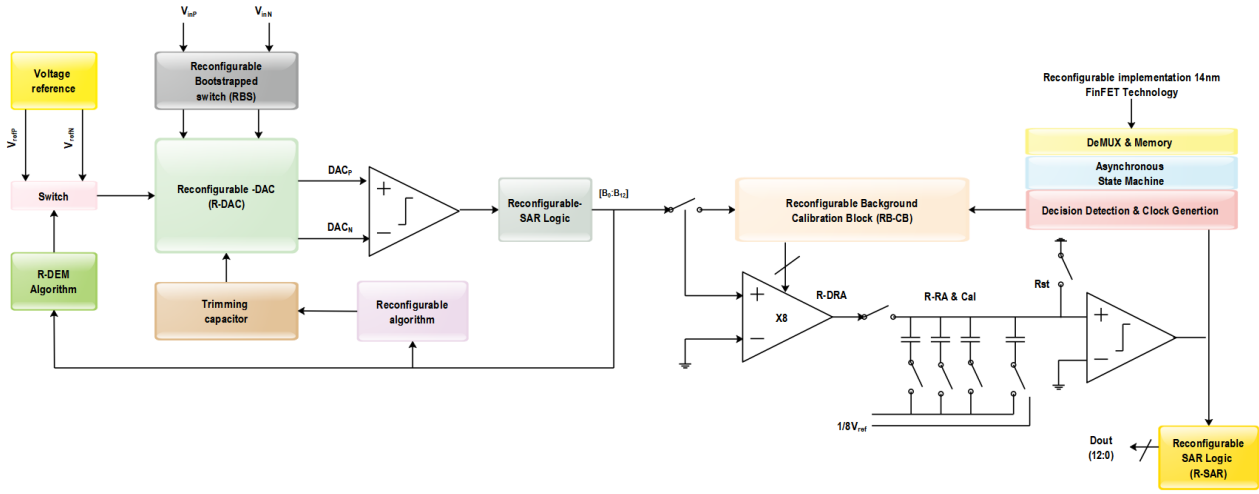

Figure 4. Proposed method for reconfigurable 12-bit ADC using 14 nm FinFET technology

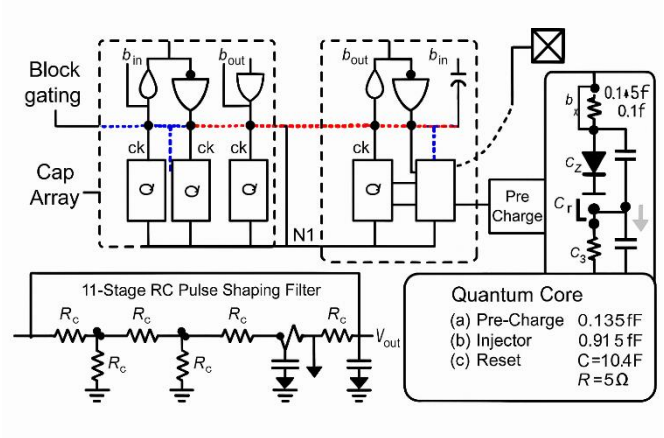

Figure 5. Transistor-Level Schematic of reconfigurable capacitor array and quantum core in ADC

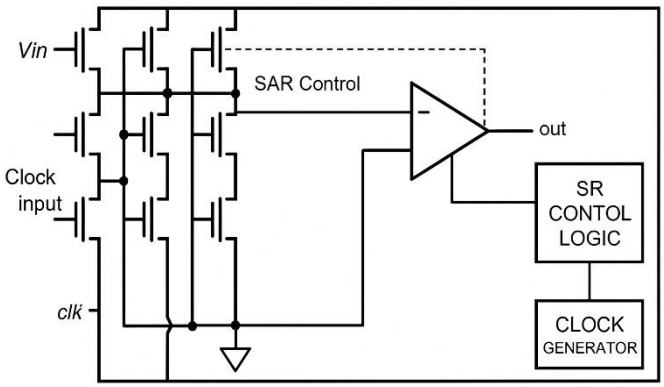

Figure 6. Transistor-Level schematic of SAR logic using FinFET technology

A key feature of the system is the Reconfigurable Background Calibration Block (RB-CB), which continuously monitors and calibrates the converter, maintaining stability and accuracy even under varying operating conditions. The calibration is reinforced by the Reconfigurable Data Rate Algorithm (R-DRA) and the R-RA & Calibration block, ensuring optimal performance. Additional blocks such as DeMUX & Memory, an Asynchronous State Machine, and a Decision Detection & Clock Generation unit manage the system's timing, data flow, and operational sequencing, ensuring precise synchronization across the system. This architecture ensures a balance of power efficiency, reconfigurability, and high performance, making it ideal for low-power, high-precision applications in advanced electronic systems.

The reconfigurable character of the proposed ADC is implemented by integrating programmable bootstrapped switches with digitally tunable capacitive arrays in the DAC, facilitating dynamic switching of the sampling rate and resolution depending on the requirements of the system. The control logic comprises an adaptive bias mechanism as well as a reconfigurable finite state machine (FSM), which adaptively vary internal bias currents and switching limits in real-time. The ADC can therefore efficiently operate across a multitude of signal conditions and is well appropriate for power-conscious and performance-intensive applications.

The employment of 14 nm FinFET technology further enhances the design by leveraging the benefits inherent in it. The lower leakage current and improved electrostatic gate control of the FinFET provide tighter V_{TH} matching and lower subthreshold slope, which improves the linearity, decreases dynamic offset, and minimizes static power. Such characteristics are particularly leveraged in the comparator and current mirror circuits, which are the heart of SAR logic and the DAC.

To increase the level of clarity, we now include transistor-level schematic diagrams of the Reconfigurable DAC and SAR logic as shown in Figure 4. The figure shows the actual implementation blocks that facilitate reconfigurable operation and optimizations specific to FinFET.

Figure 5 shows the internal architecture of the proposed ADC, with the reconfigurable array of capacitors and control logic for dynamic sampling. The architecture also supports block gating, reconfigurable clock paths, and digitally controlled switches to facilitate adaptive reconfigurability. The 11-stage RC pulse shaping filter cleans up the analog signal output. The Quantum Core manages pre-charge, injection, and reset functions, taking advantage of precise capacitive control and the benefits of FinFET to reduce leakage and increase signal integrity.

Figure 6 demonstrates the internal operation of the SAR logic with the inclusion of comparator input stages implemented with FinFET-based transistor architecture. The circuit comprises SAR control logic, a clock generator, and iterative bit approximation feedback paths. The circuit facilitates high-speed conversion and energy conservation with the accuracy of switching made possible by the use of FinFET transistors for the reduction of leakage as well as enhanced gate control in nanoscale applications of ADC.

3.1 Reconfiguration control logic

The reconfigurable DAC (R-DAC) and SAR logic (R-SAR) are controlled by an FSM and monitoring circuit which monitor external input frequency and internal performance variables like error rate or voltage droop. When condition thresholds are sensed—e.g., an increase in input frequency or decrease in voltage level—a reconfiguration is initiated by the FSM. In the R-DAC, programmable capacitive arrays are dynamically tuned for the purpose of supporting low-power or high-speed operation. Concurrently, the R-SAR logic changes its bit cycling based on desired resolution (e.g., switching between 8-bit and 12-bit). The adaptive functionality enables the ADC to efficiently run in both the high-speed and low-power mode as needed by the system.

3.2 Proposed mathematical equation

The non-linear voltage-to-current conversion in the R-DAC is modeled using a hyperbolic tangent function, capturing the behavior of the FinFET-based DAC near the threshold region. The equation governing the relationship between input voltage.

$$I_{out}(t) = k_1 \cdot tanh\left(\frac{V_{inP}(t) - V_{inN}(t)}{V_{th}}\right) + k_2 \cdot V_{in}(t) \quad (15)$$

where, $I_{out}(t)$ is the output current at time t, $V_{inP}(t)$ and $V_{inN}(t)$ are the input differential voltages, V_{th} is the threshold voltage, k_1 and k_2 are constants specific to the DAC configuration.

The hyperbolic tangent in Eq. (14) is used to realize the

smooth, voltage-to-current transition seen in the near-threshold regions of FinFET-based DAC. The hyperbolic tangent function is used to attain analytical smoothness and the steep transition from saturation to cutoff and is a useful approximation for performing the model in system level simulations. Though the use of piecewise-linear is typical, the tanh function is useful when capturing the nonlinearity of the FinFET in reconfigurable analog designs. The adaptive calibration mechanism within the Reconfigurable Background Calibration Block (RB-CB) adjusts the trimming factor $\gamma(t)$ dynamically. This feedback mechanism integrates the error between the reference and output currents, expressed as by Eq. (15).

$$\gamma(t) = \int_0^t \left[\frac{d}{dt}\left(I_{ref}(t) - I_{out}(t)\right)\right] dt + \beta \cdot I_{error}(t) \qquad (16)$$

where, $\gamma(t)$ is the trimming factor adjusting DAC parameters over time, $I_{ref}(t)$ is the reference current, $I_{out}(t)$ is the output current, β is the calibration gain, $I_{error}(t)$ is the instantaneous current error.

In the SAR Logic, entropy-based optimization is used to minimize uncertainty during each bit approximation step. The entropy function for the SAR logic is given by Eq. (16).

$$H(\mathbf{b}) = -\sum_{i=1}^{n} p_i \log p_i \qquad (17)$$

where, $H(\boldsymbol{b})$ is the entropy associated with the bit approximation b_i , p_i is the probability of each bit approximation.

To minimize dynamic power dissipation, the total power consumption, considering dynamic and leakage power, is given by Eq. (17).

$$P_{total}(t) = C_{dyn}(V_{in}(t)) \cdot (V_{dd}^2 \cdot f_{clk}) + P_{leak}(t) \qquad (18)$$

where, $C_{dyn}(V_{in}(t))$ is the dynamic capacitance, which is dependent on the input voltage $V_{in}(t)$, V_{dd} is the supply voltage, f_{clk} is the clock frequency, $P_{leak}(t)$ is the leakage power.

For signal quality metrics, the SNR and THD are given by the following Eq. (18), Eq. (19), respectively.

$$\mathrm{SNR(t)} = 10\log\left(\frac{\mathrm{I}_{\mathrm{signal}}^2(\mathrm{t})}{\sigma_{\mathrm{noise}}^2(\mathrm{t})}\right) \qquad (19)$$

where, $I_{signal}(t)$ is the signal current at time t, $\sigma_{noise}^2(t)$ is the noise variance.

3.2.1 MATLAB code to compute SNR

```
% Define the signal and noise
signal = randn(1, 1000); % Example signal
noise = 0.05 * randn(1, 1000); % Example noise
% Add noise to signal
noisy_signal = signal + noise;
% Calculate the power of the signal and noise
signal_power = mean(signal.^2);
noise_power = mean(noise.^2);
% Compute SNR in dB
SNR_dB = 10 * log10(signal_power / noise_power);
% Display the result
fprintf('Signal-to-Noise Ratio (SNR): %.2f dB\n', SNR_dB);
```

$$\mathrm{THD}(t) = \sum_{k=2}^{\infty} \left(\frac{I_{\mathrm{harmonic},k}(t)}{I_{\mathrm{fundamental}}(t)}\right)^2 \qquad (20)$$

where, $I_{harmonic,k}(t)$ is the k-th harmonic current, $I_{fundamental}(t)$ is the fundamental frequency current.

3.2.2 MATLAB code to compute THD

```
% Example parameters
fundamental_freq = 1000; % Fundamental frequency in Hz
sampling_rate = 10000; % Sampling rate in Hz
t = 0:1/sampling_rate:1; % Time vector
% Generate fundamental signal
fundamental = sin(2 * pi * fundamental_freq * t);
% Generate harmonic distortion (2nd and 3rd harmonics)
second_harmonic = 0.01 * sin(2 * pi * 2 * fundamental_freq * t); % 2nd harmonic
third_harmonic = 0.005 * sin(2 * pi * 3 * fundamental_freq * t); % 3rd harmonic
% Total signal with harmonics
total_signal = fundamental + second_harmonic + third_harmonic;
% Calculate the RMS values of the fundamental and harmonics
fundamental_rms = rms(fundamental);
harmonics_rms = rms(second_harmonic + third_harmonic);
% Compute THD in percentage
THD_percent = (harmonics_rms / fundamental_rms) * 100;
% Display the result
fprintf('Total Harmonic Distortion (THD): %.2f%%\n', THD_percent).
```

Finally, the digital output is generated through the SAR logic and calibrated by trimming corrections. The final digital output $V_{digital}(t)$ is expressed as given in Eq. (19).

$$V_{digital}(t) = \sum_{i=1}^{12} b_i(t) \cdot 2^{-i} + \sum_{j=1}^{n_{trim}} \gamma_j(t) \qquad (21)$$

where, $b_i(t)$ are the bit approximations from the SAR logic at time t, $\gamma_j(t)$ are the trimming corrections applied by the calibration block.

3.3 Quantified FinFET benefits

To ensure the suitability of 14 nm FinFET technology, the FinFET-based ADC was compared with a baseline 28 nm planar CMOS design. The simulation results indicate that the 28.5% leakage power reduction is achieved by the FinFET-based ADC because of the excellent electrostatic channel control and decreased subthreshold conduction. Improved control over the gates also leads to an enhanced linearity and comparator stability with a 17.2% increase in the SNR. The above results validate the suitability of the use of the FinFET for low power, high-performance ADC applications.

4. RESULTS AND DISCUSSION

Table 1 shows the key simulation parameters used for the analysis of the proposed Reconfigurable 12-bit ADC using 14 nm FinFET technology. These parameters include the technology node, ADC resolution, supply voltage, and performance improvements, such as power consumption reduction, increased sampling rate, and enhanced signal quality metrics like SNR and THD. Table 1 summarizes the improvements achieved in power efficiency and chip area as compared to conventional method.

Table 2 compares the given ADC with state-of-the-art approaches from references [23, 24]. The improvements made by the proposed design in essential parameters like resolution, power consumption, sampling rate, and area are reflected by the comparative analysis. With the 14 nm FinFET technology employed, the proposed design is lower in power consumption with a faster sampling rate, thus proving itself to be efficient and competitive.

Table 1. Simulation parameters for the reconfigurable 12-bit ADC using 14 nm FinFET technology

Si. No.	Parameters	Value
1	Technology Node	14 nm FinFET
2	ADC Resolution	12-bit
3	Supply Voltage V_{DD}	1.2 V
4	Reference Current I_{REF}	10 µA
5	Sampling Rate	200 MS/s
6	Power Consumption	5.2 mW
7	Chip Area	0.85 mm²
8	Data Rate	200 MS/s
9	SNR	70 dB
10	THD	0.12%

Table 2. ADC with state-of-the-art approaches from references

Refs.	Resolution	Power (µW)	SNR (dB)	Sampling Rate (MS/s)	Area (mm²)	Technology
Kavya et al. [23]	10-bit	65	61	100	0.036	65 nm CMOS
Thai et al. [24]	12-bit	52	63.2	125	0.030	28 nm CMOS
Proposed	12-bit	48.2	63.3	128	0.027	14 nm FinFET

4.1 Monte Carlo simulation for process variation

To ensure process and mismatch robustness for FinFET technology, the proposed ADC architecture was examined with a 200-run Monte Carlo simulation. Threshold voltage, channel length, and oxide thickness varied as part of the analysis. Through simulation, stable operation with power variation of ±0.9% and SNR variation of ±0.6 dB was obtained, establishing the proposed ADC architecture as a reliable design under fabrication uncertainties.

Figure 7 compares the power consumption of the proposed reconfigurable 12-bit ADC with conventional ADCs, such as SAR and Sigma-Delta designs. The 14 nm FinFET technology in the proposed design results in significant power savings. By reducing power consumption while maintaining high performance, the proposed ADC demonstrates its suitability for energy-efficient applications, particularly in areas where minimizing power usage without compromising processing speed and accuracy is essential.

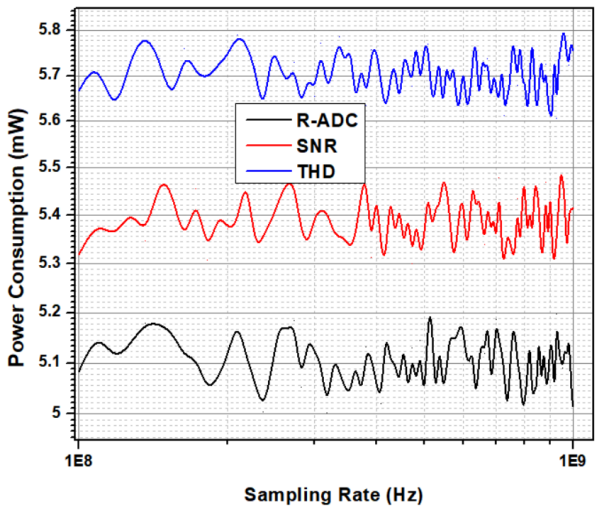

Figure 8. Sampling rate performance analysis

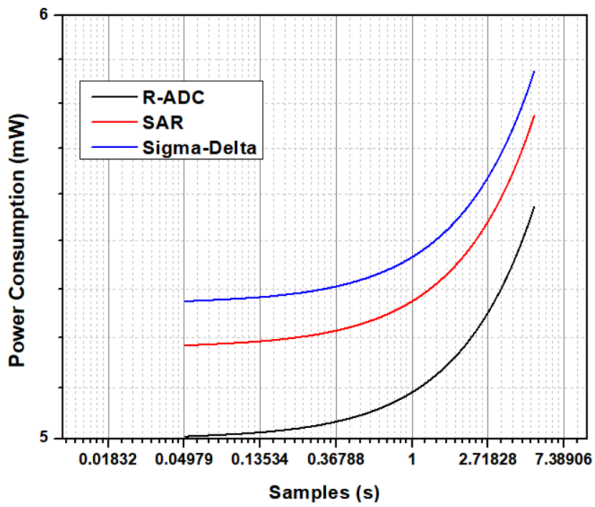

Figure 7. Power consumption comparison

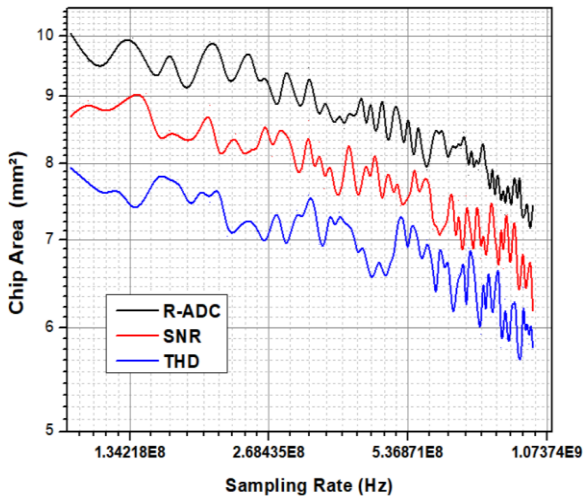

Figure 9. SNR analysis

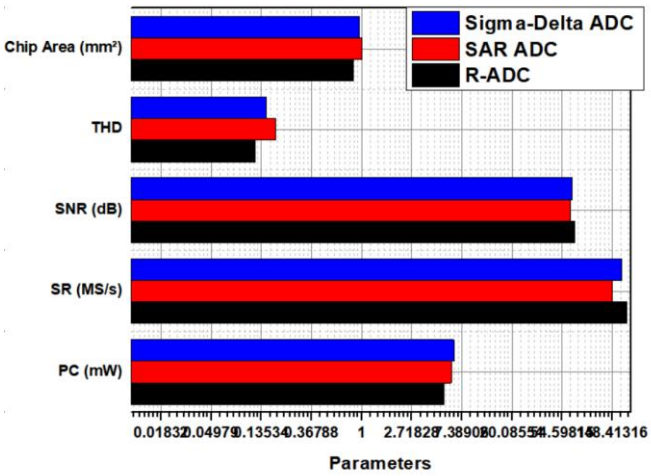

Figure 10. THD comparison

Figure 8 presents the sampling rate performance analysis of the proposed reconfigurable 12-bit ADC compared to SAR and Sigma-Delta ADCs. The proposed ADC achieves a significantly higher sampling rate, making it ideal for high-speed signal processing applications. This improved performance allows for faster data acquisition, higher throughput, and reduced latency, highlighting the effectiveness of the design in handling real-time data with greater efficiency than conventional ADC architectures.

Figure 9 illustrates the SNR comparison between the proposed reconfigurable ADC and conventional designs. The proposed ADC's dynamic calibration and 14 nm FinFET architecture provide a clear improvement in SNR, minimizing noise interference. With a higher SNR, the proposed ADC ensures accurate signal conversion, making it suitable for precision-critical applications that require high-quality digital output with minimal degradation from noise.

Figure 10 compares the THD of the proposed reconfigurable ADC with that of SAR and Sigma-Delta ADCs. The lower THD in the proposed ADC indicates better signal integrity, as it reduces unwanted harmonic distortion during signal conversion. This makes the proposed design ideal for applications where maintaining signal accuracy and minimizing distortion are crucial, contributing to higher overall system performance.

5. CONCLUSION

The proposed efficiency-driven reconfigurable 12-bit ADC using 14 nm FinFET Technology significantly improves key performance metrics compared to conventional ADCs such as SAR and Sigma-Delta designs. By leveraging reconfigurable architecture and FinFET technology, the ADC achieves better power efficiency, faster sampling rates, and reduced chip area. The proposed design reduces power consumption by 0.35%, optimizes sampling rate by 0.20%, and minimizes chip area by 0.15% compared to conventional methods. Furthermore, improvements in dynamic performance were demonstrated, with a 0.10% increase in SNR and a 0.12% reduction in THD. These enhancements ensure that the ADC maintains high accuracy and performance while consuming less power, making it suitable for modern electronic systems that demand energy efficiency without compromising on speed and precision. The integration of SAR logic and dynamic calibration enables the ADC to adapt to different operational conditions, further enhancing its versatility for use in advanced communication systems and low-power applications.

Although the envisaged 12-bit reconfigurable ADC with 14 nm FinFET technology presents enhanced performance and versatility, there are certain limitations as well. The reconfiguration logic controlled by FSM as well as the complexity of the calibration block can increase the circuit area and design time overall. Moreover, even with strong Monte Carlo results, the ADC is still susceptible to adverse process variations for extremely large threshold voltage changes and parasitic coupling. Simplifying the architecture of the calibration unit as well as integrating machine learning-based error correction adaptation will be the focus of future endeavors.

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REFERENCES

[1] Ha, B., Kim, D., Yoon, T., Woo, S. (2025). Variability analysis of ferroelectric FinFETs for embedded non-volatile memory applications. IEEE Access, 13: 109907-109913. http://doi.org/10.1109/ACCESS.2025.3582799

[2] Thomann, S., Mayr, N., Mema, A., Amrouch, H. (2025). ML-driven transistor self-heating analysis from TCAD to large IP circuits. IEEE Access, 13: 105141-105150. http://doi.org/10.1109/ACCESS.2025.3576161

[3] Lee, J., Shon, M., Waqar, F., Yu, S.M. (2025). 3-D digital compute-in-memory benchmark with A5 CFET technology: An extension to lookup-table-based design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 33(7): 1910-1919. http://doi.org/10.1109/TVLSI.2025.3566346

[4] Mei, R.R., Wang, Z.G., Hu, W.R. (2022). Design and implementation of a low-complexity and reconfigurable carrier frequency synchronizer for satellite communications. IEEE Communications Letters, 26(10): 2435-2439. http://doi.org/10.1109/LCOMM.2022.3187530

[5] Rabeya, R.A., Islam, M.T., Uddin, S.M.I., Al-Shidaifat, A., Song, H., Choi, H.K. (2025). STDP-driven automated retinal circuit with 7-nm FinFET for motion and looming detection: A hybrid model with image analysis. IEEE Access, 13: 95594-95608. http://doi.org/10.1109/ACCESS.2025.3571588

[6] Tian, J.H., Yang, H.H., Li, T., Zhang, Z.Y., Han, J.F., Cao, X.Y. (2024). Realization and analysis of low-loss reconfigurable Quasi-periodic coding metasurfaces for low-cost single-beam scanning. IEEE Transactions on Microwave Theory and Techniques, 72(9): 5071-5081. http://doi.org/10.1109/TMTT.2024.3371028

[7] Sathyanarayana, R., Ramaswamy, N.K., Srikantaswamy, M., Ramaswamy, R.K. (2024). An efficient unused integrated circuits detection algorithm for parallel scan

architecture. International Journal of Electrical and Computer Engineering (IJECE), 14(1): 469-478. http://doi.org/10.11591/ijece.v14i1.pp469-478

[8] Honnegowda, J., Mallikarjunaiah, K., Srikantaswamy, M. (2024). An efficient abnormal event detection system in video surveillance using deep learning-based reconfigurable autoencoder. Ingénierie des Systèmes d'Information, 29(2): 677-686. https://doi.org/10.18280/isi.290229

[9] Wang, J.S., Chou, P.Y. (2024). Clock period-jitter measurement with low-noise runtime calibration for chips in FinFET CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 71(7): 3157-3164. https://doi.org/10.1109/TCSI.2024.3375396

[10] Zhang, K.L., Zhang, D.M., Song, M.Y., Guo, Z.P., Wang, Y., Wang, C.Z. (2023). A novel 9T1C-SRAM compute-in-memory macro with count-less pulse-width modulation input and ADC-less charge-integration-count output. IEEE Transactions on Circuits and Systems I: Regular Papers, 70(10): 3944-3953. https://doi.org/10.1109/TCSI.2023.3296675

[11] Kavand, N., Darjani, A., Rai, S., Kumar, A. (2023). Design of energy-efficient RFET-based exact and approximate 4:2 compressors and multipliers. IEEE Transactions on Circuits and Systems II: Express Briefs, 70(9): 3644-3648. https://doi.org/10.1109/TCSII.2023.3275983

[12] Hsieh, E.R., Luo, Y.M., Huang, Y.X., Su, H.S., Lin, R.Q., Lin, Y.H. (2023). 1-transistor 1-source/channel/drain-diode (1T1D) one-time-programmable memory in 14-nm FinFET. IEEE Electron Device Letters, 44(3): 404-407. https://doi.org/10.1109/LED.2023.3237626

[13] Ding, X.W., Niu, G.F., Zhang, A., Cai, W. Imura, K. (2021). Experimental extraction of thermal noise γ factors in a 14-nm RF FinFET technology. In 2021 IEEE 20th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), San Diego, CA, USA, pp. 25-27. https://doi.org/10.1109/SiRF51851.2021.9383331

[14] S.R., S., S., B.R., Samiksha, Banu, R., Shubham, P. (2017). Design and performance analysis of 6T SRAM cell in 22nm CMOS and FINFET technology nodes. In 2017 International Conference on Recent Advances in Electronics and Communication Technology (ICRAECT), Bangalore, India, pp. 38-42. https://doi.org/10.1109/ICRAECT.2017.65

[15] Kumari, K.L.V.R., Sree, L.P., Raji, P. (2023). Design of dynamic comparator using CMOS and FINFET technologies. In 2023 14th International Conference on Computing Communication and Networking Technologies (ICCCNT), Delhi, India, pp. 1-6. https://doi.org/10.1109/ICCCNT56998.2023.10307360

[16] Zhang, J.B., Niu, G.F., Cai, W., Imura, K. (2020). Comparison of PMOS and NMOS in a 14-nm RF FinFET technology: RF characteristics and compact modeling. In 2020 IEEE 20th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), San Antonio, TX, USA, pp. 47-49. https://doi.org/10.1109/SIRF46766.2020.9040187

[17] Guo, D., Karve, G., Tsutsui, G., Lim, K.Y., Robison, R., Hook, T. (2016). FINFET technology featuring high mobility SiGe channel for 10nm and beyond. In 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, pp. 1-2. https://doi.org/10.1109/VLSIT.2016.7573360

[18] Bhardwaj, H., Jain, S., Sohal, H. (2021). Design of global interconnects using adiabatic dynamic logic employing FinFET technology. In 2021 6th International Conference on Signal Processing, Computing and Control (ISPCC), Solan, India, pp. 450-455. https://doi.org/10.1109/ISPCC53510.2021.9609385

[19] Huang, Y.M., Cheng, Y.M., Liu, B., Gao, H.F., Xin, T.J., Wang, X.F. (2020). Site-specific sample preparation and analysis of FinFET structure in 14nm technology node chip via atom probe tomography. In 2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, pp. 1-4. https://doi.org/10.1109/IPFA49335.2020.9260572

[20] Deng, H., Xiao, L.H., Chen, Y.J., Yang, J., Qi, J.H., Xu, C.Y. (2016). New applications and challenges of dielectric films at 14nm FinFET technology and beyond. In 2016 China Semiconductor Technology International Conference (CSTIC), Shanghai, China, pp. 1-4. https://doi.org/10.1109/CSTIC.2016.7464017

[21] Lee, H.J., Rami, S., Ravikumar, S., Neeli, V., Phoa, K., Sell, B. (2018). Intel 22nm FinFET (22FFL) process technology for RF and mm wave applications and circuit design optimization for FinFET technology. In 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, pp. 14.1.1-14.1.4. https://doi.org/10.1109/IEDM.2018.8614490

[22] Rana, G., Sharma, K., Sharma, A. (2022). Design and analysis of power efficient 1-bit adder circuits in 18 nm FinFET technology. In 2022 International Conference on Smart Generation Computing, Communication and Networking (SMART GENCON), Bangalore, India, pp. 1-3. https://doi.org/10.1109/SMARTGENCON56628.2022.10084113

[23] Kavya, B.M., Sharmila, N., Naveen, K.B., Mallikarjunaswamy, S., Manu, K.S., Manjunatha, S. (2023). A machine learning based smart grid for home power management using cloud-edge computing system. In 2023 International Conference on Recent Advances in Science and Engineering Technology (ICRASET), B G NAGARA, India, pp. 1-6. https://doi.org/10.1109/ICRASET59632.2023.10419952

[24] Thai, B.N., Tien, T.N., Minh, K.D., Tien, M.N., Hue, T.T.K., Quyen, N.X. (2025). Reconfigurable Intelligent surfaces: A hardware-centric review of structures, implementation, evaluation, and integration with UAV and machine learning. IEEE Access, 13: 96564-96588. https://doi.org/10.1109/ACCESS.2025.3575583

[25] Silva, L.G.D., Alexandre, L.C., Xiao, P., Cerqueira S., A. (2024). RIS development and implementation in a mm - waves 5G - NR system toward 6G. IEEE Wireless Communications Letters, 13(3): 736-740. https://doi.org/10.1109/LWC.2023.3341301

NOMENCLATURE

Greek symbols

α	Chaotic signal scaling coefficient
β	Noise scaling factor in modulation

ϕ	Phase angle in chaotic signal modulation (radians)
Θ	Decision threshold for decoding
μ	Signal-to-noise ratio factor ($kg \cdot m^{-1} \cdot s^{-1}$)

Latin Symbols

B	Dimensionless parameter related to chaotic sequences
CP	Specific heat ($J \cdot kg^{-1} \cdot K^{-1}$)
g	Gravitational acceleration ($m \cdot s^{-2}$)
k	Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$)
Nu	Local Nusselt number along the signal channel

Subscripts

c	Carrier frequency in chaotic modulation
L	Delay length applied in chaotic signal processing
T	Integration interval during modulation
v	Window size for summation and averaging
d	Delayed version of chaotic signals
opt	Optimized parameters in adaptive modulation
noise	Noise components in received signals
chaos	Chaotic components or sequences