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High-Gain, Low-Noise, and Wide Bandwidth CMOS Transimpedance Amplifier Design for Next-Generation Optical Communication Systems

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ABSTRACT

The Transimpedance Amplifier (TIA) configuration using CMOS technology is pivotal in modern analogue circuit design, especially in high-speed and low-noise applications. This proposed configuration integrates PMOS and NMOS transistors to improve bandwidth, gain, and power efficiency. In the designed CMOS Transimpedance Amplifier (TIA), the circuit uses complementary transistor pairs to drive the output. The main advantage of this configuration is its ability to provide low output impedance while maintaining high bandwidth. The design arrangement reduces distortion and enhances linearity by supporting positive and negative fluctuations well. This is critical in applications such as optical receivers, where high-speed signal processing is required. The gain of the Transimpedance Amplifier is determined by the feedback resistor connected between the output and the inverting input of the amplifier, and by operating the proposed system, a gain of 64 dB is obtained. The Transimpedance gain is adjusted to balance speed and noise performance. The gain-bandwidth quotient (GBP) of 10 GHz is a critical parameter for typical CMOS TIA designs. The gain-bandwidth quotient reflects the ability of an amplifier to maintain high gain while providing a wide frequency response. TIAs designed for high-speed applications often target GBP values in the multi-GHz range, ensuring the amplifier can handle high-frequency signals with minimal attenuation. The proposed system is designed and simulated in LT-Spice.

1. INTRODUCTION

The fast proliferation of communication services drives the demand for low-cost, high-speed networks. By the 2020s, fiber optic communication will be the most preferred option for high data transmission due to its potential utility in various high data applications, including radio over fiber, Ethernet, and the Internet of Things. In addition, compared to wireless and coaxial cables, linked communication systems have numerous benefits, like preventing electrical ground loops and insensitivity to spurious noise signals [1-3]. For radio frequency devices operating at high frequencies, the shrinking size of CMOS technology presents challenges, including power leakage issues and parasitic effects mentioned [4]. MOS amplifiers are frequently found in mixed-signal and analog circuits and systems. Because it affects the performance of the entire chain, the TIA is the primary critical building block given each function in the optical receiver [5, 6]. Consequently, any performance improvement necessitates careful study of the TIA design. The gain bandwidth product of the TIA is connected to its figure of merit (FoM) [3].

Enough bandwidth and sufficient gain must be obtained for high-speed applications to satisfy the goal data rate while achieving a high FoM. Nonetheless, the difficult goal is to complete a TIA design with a suitable tradeoff between all performances by considering the other noise-related difficulties, minimal cost, and low power consumption. Composed of a photodiode (PD), a transimpedance amplifier (TIA), and a limiting amplifier (LA) (Figure 1) [7]. The PD sensor converts the original electrical form of optical information into current signals. Current signals are amplified and converted into voltage signals by the TIA step in the interim. To obtain the required threshold signal in the receiver chain, the LA must do one more amplification [8-10]. Because of its low cost, fast speed, low power consumption, and continuous scalability, employing such a system in the complementary metal oxide semiconductor (CMOS) process is becoming more attractive due to advancements in fabrication technology.

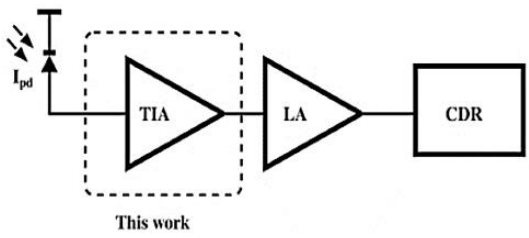

Figure 1. System of optical receivers

The TIA stage amplifies and converts the input current to voltage, while the LA stage supplies further gain [7].

These receiver systems are implemented in various

technologies, including bipolar, SiGe, BiCMOS, CMOS, and GaAs [11, 12]. Whenever CMOS technologies are employed, a few things may need to be considered. The TIA and LA phases are intended to function at high speeds to start. Secondly, there is a dominant pole at the input node caused by the enormous parasitic capacitance of the photodiode, which needs to be balanced. Thirdly, there should be adequate output current to operate a 50Ω load. Conversely, other techniques for designing high-speed circuits include fT double [11], series peaking technique, shunt peaking, and inductive peaking [13].

Optical fibers are communication mediums that can transfer high data rates. This is why there is an excellent demand for high-speed Optical Transmitters, including data transmittal and receiving devices. These systems have been implemented using newer, popularly known as solid-state devices and circuits [14]. Below are some standard data rates for the optical communication system summarised in Table 1 [15].

Table 1. Standard bit rates for optical communication

SONET	SDH	Bit Rate
OC-1	-	51.84Mbit/s
OC-3	STM-1	155.52overs
OC-12	STM-4	622.08Mbit/s
OC-48	STM-16	2.4883Gbit/s
OC-192	STM-64	9.9533Gbit/s
OC-768	STM-196	39.8131Gbit/s

Which is the optical receiver; the data from the optical fiber is converted to an electrical signal in the form of current using a PD; this signal is then amplified using a TIA and a limiting amplifier and then recovered using a CDR part [2, 9]. This thesis, hence, addresses the transimpedance amplifier, which is part of the optical receiver. It experiences significant attenuation; typically, information sent by fiber optics is anticipated to reach the photodiode (PD) [15]. As a result, very little current reaches the optical receiver. This current is about ten microamperes in magnitude. This current must be transformed into a digital signal in an optical receiver for an inexpensive, high-speed link [6, 16]. The transimpedance amplifier's primary function is to convert the current signal into a voltage signal. The transimpedance amplifier (TIA)'s output voltage is increased by the limiting amplifier, which also provides an appropriate voltage that the clock and data recovery portion (CDR) will accept [17]. To be specific, the task of the clock and data recovery part (CDR) is to synchronize the timing of the input signal and make amplitude-level decisions for the signal, which will generate the digital data stream [5].

Park [18] introduced A 16-channel CMOS inverter transimpedance amplifier (TIA) array is designed for 3-D image processing in uncrewed vehicles, offering high gain, low noise, and efficient power consumption. Zohoori and Dolatshahi [19] presented A Low-Power CMOS Optical Communication Front-End employs a Three-Stage TIA for 5Gb/s applications, showcasing 53.9dBΩ trans-impedance gain, 3.5GHz bandwidth, and 1.52mW power consumption at 1.2V supply. The paper [20] presented a compact CMOS transimpedance amplifier (TIA) based on an elliptic filter approach, achieving 50 dBΩ gain, 15 GHz bandwidth, and 20 pA/√Hz input referred noise current. Based on various design and performance architectures, the development of transition impedance amplifiers in communications, data, and electronics is examined in this article. The paper [21] will serve as a comparative analysis and resource to build completely integrated CMOS transition impedance amplifiers for the next optical receivers. Operating at a 1.5V power supply, this op-amp has a DC gain of 88dB, a slew rate of 174.2V/μs, a unity-gain bandwidth of 1.45GHz, a common-mode rejection ratio of 92dB, and a power dissipation of 224.8μW [22]. The paper [23] presented a CMOS Low-Noise and Low-Power Transistor (TIA) with 1.7GHz -3dB frequency, 54.53dB gain, 2mW power consumption, and 12.6pA/√Hz input-referred noise. Yu et al. [24] discussed a low-noise, power-efficient TIA implemented in CMOS for ultrasound transducers, featuring noise cancellation, capacitive feedback, and continuous time-gain compensation using a voltage-controlled MOS array.

This study aims to create low-power, high-amplification CMOS TIA amplifiers for critical uses in optical receiving circuits with high data transmission rates within GHz and higher bandwidth. Furthermore, the noise impact is negligible, making this study noteworthy compared to previous design and parameter utilization research. The suggested work will help explain this using contemporary simulation tools.

In transimpedance amplifier (TIA) designs, integrating PMOS and NMOS transistors can offer a balanced approach, taking advantage of the complementary characteristics of both types of transistors. Here's an overview of how this design choice might impact circuit topology and how it can differ from existing TIA designs:

- Circuit Topology: A typical TIA topology with PMOS and NMOS transistors often uses a complementary shunt inductive and resistive architecture, where both PMOS and NMOS transistors are strategically paired to handle current more efficiently advantages over traditional designs.
- Enhanced Linearity: A complementary structure leverages the different transconductance characteristics of PMOS and NMOS devices to reduce harmonic distortion and improve linearity.
- Lower Noise: Combining both PMOS and NMOS in the design reduces flicker noise (dominant in PMOS) and thermal noise (dominant in NMOS) compared to designs that use only one transistor type.
- Increased Bandwidth: This topology can achieve higher bandwidth by balancing the input and output stage capacitances using both types of transistors. This can be particularly advantageous in applications requiring high-speed or wide-bandwidth TIAs.

The proposed TIA design was simulated in LT-Spice using micro-device models from the built-in library or models provided by the manufacturer. The simulation conditions included appropriate bias, input signal levels, and operating frequency range. The main analyses performed were AC analysis for frequency response, transient analysis for time-domain behaviour, and noise analysis to evaluate noise performance. Noise effects were considered to ensure realistic operation. Key metrics such as gain, bandwidth, and noise level were measured to validate the design performance.

2. PHOTODETECTORS

Before being processed by the electronic circuitry, the light wave containing the signal travelling through the fibre must be transformed into an electrical signal using a photodetector. The photodetector is integral to the optical preamplifier design [7]. The photodetector's physical properties, such as its

efficiency in converting light energy to proportional current, switching speed, and parasitic capacitance load at the transimpedance amplifier's input node, limit and complicate the TIA circuit design. The p-i-n photodiode, commonly called the p-i-n photodetector, is the most fundamental kind of photodetector. A schematic illustration of a p-i-n photodiode is shown in Figure 2 [7, 14]. With a depletion zone width of L, the intrinsic layer is almost all depleted, and to produce a high electric field in this layer, the junction must be reverse-biased [9].

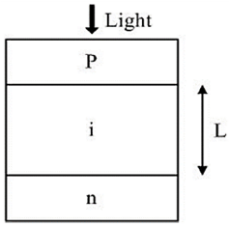

Figure 2. p-i-n photodetector

The characteristics of the photodetector significantly impact TIA design requirements because the TIA must convert the photodetector's output current into a usable voltage signal while maintaining signal integrity and optimizing performance for the photodetector's operating conditions. Key photodetector characteristics that influence. Photodetectors, such as photodiodes, often exhibit significant junction capacitance, varying with factors like reverse bias and photodiode size. High capacitance at the TIA input can limit bandwidth and stability due to the RC time constant it creates with the TIA's input resistance. To address this, the TIA design typically incorporates low input impedance or feedback capacitance to stabilise the circuit and extend bandwidth, often using a complementary PMOS-NMOS topology to balance speed and gain [7, 9, 25].

Generally, a photodetector produces electron-hole (E-H) pairs through the absorption of photons in the depleted intrinsic region [9]. The internal electric and external fields result from reverse biasing, which then separates and gathers the E-H couples to the boundaries of the depletion area [7]. Every photon that enters an ideal photodiode produces an E-H pair. However, some photons are absorbed by semiconductor materials or reflected off the surface to create heat. The quantum efficiency, denoted by (η), is the percentage of photons that produce E-H pairs. The photodetector's electrical current (IPD) generated for a specific quantity of incident optical power (Pop) can be calculated using the quantum efficiency principle [13].

$$i_{\mu t} = \eta \frac{\lambda q}{hc} P_{\sigma} \tag{1}$$

where, the light speed (c), the electron charge (q), the Planck constant (h), and the incident light wavelength (λ) are all given. The sign $\Re$ denotes the constant connecting ipd and Pop, known as the photodetector's responsivity [4].

$$i_{\mu e} = \Re P_{\mu} \tag{2}$$

$$r = \eta \frac{\lambda q}{hc} \tag{3}$$

From Eq. (3), we derive

$$r = \eta \frac{\lambda}{124.3} \tag{4}$$

where, η is expressed as a percentage, λ is expressed in terms of μm, and the responsivity R is expressed in terms of Ampere per Wart (A/W). A GaAs p-i-n photodiode typically has a responsivity of 0.6 to 0.9 A/W [26, 27]. According to recent research breakthroughs, 10 Gb/s photodetectors produced using CMOS-compatible techniques have the best responsivity of approximately 0.3A/W [11-13]. A CMOS-compatible photodetector has much lower responsiveness, but its integration advantage can assist in avoiding the additional expense and parasitic capacitance brought on by bonding and packaging. The corresponding tiny signal circuit of a naked photodetector is depicted in Figure 3 [16]. The current source represents the current produced by the incident light. The primary parasitic is the combination of contact and spreading, the photodiode junction capacitance Cpd, and the spreading resistance Rpd in conjunction with the contact. For a 10Gb/s photodetector, the parasitic capacitance Cpd is typically between 100 and 200 fF. Usually, the parasitic resistance is between 10 and 20 Ohms [27].

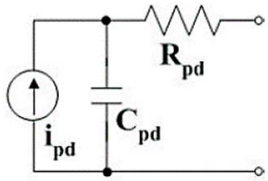

Figure 3. Small signal equivalent circuit for a 10Gb/s bare photodiode

3. PERFORMANCE OF TIA

The input referred noise, input overload current, transimpedance gain, bandwidth, and group delay are the primary design characteristics that define a transimpedance front-end. These parameters are covered in the following sections [24].

As seen in Figure 4, the transimpedance amplifier transforms the input current signal into an output voltage. The output voltage changes per input current variation are called transimpedance [2, 15].

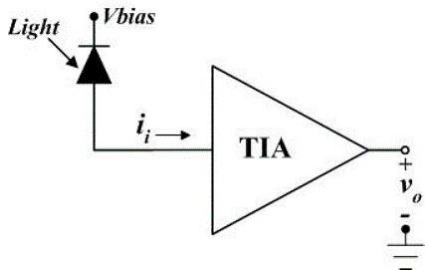

Figure 4. Input and output signals of a single-ended TIA

An essential part of optical communication systems is a transimpedance amplifier (TIA). It produces a voltage output from the input current that a photodiode generates. Broadband TIAs are necessary for high-speed applications to handle high-frequency signals.

Significant Obstacles in the Design of Broadband TIAs [19]:

- Bandwidth: Maintaining stability and gain is difficult

while achieving a large bandwidth.

- Noise: High sensitivity requires low noise.
- Power Consumption: For portable gadgets, efficient power consumption is crucial.
- Dynamic Range: The TIA should handle different input signal levels.

4. RC DELAY MODEL

RC delay models use an average resistance and capacitance throughout the gate's switching range to simulate the nonlinear CMOS transistor's I-V and C-V properties. Despite its clear limits in accurately forecasting specific analogy behavior, this approximation performs astonishingly well for delay estimation [21].

4.1 Effective resistance

The RC delay model uses a transistor and resistor as a series switch. The effective resistance is the ratio of Vds to Ids averaged across the switching interval of interest [16, 22].

RC characterizes effective defense in a single nMOS transistor. While the size of the unit transistor is variable, it typically denotes a transistor with a minimum length and contact diffusion width of 4/2λ. Alternatively, it can refer to the width of nMOS transistors in a conventional minimum-sized inverter for cell libraries. An nMOS's transistor of k times unit width has resistance R/k since it delivers k times as much current. A unit pMOS transistor has a higher resistance [28].

4.2 Effective resistance

Comparable RC circuit models of width k for nMOS and pMOS transistors with contacted diffusion on the source and drain are displayed in Figure 5 [14]. Because holes are less mobile than electrons, the pMOS transistor has roughly double the resistance of the nMOS transistor. Because the n-well is typically tied high, the pMOS capacitors are displayed with VDD as their second terminal. However, as long as the second terminal voltage remains constant, the capacitor's behaviour from a delay standpoint is independent [8]. Therefore, we occasionally portray the second terminal as the ground for ease.

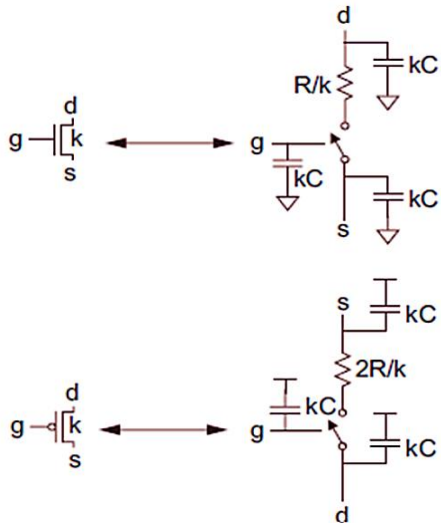

Figure 5. Equivalent transistor circuits

The individual transistors are assembled to create the analogous circuits for logic gates. The corresponding circuit for a fanout-of-1 inverter with very little wire capacitance is depicted in Figure 6. An nMOS transistor of unit size and a pMOS transistor of twice the unit size make up the unit inverters shown in Figure 6(a). Figure 6(b) shows an equivalent circuit where the first inverter drives the gate of the second inverter [29]. If input A rises, the nMOS transistor will be ON, and the pMOS will be OFF. Figure 6(c) shows this example with the switches deleted. Since the capacitors are not charged or discharged, they are also eliminated when short between two continuous supplies. On the output Y, there is a total capacitance of 6C [30].

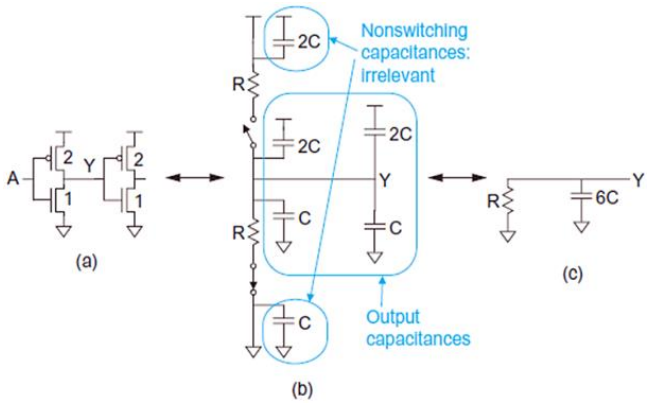

Figure 6. Comparable circuitry to an inverter

An RC tree, or an RC circuit without loops, is a common representation for most interesting circuits. The tree's root represents the voltage source, and the capacitors at the tips of its branches are its leaves [26]. The effective resistance R is on the shared channel between the source and the node and the leaf, multiplied by the total across each node of the capacitance *Ci* on the node, is how the Elmore delay model calculates the delay from a source switching to one of the leaf nodes. The best way to demonstrate Elmore's delay application is by using examples.

$$t_{pd} = \sum_i R_i C_i \tag{5}$$

Delay can be expressed independently of the process, making comparing circuits based on topology easier than manufacturing speed. Furthermore, circuit speed knowledge acquired in one method can be transferred to another using a process-independent delay measure. As you can see, τ=3RC is the delay of a perfect fanout-of-1 inverter without parasitic capacitance. Regarding this inverter delay, we indicate the normalized delay d as follows [21, 31]:

$$d = \frac{t_{pd}}{\tau} \tag{6}$$

5. STATIC POWER CONSUMPTION

Static power consumption in CMOS circuits is consumed when the circuit is not switching or actively changing states. This is distinct from dynamic power consumption, which occurs during switching activities. Static power consumption includes [24, 31]:

1. Leakage Power

- Subthreshold Leakage occurs when the transistor is supposed to be off but still allows a small current to flow due to the MOSFET's non-ideal characteristics. It is particularly relevant in modern, low-power CMOS technologies, where transistors are scaled down.
- Gate Oxide Leakage: This occurs due to tunneling effects through the gate oxide when the gate voltage is applied.
- Junction Leakage: This leakage happens at the pn-junctions in the transistors, especially significant in scaled-down technologies.

2. Power Supply Sources

- In CMOS circuits, power is generally supplied through voltage sources that drive the logic gates. The main types of power sources are [30]:
- Digital Power Supplies: These provide the necessary voltage to the CMOS circuits. The power supply voltage (VDD) is crucial as it determines the speed and power consumption of the CMOS circuits.
- Static Biasing: Static voltage sources are used for circuits that require a fixed voltage for certain operations or biasing conditions. For instance, certain analog CMOS circuits might need a stable reference voltage maintained by a static power source.

3. Power Management Techniques [20, 24, 32]

- To manage static power consumption, various techniques are employed:
- Power Gating: This technique involves turning off the power to certain circuit parts when not in use, thus reducing leakage power.
- Multi-threshold CMOS (MTCMOS): This type of system uses transistors with different threshold voltages to balance performance and leakage power.
- Dynamic Voltage and Frequency Scaling (DVFS): This technique dynamically adjusts the power supply voltage and clock frequency according to the computational load.

6. BROADBAND MATCHING NETWORKS

The easiest method to expand the bandwidth of an existing amplifier design is to raise each gain stage's -3 dB cut-off frequency, often achieved by lowering the corresponding resistive load. Higher thermal noise current and lesser gain result from a smaller resistive load. Since a front-end amplifier's sensitivity and gain closely correlate with communication distance, keeping the gain constant while raising the cut-off frequency is preferable [11]. The gain-bandwidth limit could be investigated using passive matching networks without compromising an amplifier's other capabilities [18-21]. The gain-bandwidth product is increased to maintain a steady load across a broader frequency range. A constant-k filter can accomplish this, meaning the filter's pass-band gain is constant. One such realisation is shown in Figure 7 for the L-C ladder filter. It has been demonstrated [17] that a two-port passive matching network can achieve a maximum gain-bandwidth product augmentation of four times, based on the Bode-Fano Limit. Put another way, the gain may remain constant even if the bandwidth was increased up to four times that of the original amplifier. A more methodical examination reveals that the highest bandwidth. A two-port broadband matching network can achieve an even higher enhancement ratio than four, namely $\pi^{2/2}$=4.93 [29, 33].

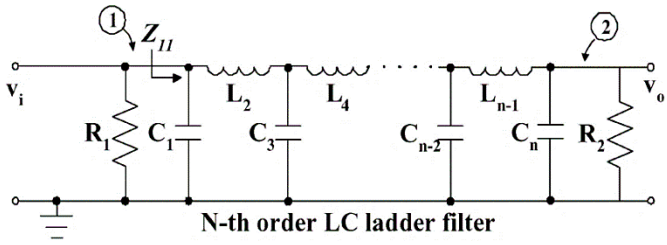

Figure 7. Comparable circuitry to an inverter

7. DESIGN PROPOSED

Since the TIA employs feedback resistance across the TIA amplifier, the NMOS and PMOS combination is intended to produce a symmetric voltage transfer function that yields optimal gain when the input and output are biased. The NMOS and PMOS show different peaks at varying current densities. The nearly equivalent NMOS and PMOS widths ensure that each device's current density is higher than 360 uA m and provides a higher frequency than up to 10 GHz at a 4-mA bias. For CMOS operations, such as NMOS/PMOS push-pull amplifiers, the inherent gain is plotted as a function of supply voltage. The suggested circuit for TIA CMOS, created in the (LT-Spice) program, is depicted in Figure 8.

The perimeters of the source and drain, PD=PS=W+0.4μm, and the source and drain areas, AS=AD=W*0.2μm.

Our design exclusively employs devices with minimum channel lengths. Longer device lengths allow us to achieve requirements at even lower power consumption or with more flexibility to account for process fluctuations.

This design's strong gain and high bandwidth depend on the PMOS and NMOS devices matching flawlessly in each stage. Inadequate matching causes the bias point for the transistors in the following stage to move and reduces gain in each stage. Realistic fabrication procedures do not guarantee such exact matching. Consequently, our design would include DC.

Several circuits were tested before the final design was chosen. These circuits included multistage amplifiers with feedback in both CMOS TIA configurations. Both designs achieved 64 dB gain while maintaining a 3 dB bandwidth at 10 GHz. However, the inverter configuration was more power efficient. A two-stage design of the inverter configuration developed 64 dB of gain. For high gain, we tested the Cascade with feedback amplifier circuits. One Cascade achieved 60 dB of gain.

PMOS & NMOS width, channel length, and other parameters are important in design, as explained in Figure 9.

The TIA design criteria, the load it drives, and the process technique employed can all substantially impact this number (0.9 mW). Although a shunt inductive TIA design may need more biasing to accommodate higher frequencies, its general goal is to increase bandwidth without unduly increasing power.

To achieve a gain of 64 dB in the TIA, the feedback resistance R_f was set to approximately $1585\text{k}\Omega$. His value was calculated based on 64 over 20 end superscripts; the formula cap R sub f equals 10 to the 64 over 20 end superscripts, the formula $R_f = 10^{\frac{64}{20}} \approx 1585\text{k}\Omega$. The choice of R_f balances gain, bandwidth, and noise performance, while a higher feedback resistance increases gain, it can also limit bandwidth due to parasitic capacitance and raise thermal noise. Thus, 1585kΩ was selected to optimize the TIA's performance while meeting the gain requirement.

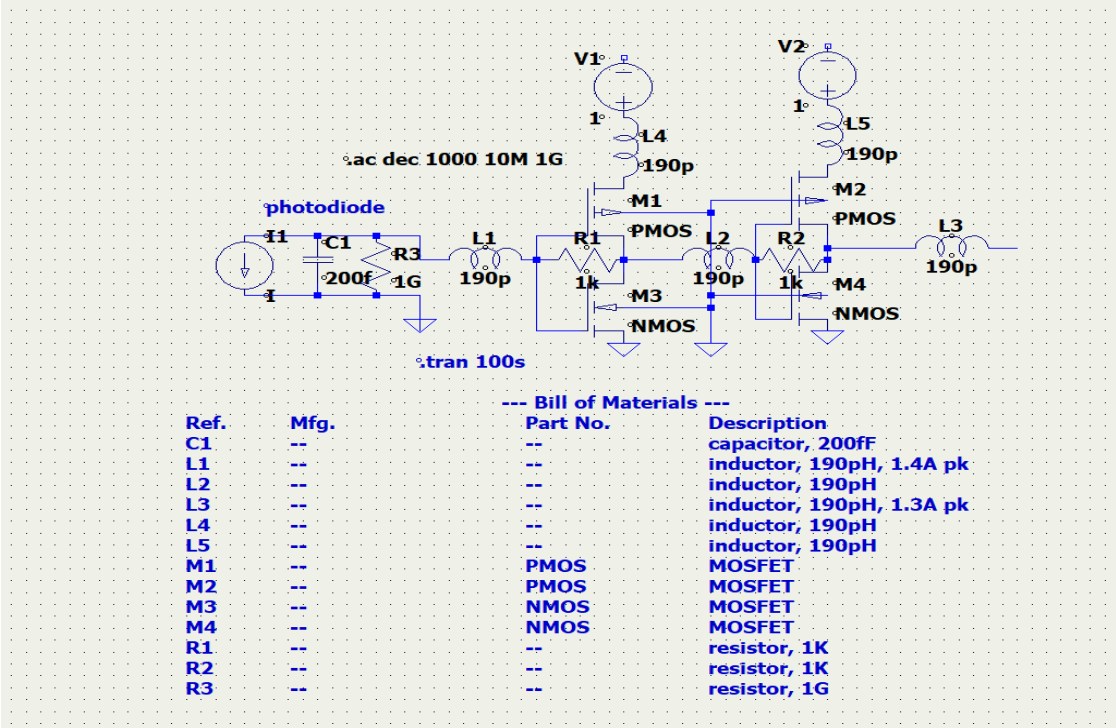

Figure 8. The proposed circuit in LT-Spice

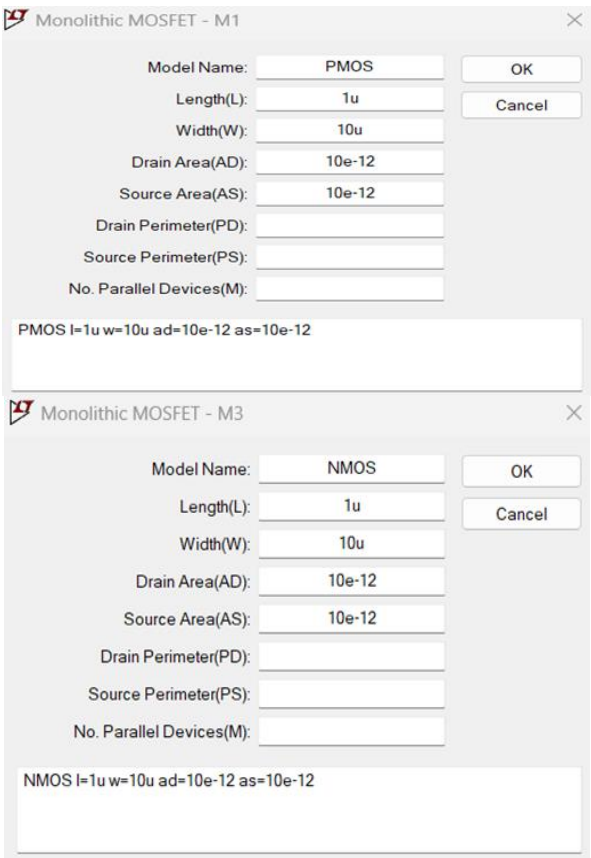

Figure 9. The proposed parameter PMOS & NMOS in LT-Spice

8. RESULTS AND DISCUSSION

Because the TIA uses a feedback resistor, the NMOS and PMOS topologies were chosen to produce a symmetrical voltage transfer function that provides optimal gain when the input and output are biased. The data in Figure 10, which shows all the voltages and currents for the characteristic NMOS and PMOS peaks at different current densities, provides evidence. Each device has a current density of over 360 µA thanks to the nearly equal width of the NMOS and PMOS, which provide frequencies above 10 GHz. Plotting the inherent gain versus supply voltage is common for CMOS processes (e.g., NMOS/PMOS).

This section presents simulation results for a design that minimizes power consumption and traces the signal voltage and amperage of a TIA CMOS to calculate the gain with bandwidth. Each graph will contain multiple paths, each representing a different operating state.

Since the first stage noise will be amplified by 1.55k, the TIA noise analysis offers a vital evaluation to determine whether the entire design will fulfill the minimal criteria for input referred noise less than 500 nv/√Hz. Since 10GHz is the bandwidth used in the overall amplifier design for the optical receiver, as shown in Figure 11, this will be the area of interest in the noise simulation. To ascertain the range of input capacitances the TIA could tolerate before surpassing the minimum noise requirements, a capacitance was attached to the input with values from 0fF to 200fF. The simulation results found in the file TIA gain FFT signal are shown in Figure 12 below.

In CMOS TIAs, there are three main parameters to analyze: gain, bandwidth, and noise. The TIA results from the gain of TIAs as the output voltage per unit of input current, usually expressed in ohms (volts/amperes or ohms). As can be seen from the signals in Figure 10, by dividing the value of each voltage point by the input current, the circuit's gain is calculated to be 64 dB upwards. In advanced CMOS TIAs, achieving multi-gigahertz frequency ranges in TIAs for high-speed data communications (e.g., 10 Gbit/s or 100 Gbit/s optical links) is possible. As shown in the figure, the input noise in TIAs is very significant, especially in low-signal applications such as photodetector circuits.

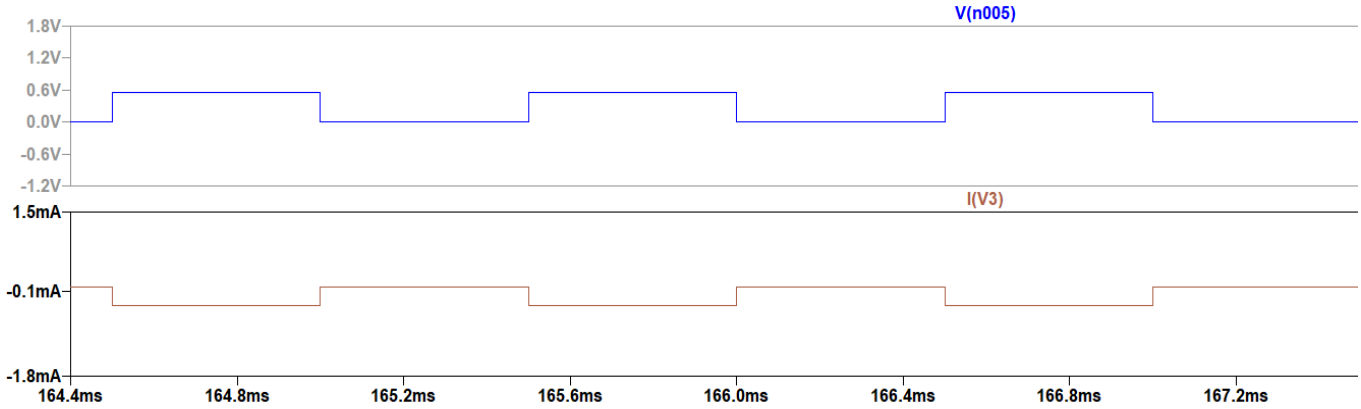

Figure 10. TIA CMOS (Time domain for input current & output voltage) to obtain transimpedance gain

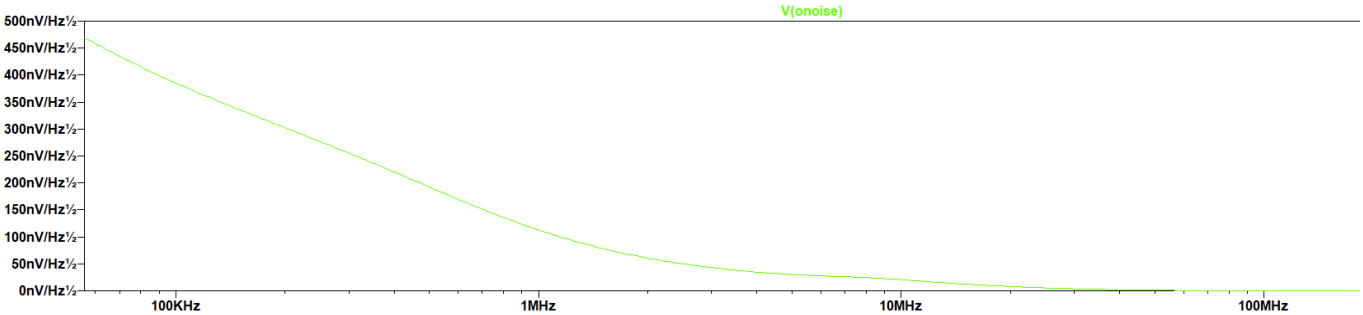

Figure 11. TIA CMOS (Input referred noise)

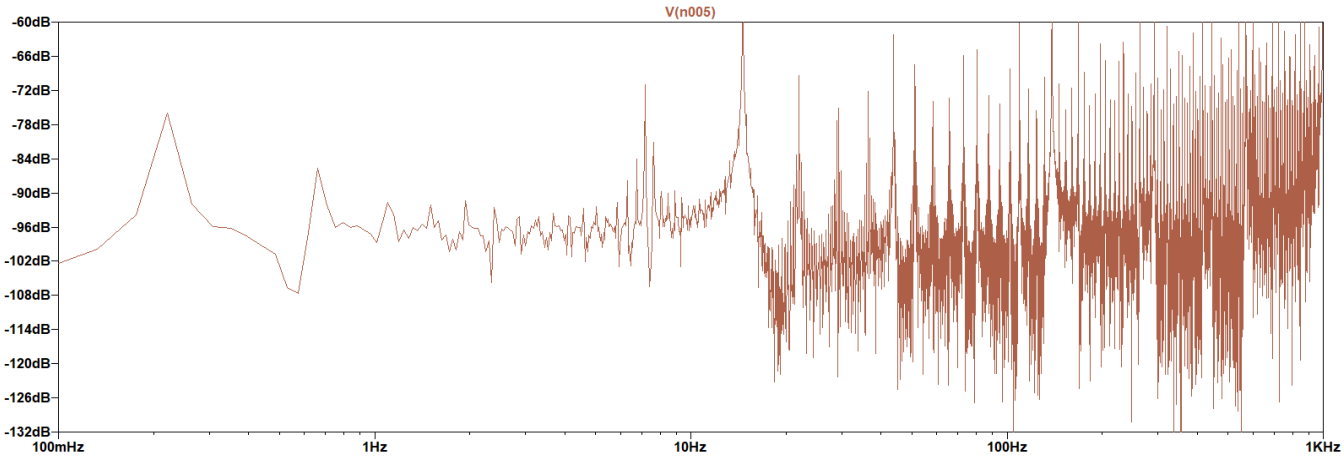

Figure 12. TIA CMOS (Frequency domain FFT for input current & output voltage) to obtain transimpedance gain

The suggested TIA design attains a low input-referred noise current density, essential for improving signal quality in optical communication systems. Because this design strikes a mix between high gain and reduced noise, its noise performance compares favorably to other documented TIAs. Compared to traditional systems, the TIA efficiently lowers heat and flicker noise contributions by optimizing the feedback resistor and biasing conditions, increasing sensitivity. Because of its low noise level, the TIA is particularly suited for high-speed optical communication applications since it can identify weak optical signals.

To demonstrate the bandwidth enhancement in a TIA using shunt inductive peaking, begin by simulating the frequency response of the TIA with and without the shunt inductor to observe any -3 dB bandwidth improvement. Next, verify gain flatness and perform a stability analysis to ensure that the added inductance does not compromise circuit stability. Simulate the transient response to measure enhancements in rise and settling times, as the increased bandwidth should lead to a faster response. Lab equipment such as a network analyzer and oscilloscope can experimentally confirm these improvements if a prototype is available.

9. CONCLUSIONS

The performance of a TIA in CMOS technology is greatly influenced by its gain, bandwidth, and noise characteristics, all of which are critical to achieving optimal signal amplification in low-current applications such as optical communications and sensor systems. The gain of a TIA in CMOS technology is determined by the feedback resistors and the intrinsic properties of the MOS transistors, with higher gains generally improving sensitivity but potentially reducing stability and increasing susceptibility to noise. Bandwidth, closely related to the quotient of gain and bandwidth, is another key factor in

determining the frequency range over which a TIA can accurately amplify signals. Achieving high bandwidth while maintaining adequate gain often involves power consumption and noise performance trade-offs.

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NOMENCLATURE

S	Slew rate
V_m	Maximum voltage
R_{PD}	Spreading resistance
C_{PD}	Parasitic capacitance
G	Gain
H	Planck constant
Pop	Incident optical power
η	Quantum efficiency
$i_{\mu t}$	The photodetector's electrical current
$\Re$	Photodetector's responsivity
I_C	Drain current
I_s	Saturation current