









Three-Phase PWM Rectifier Control: Enhanced Direct Power Control with Neural Networks from Theory to Superior Reality Performance

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ABSTRACT

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direct power control, neural network control, pulse width modulation rectifiers, hysteresis comparators, nonlinear mapping

This paper proposes an innovative enhancement to conventional Direct Power Control (DPC) using Neural Network Control (NNC), presenting an effective alternative control method for three-phase Pulse Width Modulation (PWM) rectifiers. Traditional DPC techniques struggle with dynamic non-linearity and system uncertainties, leading to issues such as limited resolution, lack of adaptability, interpolation errors, sensitivity to noise, overshooting, and distorted grid currents. To address these challenges, the proposed NNC algorithm replaces the PI controller of the DC link voltage, hysteresis comparators for active and reactive power, and the lookup table. The NNC algorithm is distinguished by its nonlinear mapping capabilities and real-time parallel processing. The effectiveness of the proposed approach was validated through experimental and simulation results, using the DSpace DS1103 card along with MATLAB and Control Desk software. The Total Harmonic Distortion (THD) of the grid current in simulation and experimental results is recorded as 1.20% and 4.68%, respectively demonstrating significant improvements in overall system performance in both steady and transient states, proving the efficiency, robustness, and effectiveness of the NNC algorithm compared to traditional methods.

1. INTRODUCTION

Over the past decades, power converters have been a hot issue in industrial applications, due to the rapid progress of flexible alternating current transmission systems [1], especially in the applications associated with renewable energy sources such as solar and wind power [2, 3], smart grid [4], distributed generation systems [5-7], motor drives, the microgrids [8], etc.

A DPC based on the slide mode conception (SMC) is presented in the study [9] to simplify the design control and regulate the actual active and reactive powers without using current control loops and the rotating coordinate transformation involved. Although SMC-DPC) achieved a quicker rectifying reaction and further robustness against uncertainty parameters, the unstable tracking, especially in the steady state, remains a significant issue that requires reconsidering the control systems. To tame this trouble, the Hamiltonian system based on Port-Controlled (PCH-DPC) is designed to use the dissipative conduct of the converter system and its flatness property [10, 11], but ripple still appears as a distorted sign in the active and reactive waveforms.

One of the popular strategies of DPC, predictive control (PC) in an intuitive way, determines the vector sequence of voltage

and computes duty cycles in each sampling period to grasp the multivariable case, system restrictions, and nonlinearities [12, 13]. Although, the PC-DPC method carries out worthy closed-loop compartment. Nevertheless, an inaccurate sequential voltage could cause unwanted performance. To resolve trouble like this, redesignation of sequential voltage [14] is presented, but it suffers an extra computational burden. In order to obviate such computational issues, a novel concept is proposed to assume static vectors of voltage without using the angular position of grid voltage or the virtual-flux vector [15]. In the study [16], a simple compensation term is included in the power reference to simplify and improve DPC performance.

The need for the DPC strategy for control feedback increases the complexity and computational processes; hence, the robustness of the system is decreased. Another issue of the conventional DPC strategy is the requirement of efficient control to overcome the overshoot of the dynamic response and achieve a stable steady state performance free of oscillations to obtain the stability of the system. Otherwise, regulation of the rectifier output voltage lies directly in the abilities of the DC link voltage controller [17] to ensure a constant value of DC voltage to meet the needs of electronic devices that require a stable DC link voltage even if the AC input is fluctuating. In spite of the high value of DC link voltage rises the rectifier

efficiency, however, high DC link voltage causes much damage as the stress of converter components, insulation Breakdown, size and cost requirements of capacitors and inductors, and loads compatibility or other systems.

The motivation of the article is to overcome the limited behaviour of the hysteresis controllers of active and reactive powers, the lookup table drawbacks, and avoid the restricted and inflexible performances of PI controllers by replacing those components with two NNCs, the first one instead of (Hysteresis comparators of active and reactive powers and lookup table), while the second one is instead of PI controllers of DC-Link voltage.

The NNC-DPC technique is proposed due to the following reasons:

- Its capabilities to predict the future behaviour of the system with low computational efforts.
- Presents a good generalization capability [16].
- Reproduction of the performances of continuous function in a preselected operational domain.
- NNC can be easily implemented [18].

The rest of the paper is organized as follows. In Section 2, modelling of AC-side and DC-link voltage is introduced. Section 3 depicts the classical direct power control. Section 4 presents the proposed NNC-DPC algorithm. Sections 5 and 6 presents the simulation results and experimental validation findings. Finally, it ended with a conclusion.

2. PWM RECTIFIER MODELING

2.1 AC-Side modeling

The PWM rectifier is modelled as indicated in Figure 1, considering that, the grid voltage is balanced [5, 19], and it can be written as follows:

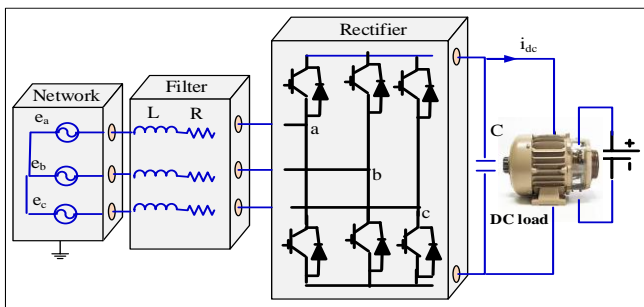


Figure 1. Configuration of two-level PWM rectifier

$$v_s = R_s i_s + L_s \frac{di_s}{dt} + u \quad (1)$$

whereas, V_s , i_s , and u are the grid voltage, the input current, and the rectifier voltage, respectively, R_s and L_s are the equivalents of series resistance and inductance, respectively. The model (1) can be characterized in the stationary α - β [20] frame as:

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} + \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \end{bmatrix} \quad (2)$$

As a result, actual active and reactive models of powers can

be defined as follows:

$$P = \frac{3}{2} (v_{s\alpha} i_{s\alpha} + v_{s\beta} i_{s\beta}), Q = \frac{3}{2} (v_{s\beta} i_{s\alpha} - v_{s\alpha} i_{s\beta}) \quad (3)$$

where, $v_{s\alpha}$, $v_{s\beta}$, $i_{s\alpha}$, $i_{s\beta}$, denote the grid voltages and their currents in the (α - β) frame, while P refers to the actual power and Q denotes the reactive power. The main objectives of controlling the PWM rectifier are to address the DC link voltage at the required level and provide the desired reactive power to improve the quality power ($\cos\phi \rightarrow 1$).

2.2 DC-Link voltage modeling

Ignoring the converter losses, the power fluctuations of the DC-link capacitor can be written as:

$$P_c = CV_{dc} \frac{dV_{dc}}{dt} = P_i - P_l \quad (4)$$

Considering that

$$P_l = V_{dc} * I_{dc} \quad (5)$$

where, P_i , P_l , and P_c are the supplied power from the grid side, consumed power by the load, and stocked power in the capacitor, respectively, C and V_{dc} are the DC-link capacitor and its voltage. Substituting (5) into (4) yields:

$$\frac{dV_{dc}}{dt} = \frac{P_i}{C} \frac{1}{V_{dc}} - \frac{1}{C} I_{dc} \quad (6)$$

The goal is to limit and stabilize the DC-link voltage fluctuations via a strategy of control more flexible with turbulences that result in costly damage to the converter [21].

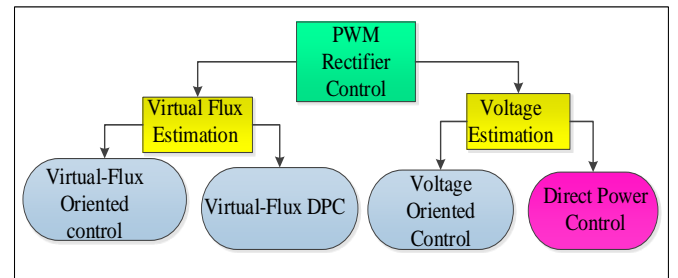


Figure 2. Control strategies of PWM rectifier

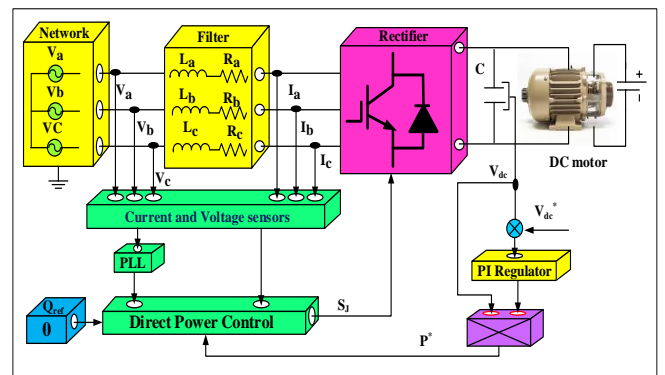


Figure 3. Configuration scheme of classical direct power control (C-DPC)

Figure 2 presents four strategies of PWM rectifier control, with DPC as one of the crucial methods. First, the modelling of DPC is briefly discussed in this section. Figure 3 depicts the typical setup of DPC for a three-phase PWM rectifier.

3. CLASSICAL DIRECT POWER CONTROL

3.1 Direct power control strategy

The DPC method is inspired by (DTC) approach [14, 22] and exploited in the electrical machine domain. The control vector is chosen using a well-defined switching table, as given in Figure 4. This table relies on three inputs, the angular position of grid voltage given by the Eq. (11) and the two instantaneous errors Δp , Δq . The active power reference comes from the regulation of DC-link voltage, whereas, the reactive power reference is assumed equal to zero to ensure the unity power factor (UPF) [23]. Figure 5 detailed configuration of DPC method.

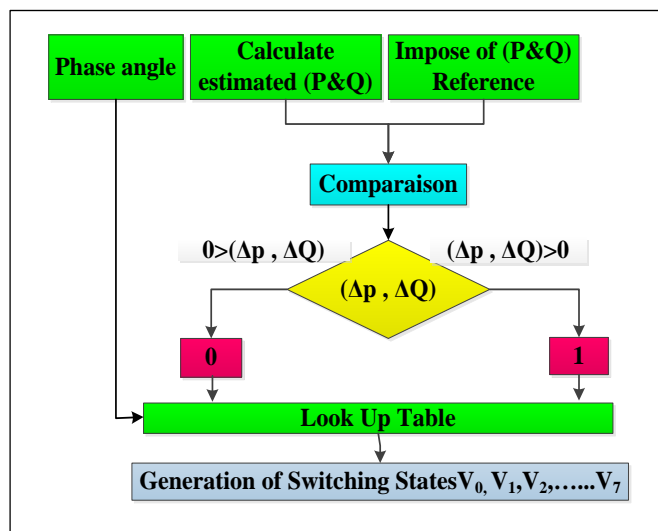


Figure 4. Generated switching states via LUT and hysteresis comparators

The DC-link voltage is maintained by adjusting the active power, and the (UPF) is fulfilled under an operating control of the reactive power to close to zero [24].

3.2 DC-link voltage control

An essential task of the PI controller is to address V_{dc} to certain reference values [25]. Eq. (7) describes the mathematical formula of the PI transfer function:

$$\frac{v(t)}{v^*(t)} = \frac{k_p s + k_i}{C s^2 + k_p s + k_i} = \frac{C}{k_p} \left(s + \frac{k_i}{k_p} \right) \quad (7)$$

$$k_p = 2 \cdot \varepsilon \cdot \omega_n \cdot C, k_i = C \cdot \omega_n^2$$

Its structure with the system anti-windup method is given in Figure 5 [26, 27]:

DPC is founded on instantaneous power calculation. In Eqs. (8)-(11), conventional formulas determine the instantaneous power P and Q in α - β reference frame.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} I_{s1} \\ I_{s2} \\ I_{s3} \end{bmatrix} \quad (8)$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_{s1} \\ v_{s2} \\ v_{s3} \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (10)$$

$$\theta = \arctan\left(\frac{v_\alpha}{v_\beta}\right) \quad (11)$$

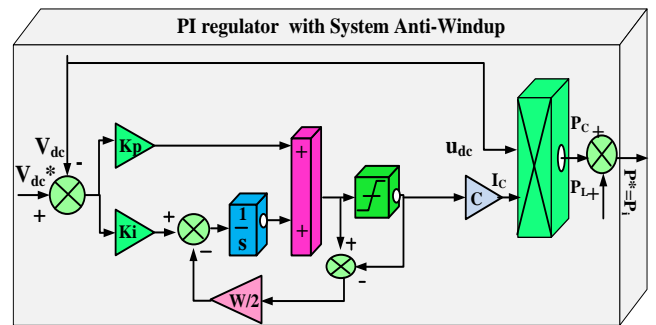


Figure 5. PI controller with system anti-windup

The knowledge of the grid voltage sector is required to determine the switching states, so the α - β plan is divided into twelve sectors, which can be proven in Figure 6(a), These sectors can be determined by the following subsequent relationship.

$$\frac{\pi}{6}(N-2) \leq (\theta_N - 1) \leq \frac{\pi}{6}(N-1) \quad N = 1, 2, 3, \dots \quad (12)$$

To create the instantaneous error of P and Q, a comparison process is achieved between the actual active and reactive powers and their references. Hysteresis comparators deal with the active and reactive errors to generate the control pulses (0 or 1) required to formulate the lookup table as shown in Figure 6(b)

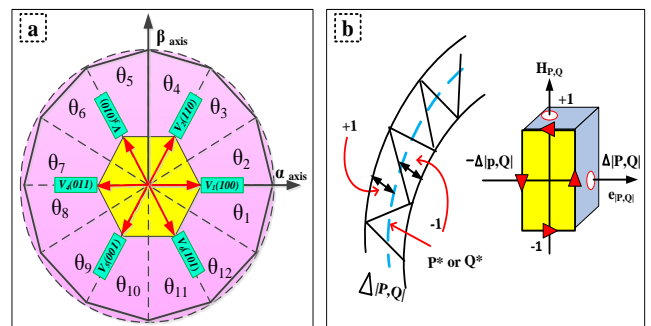


Figure 6. (a) Sectors Scheme in α - β stationary frame, (b) Hysteresis comparator scheme

The selection of the sector's voltage is synthesized and founded on the changes in sign and magnitude of the active and reactive power for each sector. Take θ_1 As an example,

Table 1 shows the active and reactive power signs, hence, the switching table voltages in θ_1 is obtained as depicted in Table 2.

The comparison process between the active and reactive power references and their actual values is achieved via the conventional hysteresis comparator to generate the output control pulse (0 or 1) as shown in Figure 6(b). To form the lookup table voltages $V(sa, sb, sc)$, the phase angle θ_N and switching pulses generated via the hysteresis comparators H_p and H_Q are configured as shown in Table 3.

Table 1. Variation of active and reactive power signs

dP/dt		dQ/dt	
if ($H_p=1$)>0	if ($H_p=1$)<0	if ($H_Q=1$)>0	if ($H_Q=1$)<0
V_2, V_3, V_4 and V_5	V_1 and V_6	V_1, V_2 and V_3	V_4, V_5 and V_6

Table 2. Switching table for sector 1

	$H_Q=1$	$H_Q=0$
$H_p=1$	V_2	V_5
$H_p=0$	V_1	V_6

Table 3. Lookup table of classic direct power control strategy

Dp	Dq	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	1	V_5	V_5	V_6	V_6	V_1	V_1	V_2	V_2	V_3	V_3	V_4	V_4
1	0	V_3	V_3	V_4	V_4	V_5	V_5	V_6	V_6	V_1	V_1	V_2	V_2
0	1	V_6	V_1	V_1	V_2	V_2	V_3	V_3	V_4	V_4	V_5	V_5	V_6
0	0	V_1	V_2	V_2	V_3	V_3	V_4	V_4	V_5	V_5	V_6	V_6	V_1

4. PROPOSED NNC-DPC ALGORITHM

4.1 NNC Based on the dataset of hysteresis controllers and lookup table

Many drawbacks are associated with the active and reactive hysteresis and lookup table performances of the conventional DPC technique. The limited performance, high rate of ripple in the current lines of the grid, slow dynamic response of the system, and a wrong selection vector coming from the lookup table can adversely affect the overall performance of the converter, furthermore, the computational burden of the LUT impacts on the response for the entire technique.

To overcome all of these cons, an NNC controller has been replaced instead of the three components (hysteresis comparators of active and reactive power and lookup table). This NNC has two hidden layers with sigmoid functions consisting of 20 neurons in each hidden layer. It has 7 inputs, errors of active and reactive power (ΔP , ΔQ) with their precedent values of error Z^{-1} , Z^{-2} and sector θ_N , respectively, while the outputs are the control switching pulses of the rectifier (S_a , S_b , and S_c) as shown in Figure 7.

4.2 NNC based on the dataset of PI DC link voltage control

The confined behaviour of the PI controller expands the peak overshoot and ripple in active power and effects directly on the dynamic response of the system not only in the transient state but also in the steady state. To remediate all cons, an artificial neural network control has been substituted for the PI controller with one hidden layer consisting of 20 neurons,

where, its input is errors of DC-link voltage, Z^{-1} and Z^{-2} , while the output is $I_c(A)$ as shown in Figure 8.

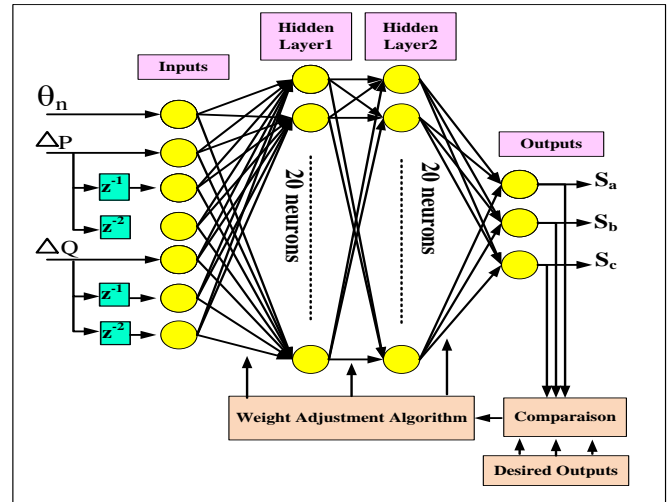


Figure 7. Closed loop scheme NNC based on hysteresis controller with LUT

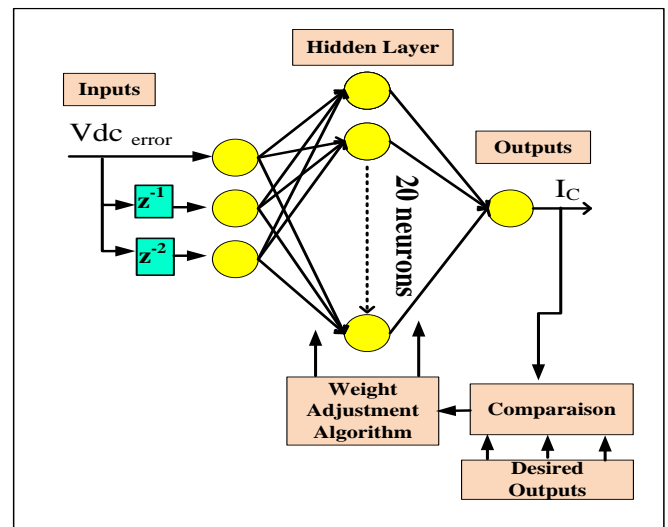


Figure 8. Structure of hidden layers closed loop NNC based on PI controller

5. SIMULATION RESULTS

To predict, optimize, and gain an effective insight into the proposed NNC-DPC algorithm behaviour, the simulation process is achieved under the Matlab/ Simulink environment. Figure 9 shows the configuration of the proposed algorithm. The parameters of the system and load are illustrated in Tables 4 and 5, respectively.

5.1 Steady state performance

To test the stability and convergence of the system, a numerical simulation process is achieved. The reference DC bus voltage is set as 170V and the reference reactive power is fixed as zero to ensure the unity power factor.

Figure 10 shows the simulation process outcomes, it can be seen that the proposed algorithm achieved a stable steady state performance free of the broadband oscillations, where the

actual DC link voltage, active and reactive powers track accurately their references with a minimum rate of harmonics as shown in Figures 10 (A, C, and B). In Figure 10 (D), it's clear that the current has a sinusoidal waveform free of significant ripples and in phase with the grid voltage, which proves the efficiency of the proposed algorithm, where the efficient transferred power from the source to load is consumed and there is no significant reactive power flow. It can be noted the efficiency of the proposed NNC-DPC algorithm via the rapid tracking in charging the initial power of the inverter capacitor as shown in the shaded zones in Figure 10.

5.2 Dynamic response test

Figure 11 shows the dynamic response of the proposed algorithm, where the reference DC bus voltage is set as 170V, then stepped up to 220V at $t=0.2s$, and then stepped down to 180V at $t=0.4s$. It can be observed that the proposed algorithm was robust and efficient, where the actual DC link voltage, active and reactive powers follow accurately their references and achieved a fast response to the reference variation of the DC voltage without overshoot and a minimum rate of ripples (THD=1.24%). The unity power factor can be described via

Figure 11 (F); it can be seen that the current and voltage of the power source are in the same phase and have sinusoidal waveforms, which refers to the less flow of reactive power from the source to the DC load.

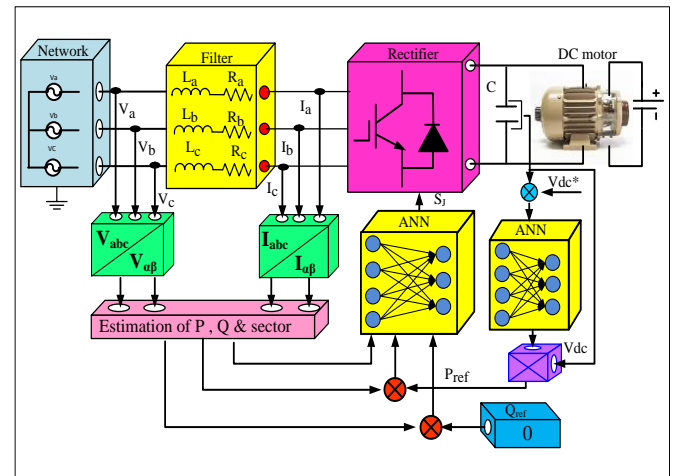


Figure 9. Configuration of proposed NNC-DPC algorithm

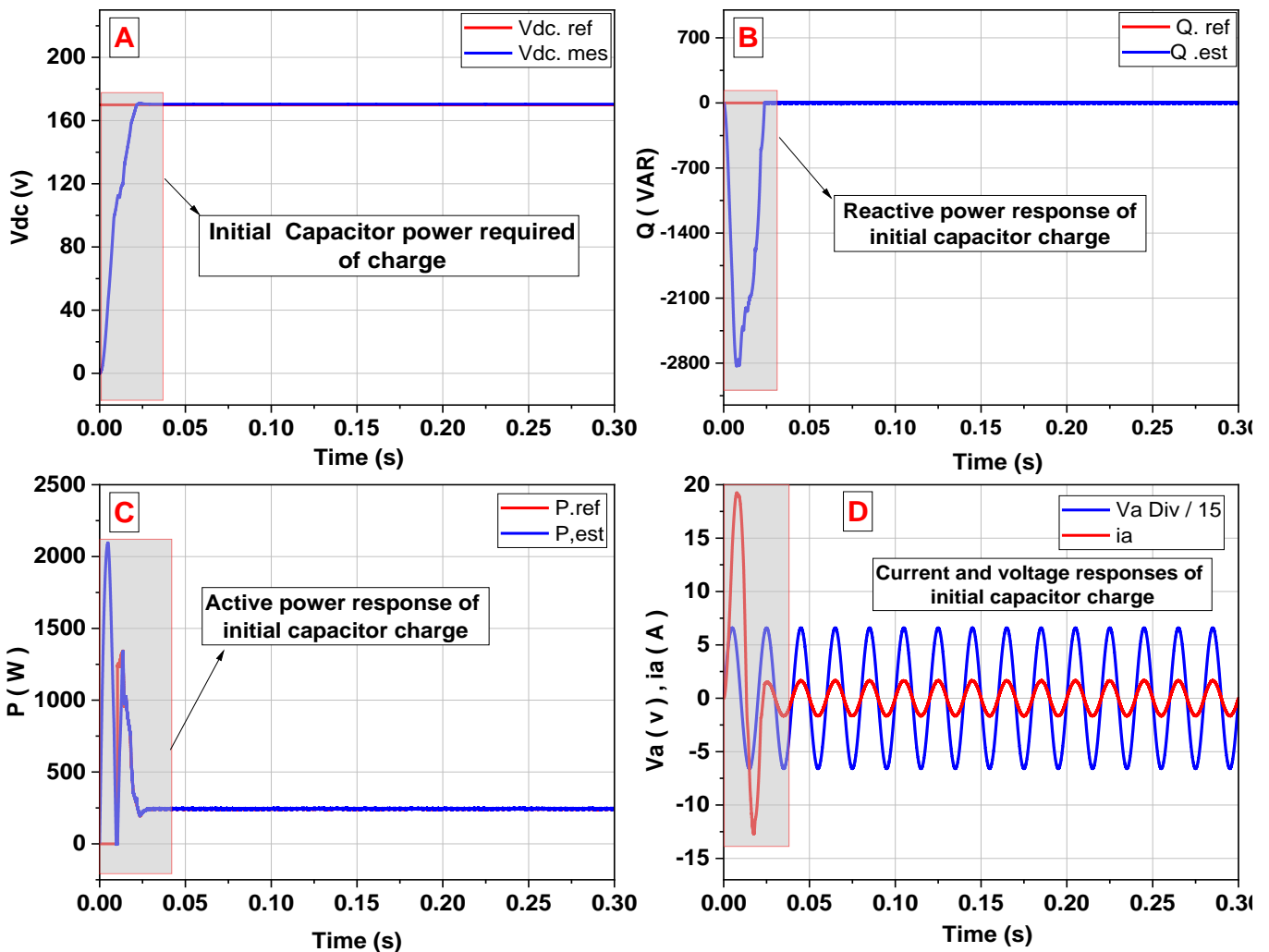


Figure 10. Simulation results: Steady-state performance of proposed NNC-DPC algorithm

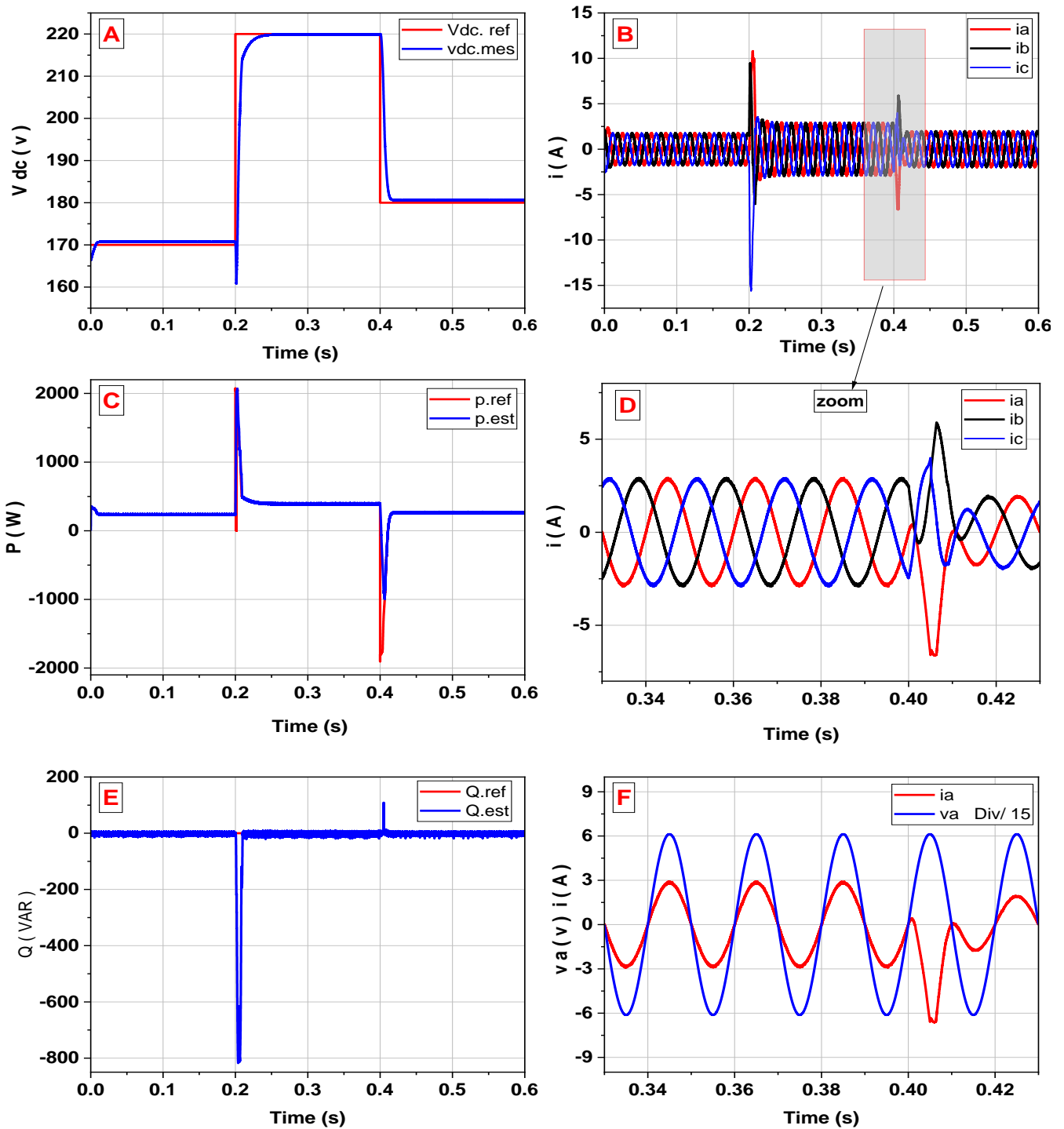


Figure 11. Simulation results: Dynamic response performance of the proposed NNC-DPC algorithm

6. EXPERIMENT VALIDATION FINDINGS

To obtain the empirical observation, and causal inference and validate the proposed NNC-DPC algorithm, the experimental tests were carried out via the DSPACE DS 1103 hardware ordered by MATLAB and control desk software [28]. Tables 4 and 5 show the parameter description used in the experiments, while Figure 12 showcases the total harmonic distortion THD of current for proposed NNC-DPC algorithm. Figure 13 illustrates the experimental platform components used to implement the proposed algorithm. It contains a three-phase IGBT with an anti-parallel diodes-based PWM rectifier. Three sensors of current measure inputs currents (I_a ,

I_b) and DC-link current I_{load} , respectively, in addition, three sensors of voltage also are used to measure the voltage inputs of the grid (V_a and V_b) and DC-link voltage V_{dc} , respectively.

Table 4. Platform parameters of DPC strategy

Parameter	Value	Unit
Phase Voltage (RMS)	53	volt
Frequency of Grid Voltage	50	Hz
Nominal AC Filter (Resistance)	2	Ω
Nominal AC Filter (Inductor)	20	mH
Nominal DC-Link Voltage	170	volt
Sampling Frequency	10	kHz

Table 5. Parameters of load (DC motor)

Parameters of Load (DC Motor)	Value	Unit
Armature Voltage	220	Volt
Armature Current	9	A
Armature Inductance L_a	0.0830	mH
Armature Resistance R_a	2.3182	Ω
Rotor Inertia J	0.0138	Kg.m ²
Rated Speed	1470	rpm
Power	1.5	Watt
Torque Coefficient K	1.2379	N.m/A
Friction Coefficient F	0.002	N.m/Rad

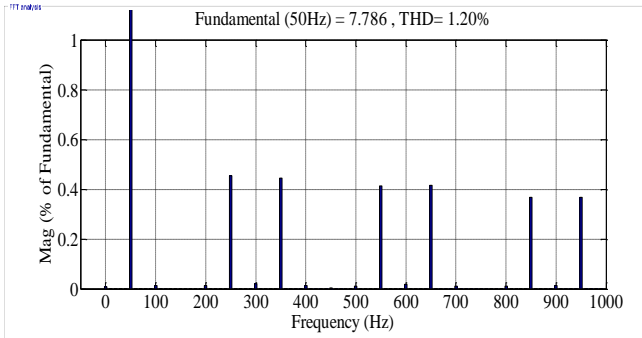


Figure 12. Total harmonic distortion THD of current for proposed NNC-DPC algorithm

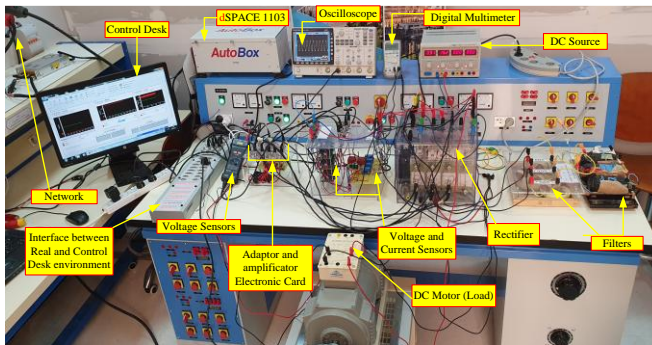


Figure 13. Experimental test setup

6.1 Steady state performance

This experiment aims to analyze, understand, and characterize the behavior of the proposed algorithm under stable operating conditions to provide insights into the stability and efficiency of the overall system.

The reference DC link voltage and reactive power are imposed as 170V and zero VAR, respectively.

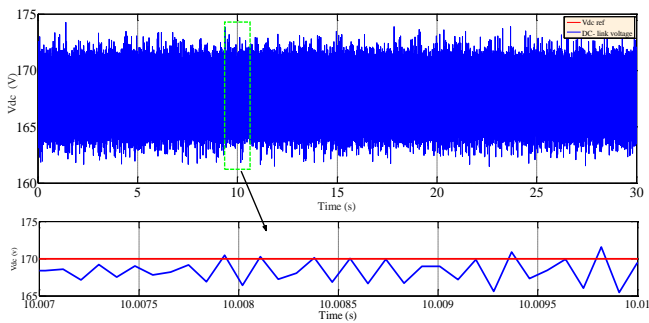


Figure 14. Experimental results of DC bus voltage performance under steady state test

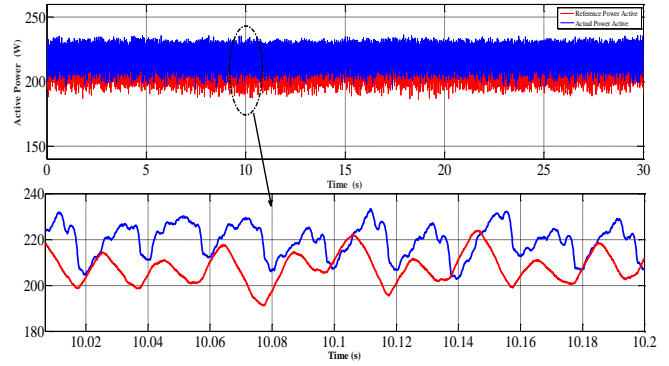


Figure 15. Experimental results of active power performance under steady state test

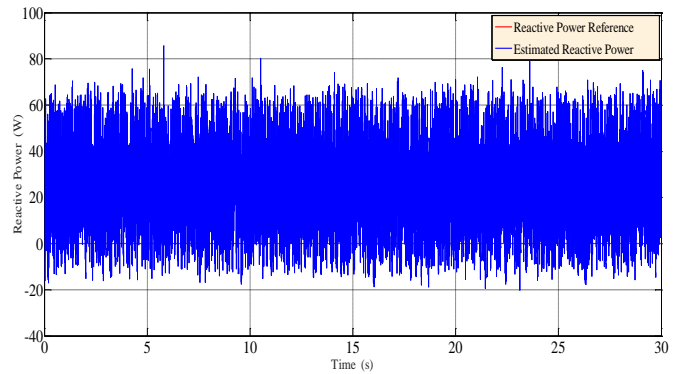


Figure 16. Experimental results of reactive power performance under steady state

Figures 14-16 show the DC bus voltage, and active and reactive power performances, respectively. The effectiveness and robustness of the system appear via the ability of control to track accurately the desired reference signals and maintain the outcomes of the system in line with the desired values with a minimum broadband oscillation due to the predictive character of the proposed NNC-DPC algorithm.

6.2 Dynamic response test

This experiment aims to analyze and understand the performance of the control system and test how the proposed algorithm reacts to sudden changes over time. In order to achieve this process, the reference DC bus voltage is posed as 170V, then stepped up to 220V at $t=33s$, and then stepped down to 180V at $t=72s$. The reference reactive power is set as zero VAR.

The stability of control appears via the accurate tracking with a minimum rate of harmonics and was able to avoid the significant. While the robustness of the control system clearly appeared by the fast dynamic response, it can be observed via the short settling time and non-overshoot as shown in Figure 17.

Figure 18 illustrates the dynamic response of the active power; it can be seen that the actual active power tracks accurately its reference in the steady and transient states. The proposed algorithm achieved a fast dynamic response to the sudden changes and was able to track the variable reference active power without chattering and able to minimize the significant oscillations. It ensured a stable and robust performance.

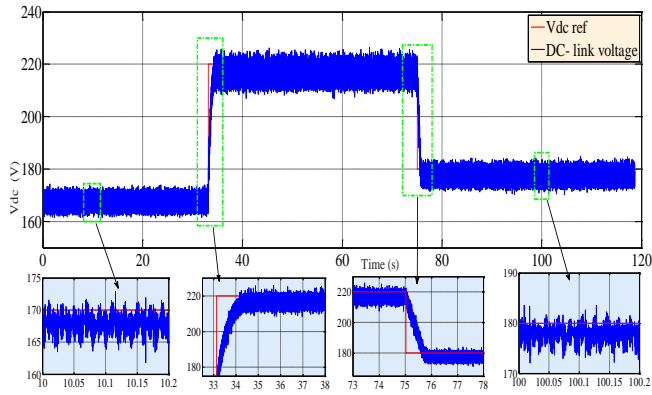


Figure 17. Experimental results of the proposed NNC-DPC, performance dynamic response of V_{dc} link voltage

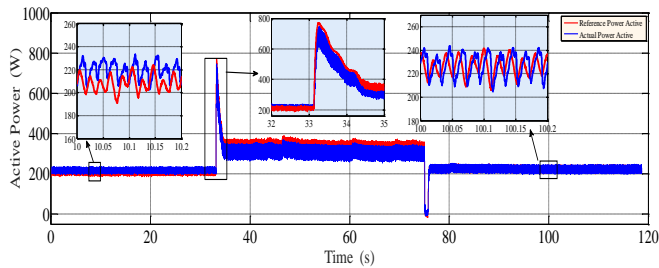


Figure 18. Experimental results of proposed NNC-DPC, active power dynamic response performance

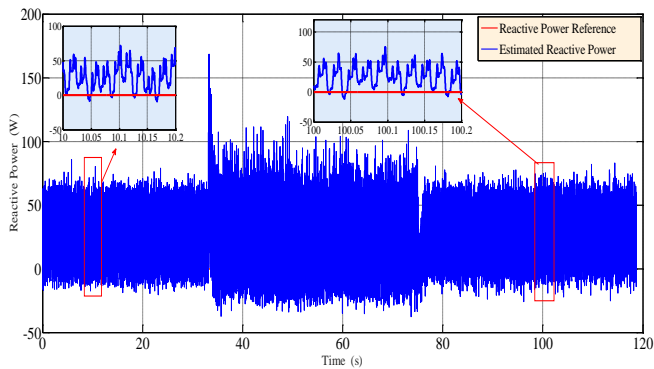


Figure 19. Experimental results of reactive power performance of the proposed NNC-DPC technique

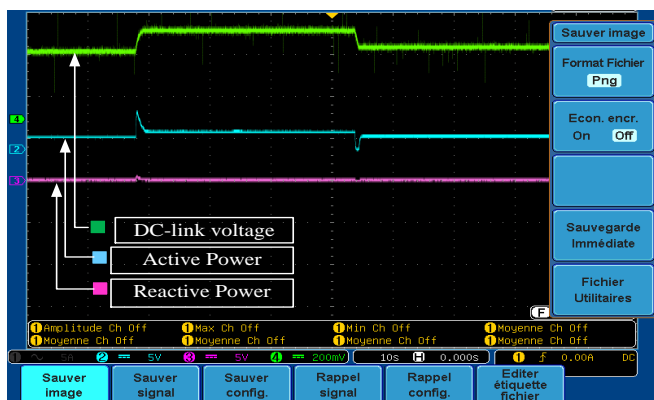


Figure 20. Experimental results of proposed NNC-DPC algorithm, DC link voltage, P & Q waveforms

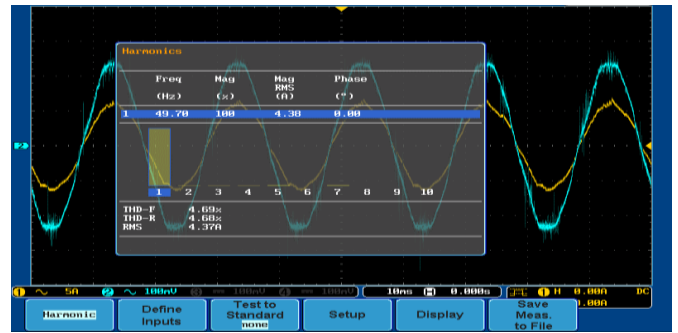


Figure 21. Experimental results of proposed NNC-DPC algorithm, current and voltage waveforms

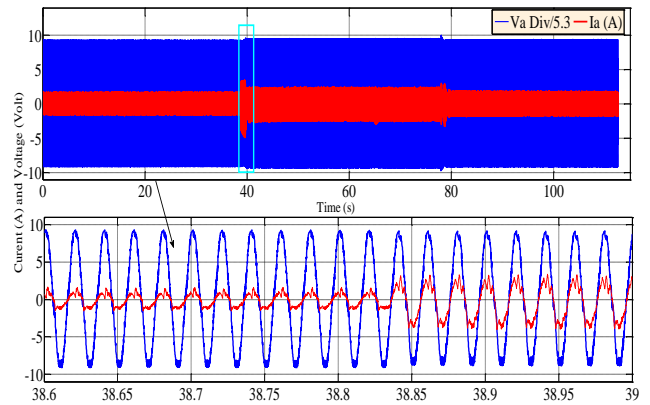


Figure 22. Experimental results of current and voltage performance of the proposed NNC-DPC technique

The reactive power is an important sign to recognize the power flow from the source to the load, where the minimum value of reactive power means that the major real active power is utilized via the load and vice versa. Figure 19 shows the reactive power waveform. It can be noted that the proposed algorithm was able to minimize the reactive power rate, reduce the energy losses, and decrease the significant ripples that distort the current line. The proposed algorithm achieved a stable and robust performance, where the actual reactive tracks its reference with small broadband oscillations.

To observe the dynamic response of the proposed algorithm in real-time, the DC bus voltage and active and reactive power are presented via the oscilloscope as shown in Figure 20. It's clear the smooth and accurate tracking of the system, where the waveforms were free of the significant oscillation and the dynamic control response was fast and free of overshoot.

Figures 21 and 22 show the unity power factor, it is clear that the current and voltage of the source have a zero phase difference which proves that the proposed algorithm transfers efficiently the actual maximum power between the source and DC load. Smooth sinusoidal waveforms of current and voltage refer to the ability of the proposed algorithm to reduce the harmonics, (experimental THD of the current line is 4.68%) which means a stable performance.

7. CONCLUSIONS

In this research, a novel NNC-DPC approach for a three-phase PWM rectifier is introduced. The assumed technique demonstrated its competence and adaptability, a significant improvement in the system's transient responsiveness and

steady-state performance. The experimental and simulation results proved the efficiency and robustness of the proposed algorithm; it was able to overcome the major defects of the conventional DPC via using a powerful machine-learning algorithm enabled to achieve superior behavior, good regulation, and accurate tracking not only in dynamic fast response but also in the stable steady state performance. The proposed algorithm transferred efficiently the actual power from the source to the DC load with minimum energy losses, which appeared via the smooth sinusoidal waveforms of current and voltage of the source (experimental THD is 4.68 %, and simulation THD is 1.20%).

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