







Analytical Modeling and Experimental Validation of Common Mode Impedance in a Low-Voltage DC Micro-Grid

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ABSTRACT

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DC micro-grid, electromagnetic interference, common mode, impedance, conducted electromagnetic, converter DC-DC, power converters, analytical modeling electrical installation

Currently, electrical networks contain more and more electrical devices interconnected by power, ground, and control cables, which are generally propagation paths of conducted electromagnetic interference (EMI). It is interesting to focus specifically on mode disturbances common. This paper proposes an effective method to recognize low voltage direct current micro-grids (LVDCMG), through common mode impedance identification. For this purpose, a direct current micro-grid (DCMG) can be modeled, it consisted from three converters connected in parallel, including the connectors; the model consists in calculating the common mode impedance of the DCMG. It should be noted that a good knowledge of impedance helps engineers to perform filter optimization, prognostic algorithms, and the protection of electrical installations. The analytical models have been tested by numerical simulation and validated by experimental measurements over a wide frequency range up to 30MHz.

1. INTRODUCTION

Efficiency, productivity, and power quality stand as the pillars of modern electrical infrastructure. The judicious selection and operation of energy-efficient equipment not only curtail costs but also yield environmental dividends by minimizing energy wastage. A dependable power supply, coupled with high-quality performance, underpins seamless operations, thereby augmenting productivity and curtailing downtime. Moreover, the maintenance of stable voltage and current levels serves as a shield for delicate electronics, averting potential damage and operational glitches. These elements are interconnected: heightened efficiency translates to reduced energy consumption, directly bolstering productivity. Concurrently, the assurance of reliable power and superior quality amplifies equipment efficiency, further elevating productivity levels. By prioritizing these vital aspects, modern electrical installations attain peak efficiency, bolstered reliability, and contribute substantively to a more sustainable future [1-10]. Each of these elements delineates objectives and guides scientific research throughout the continuous development of electrical networks across production, distribution, and optimal energy utilization [11-17]. The cornerstone of modern systems lies in the seamless integration of intelligent electronic interfaces between energy sources and diverse loads. These interfaces act as the nervous system, facilitating the efficient transfer and management of power, while enabling sophisticated control and real-time optimization. Their impact transcends traditional sectors, revolutionizing transportation through advancements in aircraft, ship, and train efficiency, controllability, and safety.

The electrification of vehicles hinges on these interfaces, ensuring optimal power flow and battery operation. Furthermore, smart grids, the backbone of a sustainable energy future, rely on these interfaces to orchestrate intelligent energy distribution. This includes real-time monitoring, dynamic optimization based on demand fluctuations, and bi-directional communication between energy producers and consumers. [18-25]. Moreover, the development of micro-grids (MGs), which can be alternating current (AC), direct current (DC), or Hybrid (AC/DC) configurations, has strengthened and improved the reliability of primary electrical installations.

Micro-grids are increasingly popular because they seamlessly integrate renewable energy sources like solar and wind power, reducing reliance on fossil fuels and promoting sustainability. Low voltage direct current (LVDC) micro-grids offer additional advantages that solidify their position as a preferred choice. Natural DC Interface: Many renewable energy sources, such as solar panels and batteries, naturally produce direct current (DC) power. LVDC micro-grids eliminate the need for multiple AC-DC and DC-AC conversions, leading to higher overall system efficiency. Reduced Losses: DC systems experience lower transmission and distribution losses compared to AC systems, particularly over shorter distances common in micro-grid applications.

Simpler Control and Protection: The inherent characteristics of DC micro-grids often simplify control strategies and protection schemes, potentially reducing system complexity and cost [26-31]. However, despite these advancements, challenges such as optimizing energy management within the micro-grid and knowledge gaps regarding long-term system behavior remain. Identifying and developing and

implementing strategic solutions to address, these issues are crucial to ensure micro-grids operate within established safety and performance standards [32-35].

The seamless integration of intelligent electronic interfaces between energy sources and diverse loads, previously likened to the nervous system of modern systems, is a technological marvel. However, a hidden challenge lurks within these powerhouses: power converters. These crucial components, characterized by their high-frequency switching operations, are pivotal sources of Electromagnetic Interference (EMI) and harmonics. This interference, if not addressed, can undermine power quality and disrupt service continuity, jeopardizing the very systems it aims to enhance [36-38].

Electromagnetic Interference manifests in two primary forms: conducted and radiated. Conducted EMI utilizes cables and conductive components as its unwelcome highway, potentially disrupting the delicate operations of neighboring electronics. Imagine a whisper traveling along a wire, capable of wreaking havoc on sensitive equipment. Radiated EMI, on the other hand, behaves like a ripple in a pond, radiating outward as a transverse wave through the surrounding space.

Understanding these distinct characteristics of EMI is crucial for devising effective mitigation strategies. As electronic systems and power converters proliferate, managing electromagnetic disturbances becomes paramount. This ensures the overall reliability, performance, and smooth operation of electrical installations, a necessity in our increasingly interconnected world [39-44]. This paper specifically delves into conducted interferences, focusing on common-mode (CM) propagation [45-50]. CM propagation utilizes the protective conductor "G", serving as a propagation path, irrespective of the connection of the entire chassis and metals to the ground through equipotential bonding of the entire installation [50-54]. Rigorous EMC standards have been imposed on electrical and electronic equipment to ensure satisfactory functioning within their electromagnetic environments without introducing intolerable disturbances [55-60]. CM Impedance Identification: This section concentrates on identifying the CM impedance of three identical converters with the same power source but providing different types of charges - resistive, capacitive, and inductive. Analytical Modeling: Beginning with the elementary converter and progressing to the complete system, this section elucidates the dependence of DC micro-grid (DCMG) impedance on each converter, considering CM current propagation paths, topology, operating states, and cables [61-67], Simulation Testing and Experimental Validation: The fourth section focus on validating the analytical models through simulation testing and experimental validation. Finally, the paper concludes with a discussion of the results and their implications. This paper investigates the identification of common mode phenomena across all microgrid segments. By addressing these issues, we aim to enhance power system performance through improved power quality, reduced electromagnetic interference (EMI), and increased stability. Additionally, we expect to bolster control system robustness, optimize control performance, and prevent system malfunctions. The developed behavioral models, derived from generic electrical systems comprising passive components and voltage sources, empower engineers with predictions of electromagnetic disturbances. These mathematical models facilitate the optimization of DC micro-grid CM filters and the monitoring of micro-grids for enhanced performance and reliability.

2. GENERAL PURPOSE

A DC micro-grid (DCMG) system consists of a network of sources and loads connected by a number of converters. As shown schematically in Figure 1, three buck converters are connected to specific loads respectively (Z_{1_load} , Z_{2_load} and Z_{3_load}).

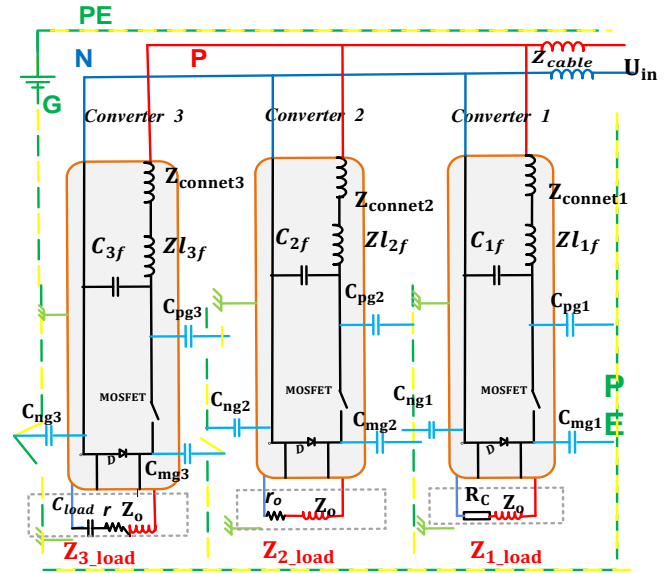


Figure 1. Model of the DC micro-grid system

This DC micro-grid topology finds widespread application across diverse sectors where ensuring safety and continuous power supply is paramount. These include critical infrastructure like hospitals, data centers, and military installations, as well as telecommunications networks, remote communities, maritime and offshore platforms, aerospace systems, industrial automation, renewable energy integration, and transportation.

In each of these domains, DC micro-grids play a crucial role in maintaining operational continuity, powering essential equipment, and managing power distribution effectively. Each converter incorporates a differential mode (DM); EMI filter at the input, consisting of a cell that combines an inductance (L_f), and a capacitance (C_f). The yellow-green dotted lines represent the Protective Earth "PE" conductor. All converter chassis should be connected together and grounded at the "G" point. This study addresses a critical challenge for DC micro-grid maintenance: real-time system monitoring and control. It proposes a methodology to identify and characterize a DCMG through elementary converter analysis. The first load (Z_{1_load}) represents resistive-inductive impedance; the second load (Z_{2_load}) is a self-inducing load with a dissipative series component. Finally, the third load (Z_{3_load}) is capacitive impedance with parasitic elements, including a small series resistance (R_s) and a small series inductance (L_c) connected in series; these impedances can be described respectively by the following equations [68-75]:

$$Z_1(\omega_p) = R_C + Z_o \omega_p \quad (1)$$

$$Z_2(\omega_p) = r + Z_o \omega_p \quad (2)$$

$$Z_3(\omega_p) = \frac{1}{C_{load} \omega_p} + r + Z_o \omega_p \quad (3)$$

where, ω_p is the signal frequencies within the system; Z_o is the impedance of the smoothing inductor; C_{load} is the capacity load. The element values of the impedances of the various components of the DC micro-grid system are identified by the Wayne Kerr Precision Impedance Analyzer (Model 6500B). As summarized in Table 1 below:

This study employs the widely used common and differential mode separation technique for electromagnetic compatibility (EMC) modeling of switching converters. By decoupling electromagnetic disturbances that propagate differently within a circuit, this method enables independent analysis. The underlying assumption of mode separation is valid under specific conditions:

- Frequency Range: Primarily applicable to switching frequencies and their harmonics, aligning with the study's focus on conducted disturbances.
 - Circuit Symmetry: Symmetrical circuit topologies, as exemplified in Table 1, facilitate accurate mode separation.
- Mode separation is a valuable tool for power electronics engineers, offering several advantages:
- Rapid assessment of a circuit's susceptibility to electromagnetic disturbances; especially in intricate systems. Effective design and implementation of filtering solutions.
 - Development of switching converters with reduced electromagnetic emissions.

Table 1. Values of the passive components of DC micro-grid system

Filter inductor (Z_{l_filter})		
$L_f=16.397 \mu\text{H}$	$r_{re}=35.110 \text{ k}\Omega$	$p_{ce}=32.182 \text{ pF}$
Filter capacitor (Z_{c_filter})		
$C_f=100 \mu\text{F}$	$s_{ie}=30 \text{ nH}$	$r_{se}=580 \text{ m}\Omega$
Smoothing inductor (Z_o)		
$L_c=1.61 \text{ mH}$	$p_{re}=119.5 \text{ k}\Omega$	$p_{ce}=79.6 \text{ pF}$
Capacitive load (Z_{3_load})		
$C_o=47 \mu\text{F}$	$s_{re}=300 \text{ m}\Omega$	$s_{le}=20 \text{ nH}$
Inductive load (Z_{2_load})		
$L_c=1.61 \text{ mH}$	$p_{re}=119.5 \text{ k}\Omega$	$p_{ce}=79.6 \text{ pF}$
Resistive load (Z_{1_load})		
	$R_c=20 \Omega$	$r_o=300 \text{ m}\Omega$
Connection cable (Z_{1_cable})		
$L_{cable}=1.5 \mu\text{H}$	$s_{re}=600 \text{ m}\Omega$	
Stray capacitance		
$C_{pg}=5 \text{ pF}$	$C_{ng}=5 \text{ pF}$	$C_{mg}=10 \text{ pF}$

3. ANALYTICAL MODELING

The Common Mode propagation current takes the PE conductor as a link between different systems, knowing that safety standards IEC 60364 require that all metals (chassis) should be grounded to guarantee the persons and materials safety [76]. This grounding arrangement is crucial for all electrical installations whether it is alternative (AC) or continuous (DC). Figure 2 shows the general operating principle of a common mode current propagation system; the CM current (I_{cm}) propagates within all system's conductors in the same direction and returns through the ground conductor "G"

or PE". The CM voltage (V_{cm}) is measured among the frame and the two active conductors positive "P" and negative "N", which consequently defines two impedances referenced to the ground. The first one (Z_{pg}) is defined between the positive and the ground conductor, the second impedance (Z_{ng}) is defined between the negative and the ground conductor. The capacitive crosstalk effects caused by the previously mentioned parasitical capacities contribute to the impedance expression of (Z_{pg}) and (Z_{ng}) [63-67, 72].

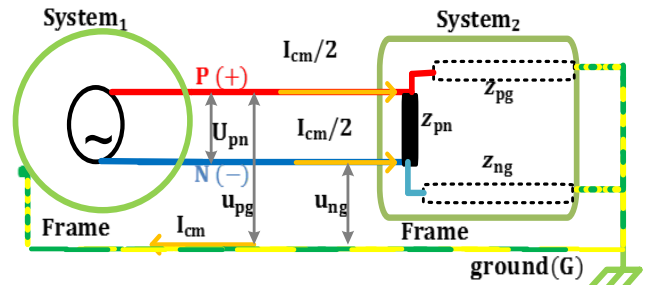


Figure 2. Common mode (CM) current propagation

3.1 Common mode impedance of the elementary converter connected to the micro-grid

Figure 3 illustrates the schematic used to calculate the common mode (CM) impedance of one of the three buck converters connected to the tested micro-grid, as shown in Figure 1 above. The employed method, known as the voltage-current (U-I) method, involves injecting a small signal voltage, as it is mentioned below in Eq. (4) into the buck converter and subsequently measuring the response [68-75].

The parasitic capacitances between the two active conductors, positive "+" and negative "-", and the ground conductor "G" are represented respectively by (C_{pg1}) and (C_{ng1}), along with the floating capacitance (C_m); which varies based on the state of the static switch of MOSFET and the diode "D" [68-75]. It is important to note that these components are clearly identified on the buck circuit diagram as indicated in Figure 3 below.

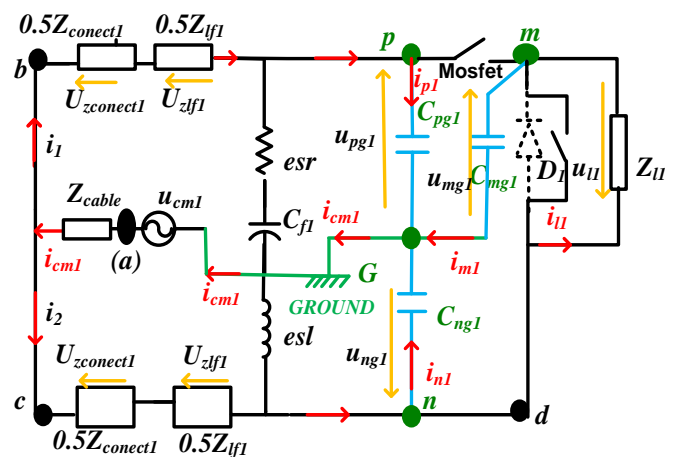


Figure 3. Elementary buck converter scheme under study

Switching States

Online State: For a converter to be online, two conditions must be met: The converter must be powered on, the static switches of the converter must be actively controlled, or the

static switches are fixed in the closed position.

Offline State: This state is met if one of the following conditions occurs: The converter is powered "off", the static switches are fixed in the open position.

The small sinusoidal signal of the voltage injected into the buck converter is given by [68-75]:

$$u_{p1}(t) = \frac{e^{j\omega_p t} - e^{-j\omega_p t}}{2j} \quad (4)$$

The common mode model is represented by impedance (Z_{cm1}) connected to the voltage source; it is given by the equation [68-75]:

$$Z_{cm1} = \frac{v_{cm1}}{i_{cm1}} \quad (5)$$

In this subsection, the CM impedance calculation (Z_{cm1}) will be computed using expression defined by Eq. (5). In the method based on the balanced impedance hypothesis [APEC ALES]; the current (i_i) is considered equal to half of the current (i_{cm1}) expressed by Eq. (6), while the Eq. (7) representing the sum of the current (i_{cm1}) in the derived branches. In the electrical circuit shown in Figure 3, the currents (i_{p1}) and (i_{n1}) respectively given by Eqs. (8) and (9) circulate respectively in the impedances (Z_{pg1}) and (Z_{ng1}) presented by the capacitors (C_{pg1}) and (C_{ng1}); the voltages (U_{pg1}) and (U_{ng1}) respectively appear across the terminal points "P" and "G" and "n" and "G". The current (i_{m1}) expressed in Eq. (10) corresponds to the current circulating through the impedance (Z_{mg1}) of the capacitance (C_{m1}) as a function of the switching cell, it is defined from the voltage (U_{mg1}) between the two points "m" and "G", as depicted in Figure 3.

$$i_i = \frac{i_{cm1}}{2} \quad (6)$$

As current is conserved; the current supplying (i_{cm1}) is given by the equality presented in the following equation:

$$i_{cm1} = i_{p1} + i_{n1} + i_{m1} \quad (7)$$

These currents which circulate in the branches are obtained respectively by the equations mentioned below [68-75]:

$$i_{p1} = \frac{u_{pg1}}{Z_{pg1}} \quad (8)$$

$$i_{n1} = \frac{u_{ng1}}{Z_{ng1}} \quad (9)$$

$$i_{m1} = \frac{u_{mg1}}{Z_{mg1}} \quad (10)$$

The voltage (v_{pg1}) expression of the circuit constituting the closed loop "abpGa" is established as follows:

$$u_{pg1} = u_{cm1} + (Z_{lf1} + Z_{cable1})i_{cm1} \quad (11)$$

Analogously, the voltage (U_{ng1}) across the closed loop "acnGa" is expressed mathematically as follows:

$$u_{ng1} = u_{cm1} + (Z_{lf1} + Z_{cable1})i_{cm1} \quad (12)$$

Concerning the state of the loop circuit "acndmGa"; when both switches are open, the expression of voltage (U_{mg1}) is represented by Eq. (13) below. It should be noted that when both switches are opened simultaneously, the converter operation case is called offline case.

$$u_{mg1} = u_{cm1} + (Z_{lf1} + Z_{connect1})i_{cm1} + u_{l1} \quad (13)$$

In the case where the diode is closed, according to the loop circuit "acndmGa", as shown in Figure 3, the voltage U_{mg1} expression is established as given by Eq. (14):

$$u_{mg1} = u_{pg1} = u_{cm1} - (U_{Z_{connect1}} + U_{zf1l}) \quad (14)$$

However, when the diode is open, according to the loop circuit "abpmGa", the voltage (U_{mg1}) expression is described by Eq. (15):

$$u_{mg1} = u_{ng1} = u_{cm1} - (U_{Z_{connect1}} + U_{zf1l}) \quad (15)$$

These both Eqs. (14) and (15) make it possible to describe the possible operating case to be studied; the online operation of the converter. Besides, when the converter is offline, the load voltage and current are respectively expressed bellow as follows [68-75]:

$$u_{l1} = Z_o i_{l1} \quad (16)$$

where, Z_o is the load impedance.

The current (i_{l1}) is equal to the value previously given by Eq. (10):

$$i_{l1} = i_{m1} \quad (17)$$

However, when the diode is closed, it shorts the load, it can be deduced that presented below in Eq. (18).

$$u_{l1} = 0V \quad (18)$$

Indeed, it can be noted that the circuit loop "acndmGa" impedance (Z_{dmG}) changes if the state of the converter changes. Therefore; it can be modelled the state of the converter (online or offline) with a defined function (Q_{sw}) called state function, as expressed in Eq. (19).

$$\begin{cases} Q_{sw} = 1, (\text{online mode}) \\ Q_{sw} = 0, (\text{offline mode}) \end{cases} \quad (19)$$

When the converter is offline, the diode is open. So the both impedances (Z_{l1}) and (Z_{mg1}) are in series; they are crossed by the same current. Otherwise, if the converter is online, the voltage (v_{l1}) is zero. Consequently, it is possible to combine the impedance (Z_{dmG}) of the converter in both cases of online

and offline operation; as illustrated in Figure 3 following the "acndmGa" loop circuit and expressed by Eq. (20):

$$Z_{dmG1} = Z_{Cmg1} + Q_{sw}(t) Z_{l1} \quad (20)$$

Consequently, it can be analytically expressed the common mode current (CM) flowing in the circuit by Eq. (21):

$$i_{cm1} = \frac{u_{ng1}}{Z_{ng1}} + \frac{u_{pg1}}{Z_{pg1}} + \frac{u_{mg1}}{Z_{dmG1}} \quad (21)$$

Knowing this current and substituting it into Eq. (5), it can be deduced the CM impedance expression of the single converter as shown below in Eq. (22).

$$Z_{cm1} = \left[\begin{array}{l} \frac{1}{(C_{ng1} + C_{pg1})p + Z_{dmG1}} \\ + \frac{1}{2}(Z_{lf1} + Z_{conect1}) + Z_{cable} \end{array} \right] \quad (22)$$

3.2 CM impedance modeling of the whole DC micro-grid

This subsection identifies the DCMG modeling system shown in the previous Figure 3, which was analyzed and its CM Impedance expression calculated as indicated by Eq. (22).

Figure 4 presents the current propagation paths (i_{cm}) in the DCMG; the terms (i_{cm1} , i_{cm2} and i_{cm3}) respectively express the common mode currents of converters 1, 2 and 3; as mentioned in Eq. (23).

$$i_{cm} = i_{cm1} + i_{cm2} + i_{cm3} \quad (23)$$

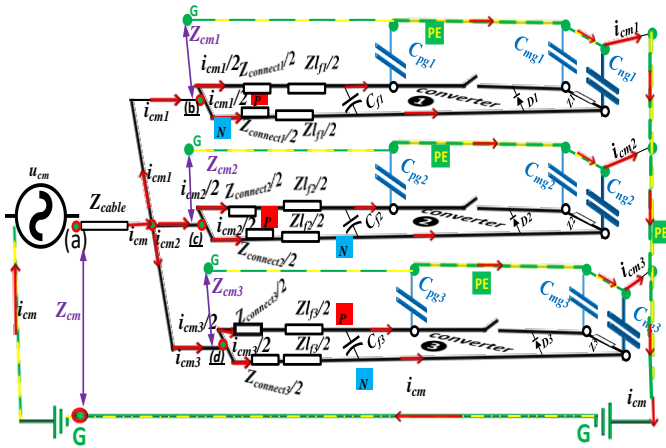


Figure 4. DCMG model of common mode current propagation paths

According to this figure of the common mode load equivalent model; it can be distinguished the CM electrical parameters as follows [68-75]:

- (u_{cm} and Z_{cm}) are respectively the applied voltage of the source and the input impedance of the DCMG connected between points "G" and "a".
- (u_{cm1} and Z_{cm1}) are respectively the voltage in converter 1 and the impedance between points "G" and

"b".

- (u_{cm2} and Z_{cm2}) are respectively the voltage in converter 2 and the impedance between points "G" and "c".
- (u_{cm3} and Z_{cm3}) are respectively the voltage in converter 3 and the impedance between points "G" and "d".

The DCMG impedance is calculated as follows [68-75]:

$$Z_{cm} = \frac{u_{cm}}{i_{cm}} \quad (24)$$

Substituting Eqs. (21) and (23) into Eq. (24), the following expression is obtained:

$$Z_{cm} = \frac{u_{cm}}{\frac{u_{cm1}}{Z_{cm1}} + \frac{u_{cm2}}{Z_{cm2}} + \frac{u_{cm3}}{Z_{cm3}}} \quad (25)$$

As indicated in Figure 4, the voltage are equal, then it can be obtained:

$$u_{cm} = u_{cm1} = u_{cm2} = u_{cm3} \quad (26)$$

Consequently, after reduction and simplification, it can be directly yielded the following expression:

$$Z_{cm} = \frac{1}{\frac{1}{Z_{cm1}} + \frac{1}{Z_{cm2}} + \frac{1}{Z_{cm3}}} \quad (27)$$

According to Table 1, the values of the parasitic capacitors, the connections, and the impedance of the filter are identical; the following expression can be written:

$$Z_{cm} = Z_{cm1} = Z_{cm2} = Z_{cm3} \quad (28)$$

Then; it can be concluded that:

$$Z_{cm} = \frac{Z_{cm1}}{3} \quad (29)$$

By combining Eqs. (22) and (29), Eq. (30) is derived which refers to the general form of the electrical model:

$$Z_{cm} = \left[\begin{array}{l} \frac{1}{K \cdot (C_{ngk} + C_{pgk})p + \sum_{i=1}^{i=n} Z_{dmGi}} \\ + \frac{1}{2(k+i)}(Z_{lf} + Z_{conectic}) + Z_{cable} \end{array} \right] \quad (30)$$

where, k is the number of online converters, this variable signifies the number of converters presently in operation; i is the number of offline converters, this variable denotes the number of converters currently not in operation.

The equivalent electrical model of the DC micro-grid system, illustrated in Figure 5 and elucidated in Eq. (30), provides a comprehensive representation of its entire

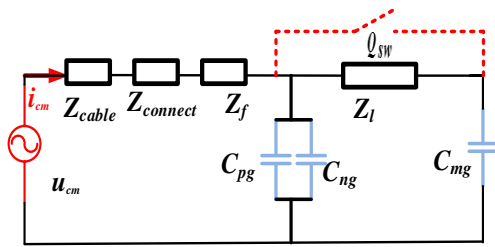


Figure 5. Electrical model of the DCMG

The Q_{sw} parameter indicates the converter's state during offline operation. Z_{cable} , $Z_{connect}$, Z_f , C_{ng} , C_{pg} , Z_l , and C_{mg} are the circuit elements of DCMG system.

4. PSPICE VALIDATION AND MEASUREMENT METHODOLOGY

4.1 PSpice simulation

The equivalent circuit illustrated in Figure 4 was simulated using PSpice Software Version 17.2-2016 P010. Measurements of converter components, including inductances, capacitors, and the load, were carried out with the 65120B precision impedance analyzer. To incorporate parasitic elements into the simulated circuit, as indicated in Table 1, an AC signal source was employed to inject frequencies incrementally, ranging from a few Hertz up to 120 MHz. The common mode (CM) impedance was determined for each injected frequency, as specified by Eq. (4).

4.2 Measurement methodology

Impedance measurements were performed using a high-precision WAYNE KERR 65120B impedance analyzer, with the system completely offline. The measurement was carried out on the set of MG converters, cables, and loads by switching converters. A solder was placed between drain and source to simulate a closed static switch (MOSFET).

The experimental test bench designed for this study is presented in Figure 6. It is composed of:

- Three converters (DCMG)
- Plane connected to the ground
- Impedance Analyzer

This study aimed to test the impedance measurements and to complete and validate the CM models of a DC micro-grid.

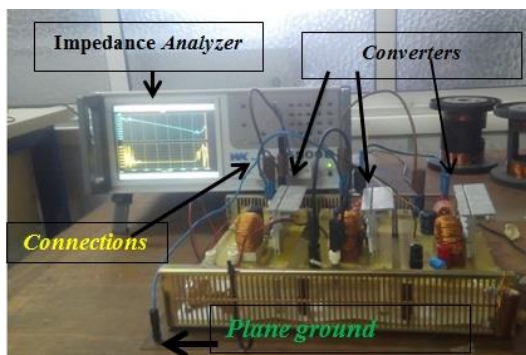


Figure 6. Test bench

5. RESULT AND DISCUSSION

This study consists of validating a novel analytical model to determine the common mode impedance (CMI) of a micro-grid DC model. This comprehensive model simultaneously takes into account the influence of parasitic capacitances, load impedance and filter inductances. It thus allows a more profound comprehension of the behavior of the common mode impedance. The model's accuracy has been rigorously validated through PSpice simulations and impedance analyzer measurements to reinforce and verify its reliability and performance.

Figure 7 contrasts the performance of two distinct converters sharing identical filter and connection configurations but differing in parasitic capacitance values. The figure elucidates the interplay between parasitic capacitance and the resulting impedance response. A low parasitic capacitance can obscure the first resonance peak associated with the load impedance, dominating the overall curve. Conversely, a higher parasitic capacitance permits the load impedance to emerge, revealing the initial resonance. Consequently, a low parasitic capacitance effectively acts as a shunt, masking the load's influence, as exemplified by the indistinguishable online and offline impedances.

Figure 8 represents the common mode impedances of the frequency of an elementary converter of a microgrid (DCMG); in correlation with the systems reported in Figures 3 and 4.

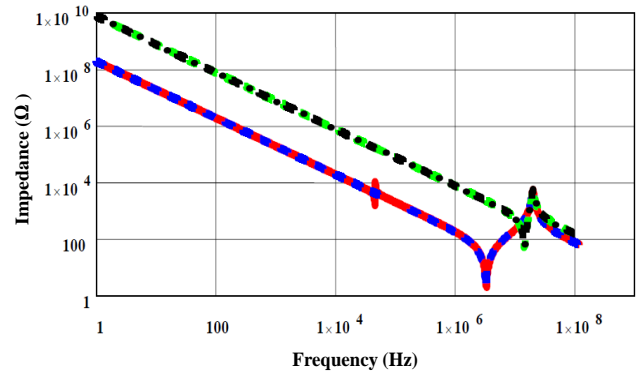


Figure 7. CM impedance spectrum of the first converter under study;(Green) online and (Black) offline; Z_{cm} with ($C_{ng}=C_{pg}=5$ pF and $C_m=10$ pF). Second converter (Blue) online and (Red) offline; Z_{cm} with ($C_{ng}=C_{pg}=200$ pF, and $C_m=400$ pF)

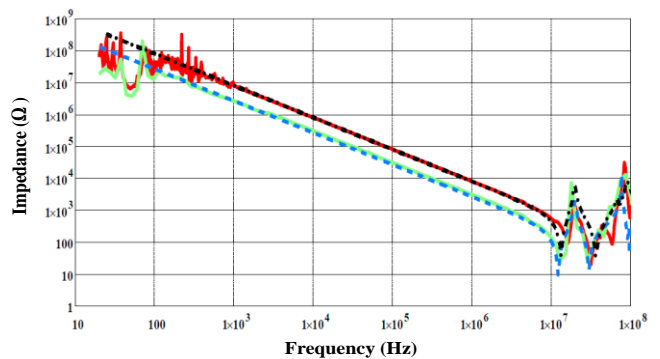


Figure 8. Z_{CM} impedance of the elementary converter simulation model in (Blue), the measured model in (Green), the DCMG represented by the simulated model in (Red), and the measured model in (Black)

The plot visualized over the frequency range from 100Hz to 120 MHz, emphasizing the effects of different parasitic components on the overall behavior. As shown in this figure; it can be directly distinguished several types of intervals:

Interval of 100 Hz to 14.5 MHz: This segment is primarily influenced by parasitic capacitances: (C_{ng} , C_{np} , and C_m). For the DCMG, CMI arises from the parallel connection of the input capacities of the elementary converters, exerting the most significant influence in the range from 1Hz to 14,5 MHz.

Interval of 14,5 MHz to 30 MHz: In this frequency band, the impact of filter inductance likely becomes more prominent.

Interval of 30 MHz to 70 MHz: This range may see effects from the characteristics of the printed circuit board (PCB) and its connectors.

Interval of 70 MHz to 120 MHz: The response in this higher frequency spectrum is probably influenced by the impedance of the wiring used to connect the DCMG converters.

Figure 9 presents a detailed comparison between simulation results, measured data and theoretical analysis curves for the characteristic impedance of the DCMG. The excellent agreement between these three datasets underlines the robustness and accuracy of the developed model.

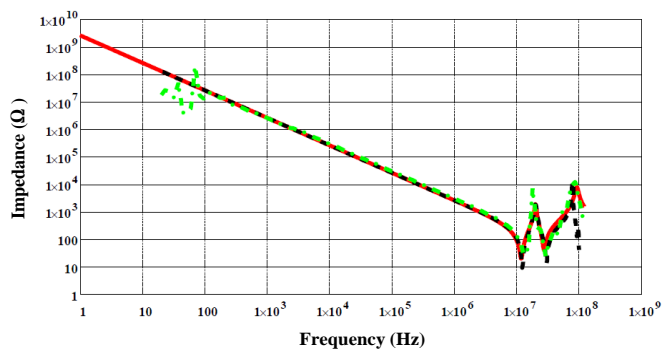


Figure 9. CM impedance representation; (Red) analytical model, the (Green) measured model, and the (Black) present the simulation model of DCMG

Key points and interpretations

Model validation: The close correlation between simulation results, experimental measurements and theoretical predictions confirms the validity of the model to describe the behavior of the DCMG characteristic impedance over a wide frequency range.

Parasitic component effects: The analysis of Figure 9 allows to identify the influence of different parasitic components on the impedance in different frequency bands:

- 100 Hz to 14.5 MHz: Domination of parasitic capacitances (C_{ng} , C_{np} and C_m), in particular the input capacitance of the converters.
- 14.5 MHz to 30 MHz: Increasing influence of the filter inductance.
- 30 MHz to 70 MHz: Effects of PCB and connector characteristics.
- 70 MHz to 120 MHz: Wiring impedance dominance.

Model limitations: The slight discrepancies observed between 70 MHz and 120 MHz are attributed to interference between conductors and the PCB. These minor deviations highlight that even the most accurate models may have limitations under specific conditions.

Model scope: The results suggest that the model is applicable to a wide range of voltages in microgrids and is not limited to low voltage.

6. CONCLUSION

A DCMG consists of a network of sources and loads connected by a number of power electronic converters. It is more important to identify the common mode impedance of the DC micro-grid in order to effectively reduce electromagnetic interference (EMI) between electronic equipment and control the possible effects. An advantage presented to the knowledge of common mode impedance, it allows the paths of unwanted currents to be discerned, thus facilitating the design of preventive and corrective measures. This promotes the development of more robust, reliable and compliant systems. This study presents a novel approach to identify common mode impedance for DC micro-grids. The effectiveness of this approach was confirmed by numerical simulations and real measurements in various operational scenarios, including online and offline modes, with different load distribution configurations. While this study underscores the significance of CMI analysis in DC microgrid design, it is crucial to acknowledge the limitations of the mode separation hypothesis, which underpins the proposed methodology. Factors such as circuit asymmetry, non-linear components, and radiated perturbation high-frequency phenomena can compromise the accuracy of this assumption. Future research should focus on refining the model to incorporate these complexities and expanding its applicability to a wider range of operating conditions.

This analysis underscores the influence of system layout and components on common mode impedance, particularly the interaction between stray capacitances, load impedance and filter inductances. Crucially, this approach remains adaptable to different contexts, accommodating variations in grid voltage, micro-grid structure, and external electromagnetic interference disturbances. This adaptability renders it a valuable tool for optimizing DC micro-grid design.

This study sets the stage for further exploration. One promising avenue for future work involves integrating CMI analysis into established DC micro-grid design methodologies. This could entail devising design guidelines or optimization algorithms that consider CMI alongside other pivotal factors like power flow and efficiency. Additionally, future research could delve into how the proposed CMI identification method can diagnose and alleviate EMI issues in existing DC micro-grid installations. By incorporating CMI analysis into routine maintenance procedures, the enduring performance and reliability of these prevalent systems can be continuously and increasingly safeguard.

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NOMENCLATURE

AC	alternating current
CM	common mode
CMI	common mode impedance
DC	direct current
DCMG	direct current micro-grid
DM	differential mode
EMC	electromagnetic compatibility
EMI	electromagnetic interference
G	ground point
IEC 60364	international electrotechnical commission standard on electrical installations of buildings
LV	low voltage
MG	micro-grid
MOSFET	metal oxide semiconductor field effect transistor
N	negative active conductor
P	positive active conductor
PCB	printed circuit board
PE	protective earth conductor
Qsw	state function