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Design Optimization of CMOS Folded Cascode OTA Using Water Cycle Algorithm for Enhanced Performance

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ABSTRACT

The growing need for high-performance folded cascode CMOS OTAs in various fields, such as electronics and communications, requires them to operate with wide bandwidth, high voltage gain, compact devices, and low power consumption. Recent research indicates that implementing the water cycle algorithm (WCA) can greatly improve the performance of the folded cascode CMOS operational transconductance amplifier (OTA). This is due to the WCA's ability to perform both global search and local exploration efficiently. Notably, the OTA in question is constructed using 0.18µm TSMC technology and operates with a voltage supply of ±1.8V. The results of the simulation were collected using PSPICE software (version 17.4). These design solutions demonstrate exceptional efficiency, delivering significant amplification, high frequency, and minimal power usage. In addition, the paper demonstrates the implementation and simulation outcomes of a folded cascode CMOS operational transconductance amplifier utilizing the water cycle algorithm, MATLAB was employed for this purpose. Using WCA in the design of an OTA for folded cascode CMOS OTA results in significant improvements in performance metrics. Experiences a significant increase in voltage gain, with an increase in gain bandwidth by a factor of five compared to the algorithm-free design. In addition, power consumption is reduced by 15.5%, and the common mode rejection ratio is improved by 15.18% compared to the non-WCA folded cascode CMOS OTA design. The results highlight the effectiveness of the WCA technique as a powerful optimization strategy to improve the performance of folded cascode CMOS OTA.

1. INTRODUCTION

Using operational amplifiers has become increasingly important in analog circuit design due to their high gain and direct connection. Typically, they consist of a level transistor, a differential amplifier stage, and an output stage [1]. The prevalence of Complementary Metal-Oxide Semiconductor (CMOS) technology over bipolar technology in analog circuit design for mixed signal systems is primarily driven by the industry's inclination to integrate analog and digital circuits on a single chip utilizing common process technologies [2]. Modern technologies that reduce the size of the transistor provide many benefits and advantages needed by many applications. Among these benefits are increased integration density, reduced energy consumption, as well as improved performance, in addition to cost efficiency and other benefits.

Digital CMOS technology manufactures the majority of analog integrated circuits. Over the years, the efficiency of digital CMOS circuits has enhanced due to advancements in digital technology. Digital technology has consistently reduced the minimal feature size, enabling the construction of digital circuits with smaller dimensions, increased speed, and reduced parasitic effects. However, manufacturers continue to manufacture analog circuits with greater channel lengths to optimize circuit performance [3]. Scalability is a characteristic of digital circuits, which allows for the adaptation of the same circuit to a more advanced technology over time with minimal modifications. However, while transitioning from an older to a newer technology in analog circuits, it is necessary to reconfigure the aspect ratios of most transistors in order to preserve the desired performance.

Several designs of CMOS op-amps can be found in Accepted Manuscript literature, all of which aim to optimize their performance parameters. Genetic algorithm, particle swarm optimization, simplex-PSO, modified cuckoo optimization algorithm, hybrid whale particle swarm optimization, aging leader and challenger PSO (ALC-PSO), and colliding bodies optimization (CBO) are just some of the methods utilized to optimize the dimensions of each transistor and enhance the performance of op-amps for design the analog and mixed-signal integrated circuit [4-11]. The improvements reported in more research papers demonstrate that certain performance parameters have been enhanced. However, it is evident that other parameters still require further optimization.

The key challenge in this design is to strike a balance between the various performance metrics, such as gain, bandwidth, noise, power consumption, and linearity, while ensuring the OTA can function effectively in high-frequency domains. Careful transistor sizing, biasing techniques, compensation methods, and other circuit design strategies may

be employed to address this challenge and further improve the overall performance of the folded-cascode CMOS OTA.

In this paper, the WCA algorithm was employed to enhance the performance characteristics of the proposed folded cascode CMOS OTA. The performance of the folded cascode CMOS OTA was compared with and without the WCA algorithm. The simulation results indicated that the proposed design developed using the WCA method exhibited superior performance parameters, thus demonstrating the effectiveness of the WCA algorithm.

2. DESIGN OF FOLDED CASCODE CMOS OTA

This circuit amplifier consists of two types of cascode CMOS OTAS. The first one is the telescopic cascode CMOS OTA which is realized using one-stage input differential pair MOS transistors and a tail current transistor which connected in series with two legs of cascoding MOS transistors to increase the output impedance of OTA [12]. This will improve DC voltage gain, output impedance, slew rate, and settling time of OTA. This technique suffers from the limitation on the output voltage swings and input voltage common-mode range due to cascoding MOS transistors in series with the input differential pair MOS transistors [13]. The second type of cascode CMOS OTA is the folded cascode CMOS OTA as shown in Figure 1. The configuration of this technique uses input differential pair MOS transistors and output folded cascoding MOS transistors [14]. The steps to design of folded cascode CMOS OTA are shown in the following points [15, 16].

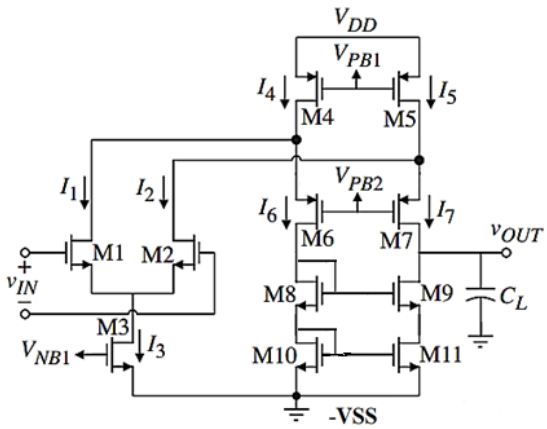


Figure 1. Schematic of folded cascode CMOS OTA circuit diagram [16]

- Slew Rate:

$$SR = I_3/C_L \tag{1}$$

- In output cascades the bias currents:

$$I_5 = I_4 = 1.2I_3 \; to \; 1.5I_3 \tag{2}$$

- Maximum output voltage

$$S_5 = 2I_5/K_P V_{DS5}^2, S_7 = \frac{2I_7}{K_P V_{DS7}^2}, (S_4 = S_5 \; \& \; S_6 = S_7)$$
$$V_{DS5(sat)} = V_{DS7(sat)} = 0.5\big(V_{DD} - V_{out(max)}\big) \tag{3}$$

- Minimum output voltage:

$$S_{11} = \frac{2I_{11}}{K_N V_{DS11}^2}, S_9 = \frac{2I_9}{K_N V_{DS9}^2}, (S_{10} = S_{11} \; \& \; S_8 = S_9)$$
$$V_{DS9(sat)} = V_{DS11(sat)} = 0.5(V_{out(min)} - V_{SS}) \tag{4}$$

- Gain bandwidth

$$(\text{GB}) = \frac{g_{m1}}{C_L}, S_1 = S_2 = \frac{g_{m1}^2}{K_N I_3} = GB^2 C_L^2 / K_N I_3 \tag{5}$$

- Minimum input CM

$$S_3 = \frac{2I_3}{K_N\left(V_{in(min)} - V_{SS} - \sqrt{\frac{I_3}{K_N S_1}} - V_{th1}\right)^2} \tag{6}$$

- Maximum input CM

$$S_4 = S_5 = 2 * \frac{I_4}{K_P\{V_{DD} - V_{in(max)} + V_{th1}\}^2} \tag{7}$$

S_4 and S_5 must satisfy or surpass the specified value of step Eq. (3).

- Power dissipation:

$$\text{P}_{diss} = (V_{DD} - V_{SS})(I_3 + I_{10} + I_{11}) \tag{8}$$

- Differential voltage gain,

$$AV = \frac{V_{out}}{V_{in}} = (\frac{2+K}{2+2K}) g_{m1} R_{II}$$
$$K = \frac{R_9(g_{ds2} + g_{ds4})}{g_{m7}\, r_{ds7}}, R_9 = g_{m9}\, r_{ds9} r_{ds11}$$
$$R_{II} = R_9 \parallel [g_{m7}\, r_{ds7}(r_{ds2} \parallel r_{ds5})] \tag{9}$$

- Biase voltage

$$\text{V}_{\text{PB1}} = \text{V}_{\text{DD}} - (\text{V}_{\text{OD5}} + \text{V}_{\text{th5}}) \tag{10}$$

$$\text{V}_{\text{PB2}} = \text{V}_{\text{DD}}(|\text{V}_{\text{GS3}}| + |\text{V}_{\text{OD5}}|) \tag{11}$$

The input differential MOS transistors are connected to a tail current source MOS transistor. This topology is very suitable for high input common-mode voltage range, high output swings, large voltage gain Av, high gain bandwidth product (GB), and large slew rate (SR) due to the cancellation of extra phase shift that is required by the second stage of the conventional two stages CMOS OTA.

3. WATER CYCLE ALGORITHM (WCA)

One of the phenomena that occur in nature is the water movement between rivers and streams towards the ocean. This phenomenon is called the water cycle [17]. River water, water resulting from the photosynthesis of plants, melting snow, groundwater, and rainwater resulting from the evaporation of river and lake water, all collect in the sea in a sequence of states called the water cycle as in Figure 2 and its flow chart in Figure 3. While in Table 1, the parameters of input for the optimization process are outlined.

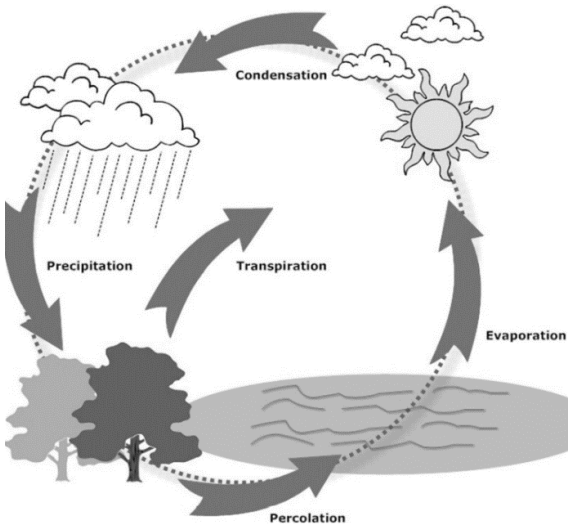


Figure 2. A simplified schematic illustrating the hydrologic cycle (water cycle) [18]

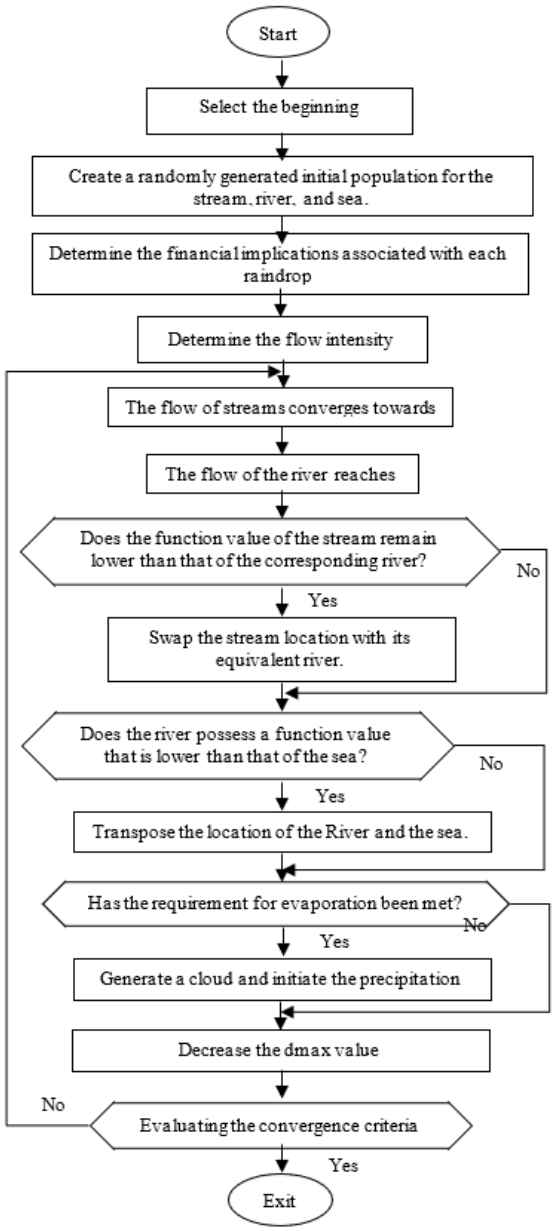


Figure 3. Flowchart of WCA [19]

Table 1. Parameters of WCA

No.	INPUTS Algorithm Parameter	Value	Parameter Definition
1	Nvars	3	Number of design variables
2	Npop	200	Population size
3	Nsr	8	Number of rivers + sea
4	dmax	1e-20	Evporation condition constant
5	Max_it	1000	Maximum number of iterations

The WCA initial population consists of raindrops that occur during rain or precipitation. A single raindrop is considered to be a part of the sea. The valuable rains symbolize the rivers. The residual raindrops are the tributaries that flow into the rivers and, ultimately, the ocean.

A single solution or a raindrop of the optimization problem in WCA terms is represented by a $1 \times N_{var}$ dimensional array, as specified below [20]:

$$Raindrop = [X_1, X_2, \dots, X_{N_{var}}] \tag{12}$$

The optimization problem dimension is N_{var}.

The raindrop cost functions (Cost) is determined by:

$$Cost_i = \int (X_1, X_2, \dots, X_{N_{var}}), i = 1,2, \dots, N_{pop} \tag{13}$$

where, the raindrop counts is stored in N_{pop}.

The direction of rainwater flow, whether it goes into the sea or rivers, is determined by the equation, which takes into account the intensity of the flow:

$$NS_n = round\left\{\left|\frac{Cost_n}{\sum_{i=1}^{N_{sr}} Cost_i}\right| * N_{\text{Raindrops}}\right\}, \quad n = 1,2, \dots, N_{sr} \tag{14}$$

where, N_{sr} is the single sea and river's total number. $N_{\text{Raindrops}}$ refers to the remaining portion of the population, specifically those raindrops that fall directly into the sea or rivers.

$$N_{\text{Raindrops}} = N_{pop} - N_{sr} \tag{15}$$

The raindrops give rise to the formation of streams. The streams serve as tributaries that give rise to rivers or directly discharge into the ocean. The sea, being the most optimal destination, serves as the final terminus for all streams and rivers. The assessment of the new location for the rivers and streams is conducted by:

$$X_{Stream}^{i+} = X_{Stream}^{i} + rand * C * (X_{River}^{i} - X_{Stream}^{i}) \tag{16}$$

$$X_{River}^{i+} = X_{River}^{i} + rand * C * (X_{Sea}^{i} - X_{River}^{i}) \tag{17}$$

Assuming that C is a variable that can assume values between 1 and 2, and rand is a uniformly distributed random number between 0 and 1.

The roles of the stream and the river can be reversed if the solution presented by the stream is more effective than the solution represented by the river. Similarly, the sea and the

rivers can also interchange their roles. The parameter d_{max} has a significant influence on determining whether further exploration around the sea, which represents the best solution, should be promoted or discouraged [21]:

$$d_{max}^{i+1} = d_{max}^{i} - \frac{d_{max}^{i}}{Iter\_max} \quad (18)$$

Precipitation follows the process of evaporation. The formation of new streams occurs when fresh raindrops accumulate in certain designated locations:

$$X_{stream}^{new} = LB + rand * (UB - LB) \quad (19)$$

In the given problem, the upper and lower limits of the search parameters are denoted by UB (Upper Bound) and LB (Lower Bound), respectively. These limits define the range within which the search algorithm explores and evaluates potential solutions.

4. SPECIFICATIONS AND DESIGN PROCEDURE

To ensure accurate representation and analysis of the folded cascode CMOS OTA, several design parameters and specifications are outlined in Tables 2 and 3, respectively. Table 2 presents the design parameters, encompassing various aspects such as supply voltage, bias currents, and capacitor values. Channel length and channel width (transistor dimensions) play an important role in improving performance parameters. The focus of the design appears to be on a folded-cascode CMOS Operational Transconductance Amplifier (OTA) targeted for high-frequency applications. These high-frequency applications may include Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), universal filters, and other circuits that operate at elevated frequencies [22].

Table 2. Folded cascode CMOS OTA specifications

Design Parameters	Values with Units
Voltage Gain	>70 dB
Gain Bandwidth	>40MHz
Slew Rate	>35V/µsec
Supply Voltage (VDD, VSS)	±1.8V
Input Common Mod Range	-0.95 to +1 V
Phase Margin	≥ 55 °
Load Capacitor	0.5pF
I bias	25uA

Table 3. Folded cascode CMOS OTA aspect ratios of transistors for designed with and without WC

Number of Transistor	Gate Width (µm) W	Gate Width (µm) W (WCA)	Channel Length L (µm)
W1,2	0.725	29.53	0.18
W3,12	1.008	0.3474	0.18
W4,5	3.75	3.708	0.18
W6,7	2.435	2.17	0.18
W8,9,10,12	0.845	0.752	0.18

In order to utilize the WCA for optimization in MATLAB, it is necessary to incorporate the parameters to be optimized into the fitness equation, as depicted in Eq. (20). The WCA performs a predetermined number of iterations as specified by the user. The findings generated by the WCA can be utilized in the PSPICE program to assess the performance metrics of the Folded Cascode CMOS OTA. These criteria include minimum power consumption, gain bandwidth, voltage gain, and common mode rejection ratio (CMRR). This iterative procedure can be reiterated until the desired result of reduced power consumption, elevated voltage amplification, and enhanced gain bandwidth is attained while upholding a consistent bias current. Using these optimized parameter values, the transistors can be redesigned with enlarged dimensions. Integrating the WCA with the Folded Cascode CMOS OTA optimization allows for systematic design refinement and the achievement of higher performance. The synergy between the WCA and the PSPICE program facilitates the evaluation and refinement of the Op-Amp's performance parameters, leading to the identification of optimal transistor dimensions that result in enhanced overall circuit performance.

$$\text{Fitness function} = \frac{(\frac{1}{\text{Pdiss}} + GB) - (\text{Pdiss} + \frac{1}{GB})}{2} \quad (20)$$

Table 3 shows detailed information about the dimensions of the transistor used in the design. By based on the process parameters in Table 2 and using the Eq. (1) to Eq. (6), we can found the aspect ratio of all transistors as in Table 3, Such tables have an important role in configuring and evaluating the performance of folded cascode CMOS OTA, as they are considered a reference point for accurate evaluation using SPICE simulation.

Once the WCA optimization process is completed using the MATLAB (R2021b) program, improved results for performance parameters are obtained. The three parameters (S_1, V_{DS}, and X) are found by algorithm, and by based on these values, we can find all parameters as shown:

$$S_{1,2} = 164.07 \Rightarrow w_{1,2} = 0.18 * 164.07 = 29.53\mu m$$

$x = 1.2$, x is the ratio of current in $M_{4,5}$ ($I_{4,5}$) to bias current I_3 in Eq. (2):

$$V_{DS} = 0.185V, \text{ where } V_{DS} = V_{DS5} = V_{DS7} = V_{DS9}$$

where, $S_{1,2}$, V_{DS}, and x are found by the algorithm. And by based on these values, we can find all parameters as follow:

$$I_5 = I_4 = 1.2I_3 \text{ to } 1.5I_3 = x * 25 = 1.201 * 25 = 30.025\mu A$$

$$I_7 = I_{4,5} - I_{1,2} = 30.025 - 12.5 = 17.525\mu A$$

$$GB = \frac{\sqrt{S_{1,2} * K_N I_3}}{C_L} = \frac{\sqrt{164.07 * 245 * 10^{-6} * 25 * 10^{-6}}}{2\pi * 0.5 * 10^{-12}} = 319.1MHZ$$

$$S_3 = \frac{2 * 25 * 10^{-6}}{245 * 10^{-6}\left(-0.95 + 1.8 - \sqrt{\frac{25 * 10^{-6}}{245 * 10^{-6} * 164.07}} - 0.5\right)^2} = 1.93 \Rightarrow W_3 = 0.18 * 1.93 = 0.3474\mu m$$

$$S_{4,5} = \frac{2 * 30.025 * 10^{-6}}{85 * 10^{-6} * 0.185^2} = 20.6 \Rightarrow W_{4,5} = 0.18 * 20.6 = 3.708$$

$$S_{6,7} = \frac{2 * 17.525 * 10^{-6}}{85 * 10^{-6} * 0.185^2} = 12.05 \Rightarrow W_{6,7} = 0.18 * 13.53 = 2.17\mu m$$

$$S_{8,9,10,11} = \frac{2 * 17.525 * 10^{-6}}{245 * 10^{-6} * 0.185^2} = 4.18 \Rightarrow W_{8,9,10,11} = 0.18 * 4.18 = 0.752\mu m$$

$$S_{4,5} = \frac{30.025 * 10^{-6}}{85 * 10^{-6}(1.8 - 1 + 0.5)^2} = 0.272 \ll 20.6$$

$$P_{diss} = 3.6 * (25 + 17.525 + 17.525) * 10^{-6} = 216.18\mu W$$

$$AV = \frac{V_{out}}{V_{in}} = (\frac{2 + K}{2 + 2K}) g_{m1} R_{II}$$

$$g_{m9} = \sqrt{2 * I_9 * K_N * S_9} = \frac{189.5\mu A}{V} \Rightarrow R_9 = r_{ds9} r_{ds11} = 385.3M\Omega$$

$$g_{m7} = \sqrt{2 * I_7 * K_P * S_7} = \frac{189.5\mu A}{V}$$

$$K = \frac{385.3 * 10^6 (\frac{1}{2 * 10^6} + \frac{1}{0.66 * 10^6})}{189.5 * 10^{-6} * 1.14 * 10^6} = 3.59$$

$$R_{II} = 385.3 * 10^6 \parallel [189.5 * 10^{-6} * 1.14 * 10^6 * (2 * 10^6 \parallel 0.66 * 10^6)] = 83.868 * 10^6 \Omega$$

$$AV = \frac{2 + 3.59}{2 + 2 * 3.59} * 1002.45 * 10^{-6} * 83.868 * 10^6 = 51195.07 * 10^6 = 94.18dB$$

$$Area = \sum = 0.18 * 10^{-6} * (29.53 * 2 + 0.3474 * 2 + 3.708 * 2 + 2.17 * 2 + 0.752 * 4) = 13.4\ \mu m^2$$

5. SIMULATION RESULTS

The folded cascode CMOS OTA was designed using the water cycle algorithm and gave great results compared to other sources that rely on the use of algorithms for optimization. In addition, a fixed amount of current was relied upon, estimated at 25µA, and also a load capacity of 0.5 square meters.

Figures 4-8 respectively present the simulation results for gain bandwidth, phase margin, slew rate (SR), settling time (St), and CMRR of the basic folded cascode CMOS OTA before and after using WCA. These illustrations offer a clear understanding of the folded cascode CMOS OTA's performance attributes and operational tendencies. Also, these figures showcase the performance enhancements achieved through the optimization process.

By comparing these results with the corresponding figures obtained before utilizing the water cycle algorithm, the impact of the optimization process on the folded cascode CMOS OTA's performance parameters becomes apparent. Table 4 delivers a detailed comparison of the main performance parameters for both scenarios: with and without the WCA implementation, as well as benchmarking against references employing various algorithms.

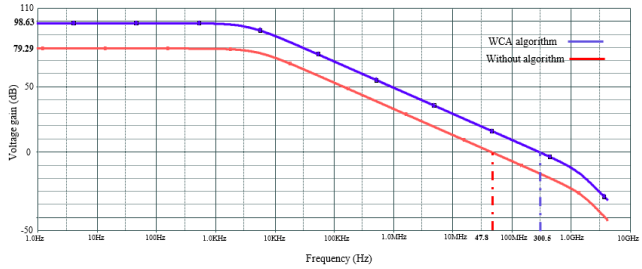


Figure 4. Simulation results for gain bandwidth (with and without WCA algorithm)

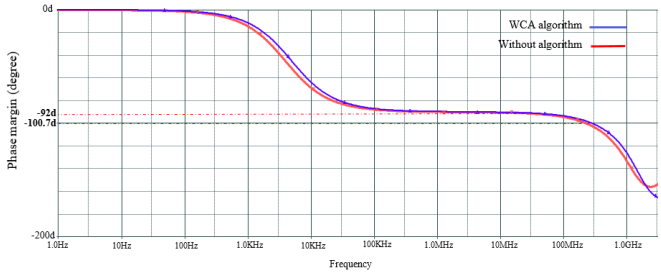


Figure 5. Simulation results for phase margin (with and without WCA algorithm)

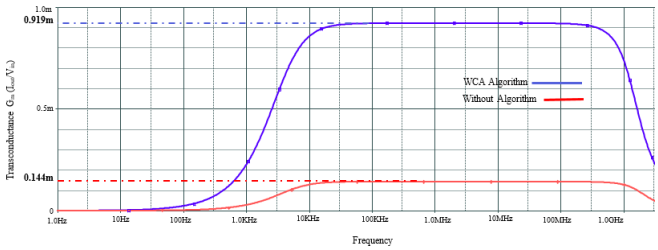


Figure 6. Simulation results for transconductance (with and without WCA algorithm)

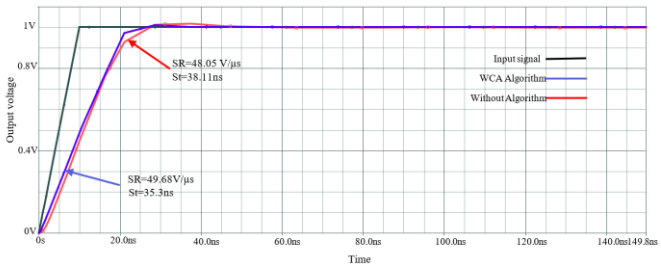
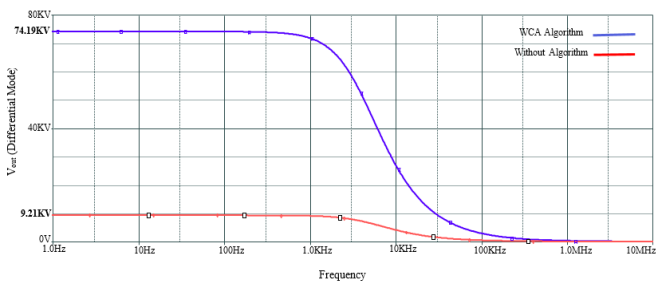
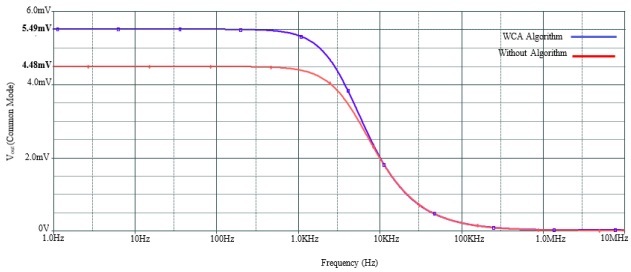


Figure 7. Simulation results for settling time (St) and slew rate measurement (with and without WCA algorithm)



(a) Diffrenetial mode



(b) Common mode

Figure 8. Simulation results of CMRR (a), (b) (with and without WCA algorithm)

Table 4. The performance parameters of the folded cascode CMOS OTA with and without WCA, as well as with other reference designs

Performance Parameters	Theoretical Results	WCA	HWPSO [8]	MCOA [23]	MRFC [24]
DC Gain (dB)	79.29	98.63	56.11	53.9	76.24
Gain Bandwidth (MHz)	47.8	300.5	0.55	398	74.7
Slew Rate(V/μS)	48.05	49.68	15.07	470	64.05
Settling time (ns)	38.11	35.3	-----	-------	----
CMRR (dB)	126.26	142.62	74.48	-----	-----
Power dissipation (μW)	255.6	216	6.106	1100	540
Phase margin (degree)	88	79.3	----	62.9	74.406
Area(μm^2)	3.46	14.3	21	128	2760
Transconductance(μA/V)	144	919	-----	-------	----
Technology	0.18	0.18	0.18	0.18	0.18
Temperature (°C)	27	27	27	27	27

The performance parameters of the proposed folded cascode CMOS OTA are affected by the load capacitance (C_L), which is demonstrated in Table 5. It is observed that when the value of CL (load capacitance) decreases:

- The voltage gain (Av) remains constant.
- The gain bandwidth (GB) increases.
- The phase margin decreases.
- The settling time decreases.

Figures 4 to 8 demonstrate that the voltage gain achieved with the WCA is 98.63 dB, representing a 24.4% increase compared to the previous value of 79.29 dB without utilizing the WCA. In the study [8], the voltage gain is reported as 56.11 dB, while in the study [22], it is stated as 53.9 dB. Additionally, the Gain Bandwidth (GB) is significantly improved with the WCA, reaching 300.5 MHz, which is improve the previous value of 47.8 MHz. In the study [8], the GB is reported as 0.55 MHz, while in reference [23], it is stated as 74.7. The power dissipation of the optimized design is reduced by 15.5%, decreasing from 255.6 μW to 216 μW after applying the WCA. In the study [8], the power dissipation is reported as 6.106 μW, while in the study [22], it is noted as 1100 μW and in the study [23], it is state as 540 μW. Moreover, other parameters such as CMRR and settling time (ts) also exhibit improvements through the use of the Water Cycle Algorithm, For temperature influence, this design is room temperatures and note the results are among the acceptable Ring compared to other research as in Table 4.

Table 5. The performance parameters of the proposed folded cascode CMOS OTA according to influence of load capacitance (C_L)

C_L(pF)	DC Gain(dB)	GB(MHZ)	Phase Margin	Settling Time(ns)
With (WCA)				
10	98.63	16.26	89.4	464.9
8	98.63	20	89.25	368.8
6	98.63	27.13	89	276.4
4	98.63	40.8	88.4	184.4
2	98.63	81.5	86.9	92.2
1	98.63	162.6	83.75	44.7
0.5	98.63	300.5	79.3	35.3
Without WCA				
10	79.29	2.6	90	692.81
8	79.29	3.2	89.9	547.51
6	79.29	4.3	89.85	413.5
4	79.29	6.4	89.78	273.81
2	79.29	13.08	89.54	134.1
1	79.29	26.1	89.08	67.13
0.5	79.29	47.8	88	38.11

Upon comparing all the results, it becomes evident that the WCA outperforms other types of algorithms in terms of achieving superior performance parameters for the folded cascode CMOS OTA. The significant enhancements observed in voltage gain, GB, area, phase margin, CMRR, and settling time validate the effectiveness of the water cycle Algorithm for optimizing the proposed design.

6. CONCLUSIONS

The continuous advancements in integrated circuit manufacturing have led to remarkable improvements in transistor performance. By conducting simulations using PSPICE (version 17.4) and based on 180nm TSMC technology, several key findings have been concluded:

1) The load capacitor (C_L), input transconductance, and aspect ratio of MOSFETs scaled down using newer technologies like 0.18μm, significantly influence the performance parameters value of the proposed design. The GB value, settling time, and phase margin are directly and inversely, respectively, affected by the load capacitor (C_L) variation.
2) The performance parameters of the folded cascode CMOS OTA have shown significant improvements due to the implementation of the water cycle algorithm.
3) The water cycle algorithm has proven to be highly efficient in enhancing the performance of the proposed folded cascode CMOS OTA. Its application can be extended to other designs with a similar operating principle.
4) The adoption of the water cycle algorithm for improving the folded cascode CMOS OTA offers a significant advantage in terms of time efficiency compared to traditional manual calculations, which may require a longer duration.

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