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# Enhanced Low-Power Digital Signal Processing via a Novel Reversible MCML-Based Carry Select Adder

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**ABSTRACT**

In Very Large Scale Integration (VLSI), the quest for designs that harmonize low power consumption with high-speed operation is paramount. Voltage scaling has emerged as a preeminent strategy for minimizing power consumption in digital systems. Although Complementary Metal Oxide Semiconductor (CMOS) technology, the predominant fabric of VLSI, exhibits enhanced performance upon scaling, it struggles to concurrently satisfy the exigencies for speed and power efficiency. Amidst this backdrop, MOS Current Mode Logic (MCML) has attracted increased scrutiny due to its rapid operational capabilities and consistent performance. Nevertheless, a perpetual challenge with MCML is its inherent static power dissipation. To mitigate this issue, this investigation introduces a novel approach employing reversible MOS current mode logic, which achieves substantial gains in power efficiency and processing speed for digital signal processing applications. The focus is on the development of a Carry Select Adder (CSLA) based on reversible logic and MCML, engineered to expedite operations while curtailing power consumption. Distinctively, the carry chain within this innovative CSLA is bifurcated into segments, each responsible for a subset of bits, ensuring the delay within the carry chain remains invariant irrespective of the bit count. This structural refinement significantly enhances the adder's speed by instituting a set carry delay. A meticulous evaluation of the proposed architecture's area, power, and delay attributes, facilitated by elementary gate-level modifications, is conducted. Comparative analyses reveal that the novel CSLA design markedly outstrips conventional CSLA models, including those predicated on TSG, Peres, and Feynman gates, registering a reduction in area by 39.01%, 44.09%, and 32.91%, a decrease in power consumption by 4.46%, 97.99%, and 33.12%, and a diminution in delay by 62.63%, 64.26%, and 47.32%, respectively. These findings underscore the potential of the proposed reversible MCML-based CSLA in setting a new benchmark for low-power, high-speed digital signal processing.

## 1. INTRODUCTION

Power consumption in VLSI design has been a significant issue in recent years. Digital systems are implemented using conventional gates [1]. Since the processing in digital circuits is irreversible, the input bits disappear as soon as a logic block emits output bits. Reversible logic circuits, however, are an exception [2]. Traditional logic gates like AND, OR, and XOR with several inputs and one output are not reversible. If there is a separate output vector for each individual input and one-on-one mapping between the inputs and outputs, then the gate is reversible. Reversible logic operations have the unique property of not dissipating energy through information loss. In traditional irreversible logic, bits of information are lost as they are processed, leading to energy dissipation in the form of heat. Reversible logic gates, on the other hand, conserve information, resulting in potentially lower power consumption [3]. Inputs and outputs must be equal for reversible gates. Heat is released during the operation of each bit of information by conventional combinational logic circuits. It is not appropriate for repeated procedures, though. Reversible logic is used to carry out repeated operations with the least amount of heat loss. Some reversible gate outputs are neither saved nor used in the following stage. Such undesirable outputs are equivalent to garbage output [4]. By using the constant inputs 0 or 1, intermediate values are saved during computation in reversible quantum circuits [5, 6].

Generally, almost in all the digital circuit designs and others, the CMOS design has been used for the hardware implementation. While CMOS technology's performance improves significantly with scaling, it cannot meet the speed and power requirements of these applications at the same time [7]. Important issues include power consumption, signal integrity, and technology scalability, which limit the performance of microprocessors [8, 9]. In recent years, MCML has replaced static CMOS circuits due to its quick functioning and minimum-noise differential logic style [10-12]. Due to its smaller swing, MCML cannot deliver a line-to-line output voltage. The speed of MCML circuits exceeds that of other logic families since they only employ NMOS

transistors [13-16]. Reducing the operating voltage allows MCML's power consumption to be reduced without sacrificing performance. Building logic gates, flip-flops, and other digital circuits like registers, clock circuits, and memories is made possible by MCML circuits [17]. The standard MCML-based full adder (FA) is built through conventional gates with six input signals [18]. It is not supported for repeated operation and has a vast area because of its irreversible nature. The full adder of MCML incorporates reversible logic to address this issue. The six input signals form the basis of the logic operation in the MCML full adder. Modifications to the logic gates are done to achieve reversibility. The inputs and outputs of the reversible gates should be mapped to one another since they have an equal number of each. The input vectors could potentially be recovered from the output vectors. Garbage outputs and constant inputs must be present in the very minimum amount to maintain reversibility. This reduces outputs of garbage and constant inputs [19]. Based on the reversible MCML-based full adder, the carry select adder is designed, which is found to be the fastest adder. In CSLA, two N-bit binary values are added arithmetically, and the results are output as an N-bit binary sum with a 1-bit carry. The CSLA operates in the same way as a Ripple Carry Adder (RCA); however, the RCA propagates carry signals through more full adders. This suggests that the operation moves very quickly [20-22]. The integration of a CSLA with reversible logic into MCML circuits involves adapting the design to the specific characteristics of MCML while leveraging the inherent power efficiency and heat minimization features of reversible logic. The primary impact of this research work is an evaluation of area, power, and delay performance, which is then compared with conventional CSLA.

The main contributions of this work are structured as follows:

- A basic overview of CMOS, MCML, and reversible logic is provided in Section 1.
- Section 2 shows the implementation of the modified CSLA.
- Section 3 discusses the findings.
- Section 4 draws the conclusion.

## 2. PROPOSED METHODOLOGY

In this proposed work, CSLA is designed using a reversible MCML full adder to attain minimum area and power. A MCML-based full adder operates logic gates according to six input signals. Changes have been made to logic gates to achieve reversibility. From the states of the output vector, there is a probability of recovering the input. In this research, a reversible logic-based full adder is implemented in the MCML circuit to reduce area and power dissipation. The performance of MCML full adder circuits can be improved using reversible logic, and the gate count, garbage output, and delay of the adders implemented using reversible logic can be evaluated.

### 2.1 Reversible MCML full adder

Figure 1 [19] depicts the MCML full adder based on reversible logic. This proposed design makes use of one PMOS and nineteen NMOS. The inputs are used to determine the outputs. To perform the reversibility, the fourth input is maintained as a constant in this circuit (D=0). P represents the carry, and Q represents the full adder sum. Outputs S and R are similar to inputs D and C. When compared with the available MCML full adder design, very few gate counts are required in the proposed MCML full adder.

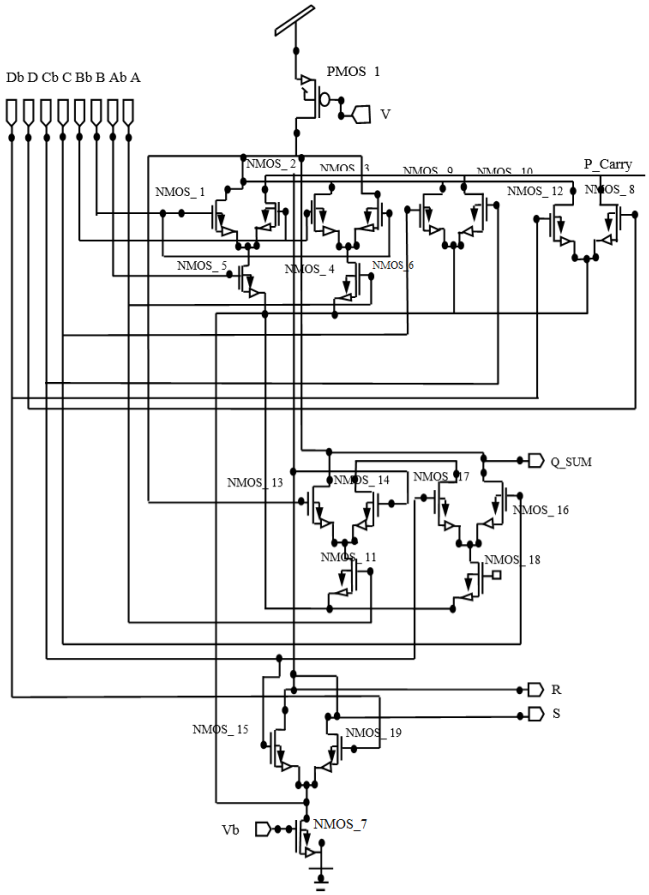


**Figure 1.** Reversible MCML full adder

### 2.2 CSLA with D-latch

The high-speed CSLA is usually constructed of the multiplexer (MUX) and RCA. Two RCAs are utilized in a CSLA to perform the operation twice when combining two N-bit values. One RCA has the carry input set to 0 and 1 by the other RCA. After finishing the addition operation and obtaining the two results, the multiplexer selects the appropriate sum and carry based on the control input. Carry propagation time is reduced by CSLA by separately generating many carries before choosing one to generate the number. However, because it uses many RCA pairs to calculate the partial outputs, the CSLA lacks efficiency with respect to area. The carry and sum outputs for the carry inputs 0 and 1 are determined by the multiplexers. Therefore, one RCA is substituted with a D latch so as to decrease the delay triggered by the RCA whose carry input is "1" and to optimize the area. In this proposed architecture, CSLA is built for word sizes of 8-bit, 16-bit, and 32-bit. As compared to normal CSLA designs, the enhanced CSLA using the D latch architecture increases the speed of addition and hence decreases the latency.

In this proposed architecture, a modification is done in CSLA using a D-latch. A D latch is a sequential circuit that stores the output for carry input 1 when the enable signal is activated and provides it as an input to the multiplexer to select either RCA output or D-latch output for carry input as the

selection line. D-latch receives an input from RCA when the enable pin is made high, and the multiplexer is provided with the D-latch output as an input. The latch holds the most recent state of the D input when the enable pin is switched low.

### 2.3 Implementation details

In this design, one of the RCA structures is swapped out with a parallel structure of D-latches with Cin=1 or Cin=0. N-D-latches are needed for the N-bit RCA structure, with the enable signal serving as the clock. Latches are used to store a bit of data. An enable pin is replaced by Cin in the RCA structure. The output is stored based on the carry input and enable pin. RCA determines the output for Cin=1 when the enable pin is made high and stores the result in the D-latch. RCA determines the output for Cin=0 when the enable pin is made low, and the multiplexer then receives both the full adder output and the D-latch output. The multiplexer produces the appropriate result according to the selected inputs. When compared to en=0, the time period for en=1 is brief. The RCA structure first computes for en=1 and subsequently for en=0. Five groups of RCA and D-Latch devices with various bit widths make up the proposed architecture. In order to save area, power, and time, this work simply uses one adder as opposed to the two separate adders used in standard CSLA. Each addition operation takes one clock cycle to complete.

Figure 2 depicts a 16-bit CSLA with a 2-bit ripple carry adder as the least significant bit. The most important portion is 14 bits wide and operates using the enable signal as a clock. Every time the clock gets high, the addition for carrying input one is carried out. The sum output is stored in the adder itself when the clock is deactivated, and the carry input is taken to be zero. For the purpose of choosing the final carry and sum, the multiplexer receives the carry-out Cout from the previous step as a control input. A D-latch is used to hold one bit of data when the clock input is set to high. In this instance, as the data on the D line changes, the output Q moves in step with the input D. The last state of the D input is kept and is in a hold position if the clock signal is turned to logic 0.

Figure 3 shows how the four D-latches are used in concert with the multiplexer to achieve the basic function of the CSLA. A full adder output is one of the multiplexer's inputs, while a D-latch output is one of its other inputs. When the two partial results are equivalent, the multiplexer is used to choose between the direct inputs and the D-latch output based on the control signal Cin.

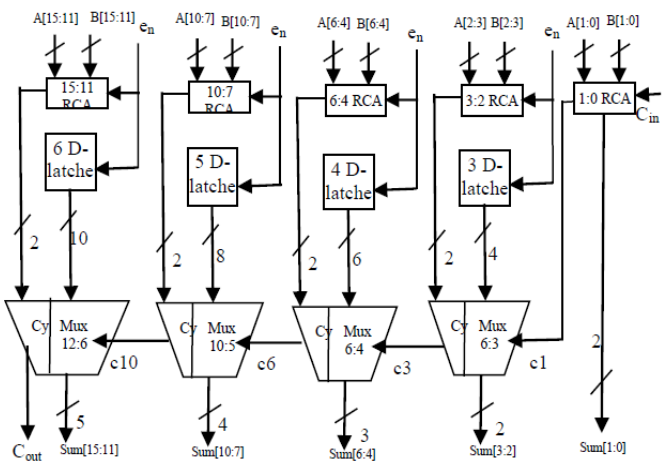


**Figure 2.** Block diagram of modified CSLA

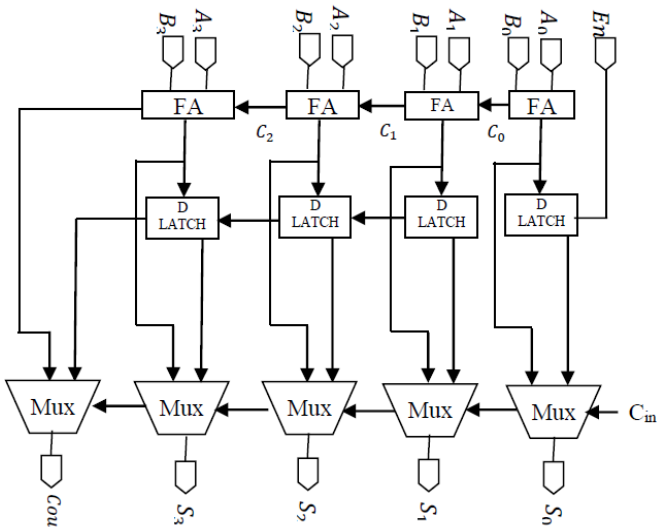


**Figure 3.** 4-Bit carry select adder

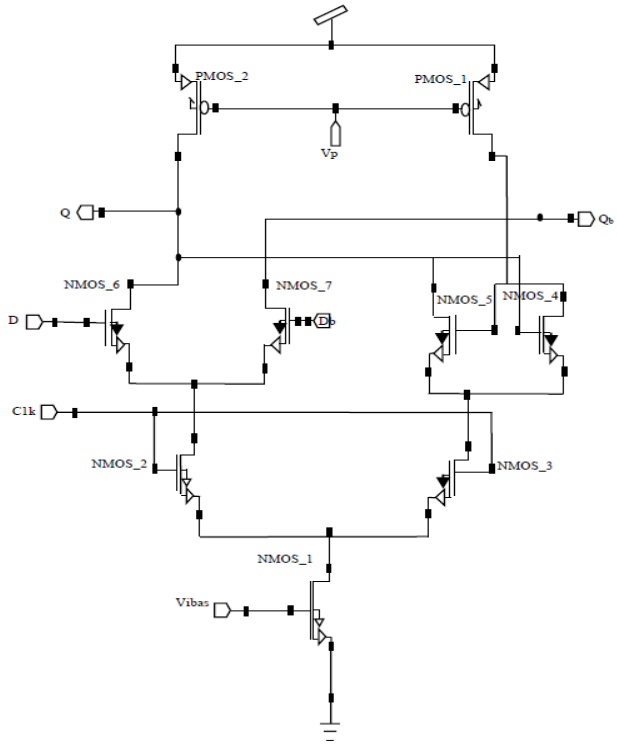


**Figure 4.** Schematic diagram of D-Latch for 4-Bit CSLA

Figure 4 shows the 1-bit D-latch design that is used in the next stage of CSLA. A bit of data is stored using a D-latch. It has a single input D, outputs Q and $Q_b$, and a clock signal Clk. In this design, seven NMOS and two PMOS transistors are used. Based on the D input signal and Clk signal, the output is produced. The design of the 2:1 multiplexer is illustrated in Figure 5, which is used for the selection of bits using the select lines. It has two inputs, A and B, with one select line. In this design, seven NMOS and two PMOS transistors are also used. The output is generated based on the inputs and select lines of theMUX.

Figure 6 shows the 16-bit CSLA design with A [15: 0] and B [15:0] with corresponding 16-bit outputs S [15:0] and $C_{out}$. In order to build this 16-bit CSLA, four 4-bit CSLA were cascaded in parallel, then two 16-bit CSLA were cascaded in parallel to form a 32-bit CSLA.

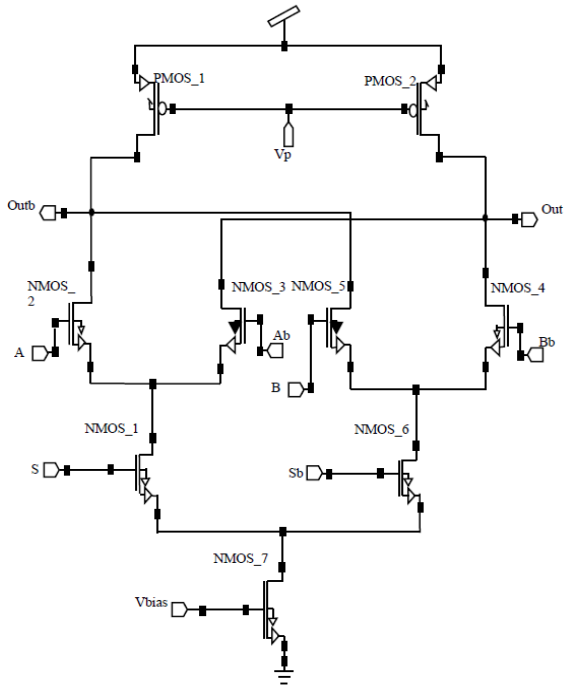


**Figure 5.** Schematic diagram of MUX for 4-Bit CSLA

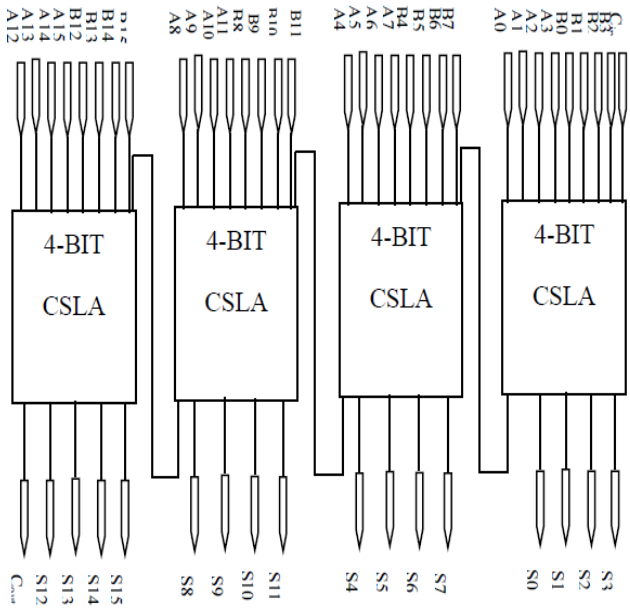


**Figure 6.** Architecture of 16-bit CSLA

## 3. RESULTS AND DISCUSSION

A simulation of a reversible MCML-based carry select adder circuit is performed using Tanner EDA tool at 180nm technology. The experimental findings of the proposed reversible 32-bit CSLA achieve reduced power, decreased area, and minimum latency because of its fast operation in comparison to the TSG gate, Peres gate, and Feynman gate-based FA. In the proposed research, a carry-select adder based on reversible logic is constructed for MCML circuits. With a minor, effective gate level modification, the reversible full adder design is used to achieve CSLA. This proposed circuit was chosen in order to reduce power and maximize speed with a smaller number of gates.

**Table 1.** Performance comparison of adders

| Parameter | Feynman Gate-Based FA | Peres Gate-Based FA | TSG Gate-Based FA | Proposed Reversible CSLA |
|---|---|---|---|---|
| Average Power (µW) | 4.48 | 213.76 | 6.4 | 4.288 |
| Static Power dissipation (mW) | 156.48 | 279.04 | 51.2 | 0.048 |
| Dynamic Power Dissipation (mW) | 2.08 | 2.252 | 1.877 | 1.764 |
| Static Current (mA) | 86.72 | 153.6 | 28.8 | 0.268 |
| Area (No of Transistors) | 2112 | 2304 | 1920 | 1288 |
| Delay (ns) | 4.85 | 5.07 | 3.44 | 1.812 |

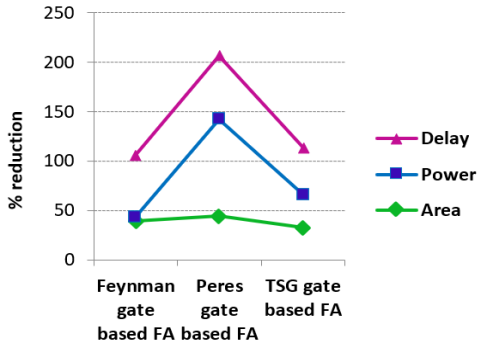


**Figure 7.** Percentage reduction in the area, power and delay

Table 1 displays the performance comparison of the reversible MCML carry select adder with the available designs of the full adder.

Table 1 shows that, in comparison to the TSG, Peres, and Feynman gate-based full adder, the proposed reversible 32-bit carry select adder has significantly reduced area by 39.01%, 44.09%, and 32.91%, low power by 4.46%, 97.99%, and 33.12%, and delay by 62.63%, 64.26%, and 47.32%. Figure 7 displays the decrease in percentage of area, power, and delay. This minimization is obtained due to the high-speed parallel adder using the D latch with the enable signal.

With an efficient gate level modification, CSLAs with different bit sizes are constructed in the proposed design. Figures 8-10 display the outputs, which are based on the values of parameters like area, power, and delay in Table 2 according to word size.

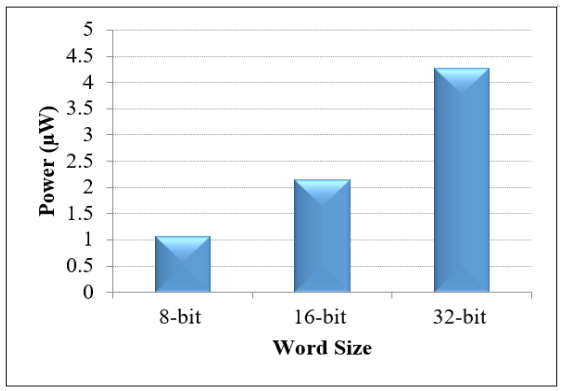


**Figure 8.** Power analysis


**Figure 9.** Delay analysis

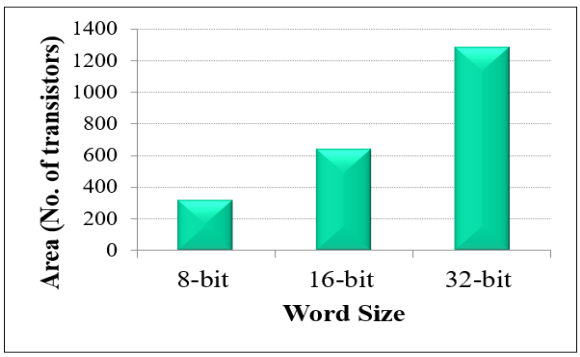


**Figure 10.** Area analysis

**Table 2.** CSLA analysis based on word size

| Word Size | Area (No. of Transistors) | Power (µW) | Delay (ns) |
|---|---|---|---|
| **8-bit** | 322 | 1.073 | 0.524 |
| **16-bit** | 644 | 2.146 | 1.357 |
| **32-bit** | 1288 | 4.288 | 1.812 |

## 4. CONCLUSION

A reversible logic-based carry select adder is built for MCML circuits in the proposed research. CSLA is implemented with a small, efficient modification using the reversible full adder design. In this research, since CMOS does not meet the speed and power requirements at the same time, MCML is preferred. But MCML suffers from static power dissipation, even though it has a high operational speed. Hence, reversible logic integrated with MCML is implemented to overcome static power dissipation and achieve minimum area, power, and delay. The proposed circuit is constructed using Tanner EDA tool using 180nm technology. Based on the outcomes of the experimentation, the presented CSLA circuit performs better than the available reversible logic circuits with respect to area, power, and delay. Therefore, the proposed design is quite effective, and this work certainly presents a new strategy for designing faster, lower-power processor hardware for digital signal processing. This research can be extended in the future by implementing the multiplier circuit using a reversible logic based MCML design.

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## NOMENCLATURE

| | |
|---|---|
| μW | Micro watts |
| mW | milli watts |
| mA | milli amps |
| ns | nano seconds |