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Advanced Phase Estimation and Design for Next-Generation Radar Systems: A Digital Approach

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ABSTRACT

Recent advancements in radar technology necessitate the development of effective digital designs to enhance productivity and reliability, thereby accelerating radar-based applications. This study focuses on the integration of highly accurate phase degree estimation, taking into account the diverse wireless standards prevalent in space applications. Field-Programmable Gate Arrays (FPGAs) in the semiconductor industry, known for their adaptability and scalability, play a pivotal role in advancing space design modeling. This paper presents an analysis of various design challenges encountered in implementing radar systems, introducing a novel approach for milli-degree phase approximation coupled with hardware optimization. The research introduces an enhanced floating-point arithmetic model with double precision, specifically designed to address minute phase errors in time-variant analog signals. The system under investigation examines fundamental signals, including amplitude, frequency, and phase measurements, in relation to the developed sample blocks. High-performance phase approximation design methods proposed herein address issues associated with conventional phase detection and synchronization. To overcome performance trade-offs in traditional phase-detection designs due to signal frequency variations, a CORDIC-based iterative phase computing system is developed. Additionally, a phase correction mechanism is designed for precise milli-degree phase estimation. This comprehensive approach not only refines phase estimation techniques but also contributes significantly to the field of radar applications, particularly in the context of digital system design and signal processing.

1. INTRODUCTION

In real-time applications, the system's overall efficiency is based on the level of arithmetic accuracy used in calculations and its minimal hardware design capability. Many phase detection applications often use fixed-point arithmetic because of its inexpensive cost. To characterize the type of data acquired in the context of space-based systems, however, functionality needs to be closely monitored. Comparing phase shift to other signal metrics, it is often the case that many obstacles arise in order to ensure the efficiency of space-borne systems. Word size matters a lot, particularly for situations where minimal computing requirements and error-free calculations are crucial. This problem requires the use of accurate floating-point arithmetic. Furthermore, integrating FPGA hardware presents challenges due to the synchronization of the system clock with the high-rate sampled data (GHz). An ADPLL-generated variable rate clock makes up the suggested phase detection system. Using several extensions over arithmetic computation and memory architectures, the high-performance phase estimation approach used in this research study finds essential applications in the following areas:

(1) In order to address synchronization problems, phase, amplitude, and frequency estimates based on the block are designed using a single compound array and a simplified ADPLL model without a controller.

(2) Provide an iterative phase computation system based on CORDIC and build a phase correction for millidegree phase estimation in order to avoid the performance trade-off that happens in standard phase detection systems during signal frequency changes.

2. FPU-BASED PHASE ESTIMATION

In order to meet the needs of high-efficiency and effective phase detection modules for high-rate space-borne systems, block-based phase estimation algorithms integrate fully digitalized phase synchronizers with floating-point arithmetic. The reliability is increased by the synchronized memory architecture and the precise and reliable phase detection network used here. This paper shows a better way to estimate phase that uses a sample block to make the performance trade-

offs that come up when estimating phase as the signal frequency changes less noticeable. The aforementioned procedure computes the phase of each succeeding sample point that corresponds to the particular sample block iteratively using FPU-based phase estimation. The proposed idea uses built-in block RAMs in FPGA devices to provide an array-based signal measure analysis methodology. A CORDIC-based post-computation system changes the initial phase, which is directly derived from sample blocks, in a big way for each iteration by using different estimates of the initial phase for each total sample point. The two objectives of this work are both specific and general.

2.1 Related work

According to the review of the literature on phase estimation by millidegree in analog signals of varying nature of time, they are used in various digital circuits like phase locked loop (PLL), finite state machine (FSM), RAM, FIFO, and CORDIC. The various algorithms available for phase estimation aim to optimize the consumption of power, calculate phase differences accurately, and reduce computational operations like adders, modulos, and multipliers [1]. The six equations from (1) to (6) are executed by the blocks, namely, adders, divisions, and multipliers, of the estimating phase [2]. However, these blocks and modules are of fixed point type and are not able to identify the millidegree, i.e., narrow differences in phase. Therefore, by using double precision FPA operations, the speed of estimating by millidegrees will be increased, and it is also due to the fact that adding and multiplying operations are performed without using any propagation of carry [3]. Phase measurement is more commonly used as the building or fundamental block. Normally, PLL is implemented by the use of a binary system of numbers that causes a major delay in propagation [4]. The large part of the delay was due to the high-order phase estimations that contain n numbers of additions and multiplications. Due to this delay, the operation speed of the ADC and the PLL decreased.

If many operators are required for blocks that are used for constant multiplications along with fixed point operations, then a new hypothetical lower limit is executed [5]. Each operation is executed by using pipelining, and the multipliers are constructed with the use of floating point formats. By using this simple structure, pipelined n-input addition and subtraction operations were executed using registers that are used in pipelining [6]. The main drawback of these fixed-point operations of the arithmetic type is that power consumption is very high, and thereby the cost is also very high. However, the one advantage of this fixed point method is that it reduces the PP to increase the speed of the multiplication [7]. The research work of K. H. Chen introduces the linear array multiplier structure by combining the different methods, which is power efficient. But the limitation of this work is that it has more delay and occupies more area. An approach that uses high operation speed and consumes low power was proposed by Chu and Chen. This utilizes the multiplier's compression tree and spurious power suppression (SPST) for Booth decoders [8]. But it occupies more area, which is the major limitation of this method. Carry Look Ahead adder and ripple carry adder are used for adding the PPs and verifying the multiplier of 32-bit numbers, as proposed by the researcher Hasan K. The authors Dastjerdi and others presented the BZ FAD method of shifting and adding multiplication for implementing the multipliers, which reduced the performance of switching and minimized the utilization of power. The benefit of this approach is that it reduces the cost of computation and increases the speed of operation. The authors Shabbir and others proposed a multiplier based on the Dadda algorithm, which operates at high speed with less power dissipation. Full adders are suggested to make use of the multipliers. Also, with the use of flip-flops, errors in the output of multipliers can be reduced.

From these deliberations, it can be concluded that for detecting the phase of the millidegree in continuous time, the necessary components are Floating Point Arithmetic (FPA) Operations, ADPLL, RAM, and FSM. A few applications of estimating the phase and identifying narrow differences in the phase are multiplication, subtraction, and addition. The number system of residues can identify and correct errors with the help of fault tolerance [9].

The necessity is majorly supported and present in the newest family of FPGAs, Field Programmable Arrays. This family provides an effective platform for implementing the algorithms that are used for detecting the phase. The requirement for this is only a few resources of hardware type and fewer cost blocks of constant multiplication [10].

3. OBJECTIVES

For space-borne systems with high data rates, the need for the highest reliable and maximum performance units for detecting the phase, a completely digital phase synchronizing unit, and the FPA are implemented in the block-based estimating system for phase. The reliability is significantly enhanced by the synchronizing architecture of memory and the network that accurately detects the phase. This research paper presents an optimized sample model that is based on block-based estimation of phases. This also consists of a FPU-based estimation of phase and an iterative method of computing the phase for all samples that are in successive order. These sample points are connected with the initial sample block to diminish the trade-off performance characteristics of estimating the phase with a dynamic signal frequency. The presented method uses the in-built RAM blocks within the devices of the FPGA for the evaluation of array-based signals. In this approach, a model that is based on cordic post-computing is presented for every iteration and implemented using independent estimations of phase over all the sampling points to improve the starting phase that was evaluated directly from the sampling blocks. This thesis has divided the overall research objectives into two broad categories: general purposes and specific objectives. Here, the available object refers to the overall research aim to prove all primary goals.

(1) To develop the best arithmetic and path delay-optimized parallel processing models for high-performance milli-degree phase estimation with improved reliability.

(2) To develop a novel sample block-based amplitude and frequency estimation using a dedicated signal processing unit.

(3) To design an iterative phase evaluation for all sample points to reduce the phase error.

4. BLOCK BASED PHASE DETECTION ALGORITHM

In the study of Huang et al. [11], the proposed phase estimation in the real-time application and estimated power are 3% using linear programming (LP). The frequency-modulated

continuous wave is presented for 4 GHz frequency and a bandwidth of 160 GHz for estimation phase and resolution discussion in the study of Ahmad et al. [12]. When a target's Doppler frequency exceeds half of the chirp repetition frequency, there is Doppler ambiguity in the range-Doppler domain of LFM continuous wave radars. Doppler ambiguity is common in radar systems, so it's important to have a maximum unambiguous Doppler shift extension for a wide range of civil and military radar applications [13]. Several applications that require reliable environmental sensing depend on phased array radar systems. There must be many receiving antenna elements to detect sensitive targets and accurately estimate the direction of arrival (DOA). Digital signal processing is necessarily burdened with a heavy computing load due to the high dimension of the element-level data [14]. When the pulse repetition interval (PRI) is changed on a regular basis, staggered synthetic aperture radar (SAR) can continuously image an extremely wide area while effectively staggered range blind areas. As a result of the changing PRI, azimuth samples are not spread out evenly in a typical staggered SAR. This means that complex resampling processing is needed, including multichannel reconstruction processing and the best linear unbiased (BLU) interpolation [14]. A possible method for the low-cost collection of multiple Doppler weather measurements is multi-static radar. In spite of this, these systems often have much higher two-way side lobe levels than monostatic radars because the receivers use low-directivity antennas. Doppler velocity estimate biases brought on by side lobe contamination have proven to be a major barrier to this technology's wider use [15]. The presented method, based on the frequency-modulated continuous-wave principle, uses both the round-trip phase difference and the frequency difference of the radio wave signal impinging at two widely separated receiving antennas to achieve extremely precise and absolute measurements of the direction of arrival.

In synthetic aperture radar processing, phase unwrapping is a crucial step whose correctness directly affects the dependability of later applications [16]. Many phase unwrapping techniques have been developed, the majority of which require that the phase maintain spatial continuity. However, these assumptions are invalidated by decorrelation noise and aliasing fringes, which cause these techniques to perform poorly [17]. A significant source of interference known as the atmospheric phase screen is introduced by tropospheric propagation delay in multitemporal interferometric synthetic aperture radar (InSAR) applications (APS) [18].

4.1 Amplitude estimation

Here, the input signal is represented as:

$$x(t) = Acos(2\pi f_0 t) + \varphi_0 \tag{1}$$

The amplitude, frequency, and phase of the input signal are denoted by A, f_0, and φ_0, respectively:

$$\int_0^T x^2(t)dt = \frac{A^2 T}{2} \tag{2}$$

In this case, the input signal's single-clock cycle time is represented by T and is equal to 1/f0. The signal energy of one full cycle is calculated as shown below by generating the signal energy equivalent value of the input signal across the single signal period T and across corresponding sample index values of the negative to positive transition np [Nnp].

$$\frac{A^2 T}{2} \times \frac{np[N_{np}]T_s}{T} = CS\left[np\left[N_{np}\right]\right]T_s \tag{3}$$

A simplified form of the aforementioned equation is employed to compute the signal amplitude:

$$A = \sqrt{\frac{2}{np[N_{np}]}}\sqrt{CS[np[N_{np}]]} \tag{4}$$

4.2 Frequency estimation

In this case, the input signal frequency is approximated using Eq. (5) and also by employing a maximum count of zero to positive transitions over a specified sample block as well as related sample points over this interval. To perform these computations, the sampling frequency, which is fixed during the signal processing, is estimated as follows:

$$F = \frac{N_{np}-1}{np[N_{np}]-np[1]}F_s \tag{5}$$

The sampling frequency of the ADC is indicated by F_s. The overall samples, in this case, is constant, however, the sample points indexes, as well as their corresponding signal transitions, vary in proportion to the signal frequency, which further causes some inaccuracies while evaluating the phase from the estimated signal frequency. To achieve acceptable system accuracy throughout the phase estimation procedure, it is necessary to derive the precise input signal frequency.

4.3 Single phase estimation

Lastly, via read-write FSM, 2400 samples are recorded in RAM

$$\emptyset_c^k = \emptyset_c^{k-1} - \frac{\sum_{m=1}^{M}(sin\theta_m(v[m]-Acos\theta_m))}{A\sum_{m=1}^{M}(sin\theta_m)^2} \tag{6}$$

where, $\omega = 2\pi f$; $\nabla t = \frac{1}{Fs}$ and

$$\theta m = \omega \times \nabla t \times (m-1) + \varphi_c^{k-1}$$

The phase's starting value is corrected and updated by computing the signal phase values of sample points from the input sample block. The advanced version of the phase estimate outcomes ultimately obtained is directly associated with the input signal's solid phase [19].

The hardware algorithm operating on an FPGA initially receives a total of M samples from array.

Furthermore, the substitution mapping function avoids the interaction between the generated vital sequences and the biometric features. This block can be modified to any sequence length throughout the implementation phase for sensor nodes [20].

Block-based phase detection algorithm: *Input*: s(t); *Output*: A, F, and P.

(1) From the input high-rate signal sequence, create a signal array of M samples.

(2) The module of BS accepts the input array along with M sample values M 0, 1,...2400 and thereby calculates four parameters, which are as follows: the number of negative to

positive transitions (Nnp), the first transition sample index value (np1), and the last transition sample index point (np[Nnp]), before computing the cumulative sum of the squares (CS) for the input array.

(3) Depending on the above four fundamental signal measurements, A as well as F, as represented in Eqs. (4) and (5), are computed.

(4) To calculate millidegrees of phase, the values from Eq. (5) are converted into IEEE 754 double precision format, and Equation is used to calculate the introductory phase (6).

(5) In Eq. (6), an iterative technique is employed to rectify phase errors, and sin and cos values are calculated by employing the CORDIC core to generate finite phase estimates.

5. EXPERIMENTAL RESULTS AND DISCUSSIONS

A synthetic sinusoidal waveform's input GHz rate sample data is supplied to the FPGA in 8-bit format, where it is processed at 375 MHz frequency and used to build the FPGA circuitry. The watch undergoes four down-conversions in order to synchronize with the system clock. Input sample values are stored forward by a 256 × 1024 FIFO. Finally, 2400 samples are recorded in RAM using read-write FSM [21].

2400 sample RAM blocks with an 8-bit size are completed for data calculation, as shown in Figure 1. The data flow from the FIFO to the block scan module, which also changes the data's format from unsigned to twos complement and stores it in RAM, is managed by each finite state machine in this instance. There are also basic signal processing metrics for parametric evaluations that the block scan unit makes. These include the number of transitions that are harmful to positive (Nnp), the sample points of the beginning and end changes (np1 and np[Nnp]), and the cumulative sum squares of array values (CS[np[Nnp]]. It also evaluates the sample block. The result shows that both the write control FSM method and the reader can work on the sampled data at a high frequency, which means that there is a lot less work to do on the computer and a lot more data to store [22].

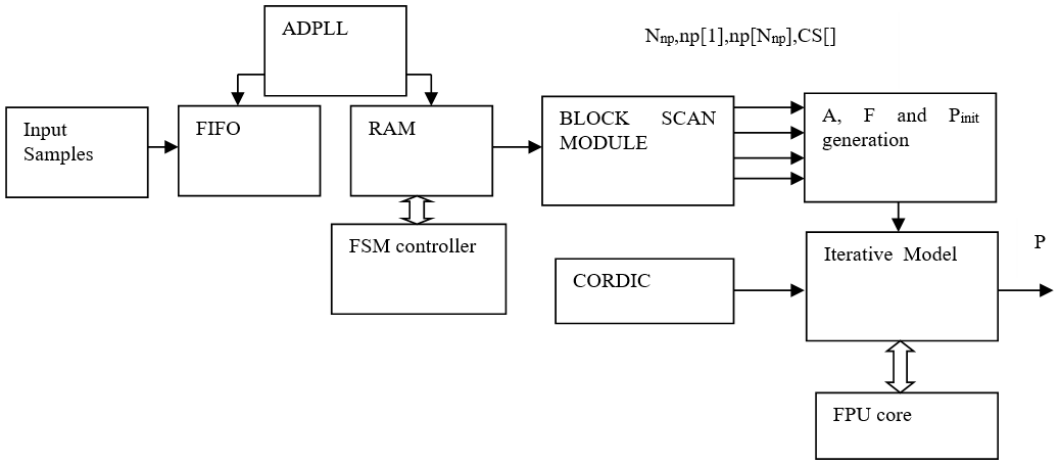

Figure 1. Block-based phase detection system

6. SIMULATION RESULTS USING MODELSIM

The basic module is simulated using a synchronous clock at different stages of the matching process to check the parametric approximation of the synchronized block-based phase detection method and see what happens when the level of accuracy is raised for millidegree phase detection. Typically, in digital systems, the input sinusoidal waveform elements are sampled at a frequency of GHz to produce signal samples. These samples are subsequently converted to binary codes of two's complement and stored in on-chip memory while hardware is being synthesized.

By simulating the effect of increased precision in the phase detection of millidegrees using a synchronized clock in various phases of matching, the estimation made using parameters for synchronizing the phase detection process based on blocks is validated. In the case of a digital implementation, the sinusoidal inputs are formed by sampling signals at a few gigahertz, as seen in Figure 2. Figure 3 illustrates how this data is transformed into the 2's complement form. Using circuitry for synthesizing on-chip memory, it is stored. is used to store it.

Table 1 provides a comparative analysis of the performance of our proposed block-based phase estimator driven by FPA (Floating-Point Arithmetic) with that of existing literature in terms of area, LUT, number of DSP blocks, delay, and power.

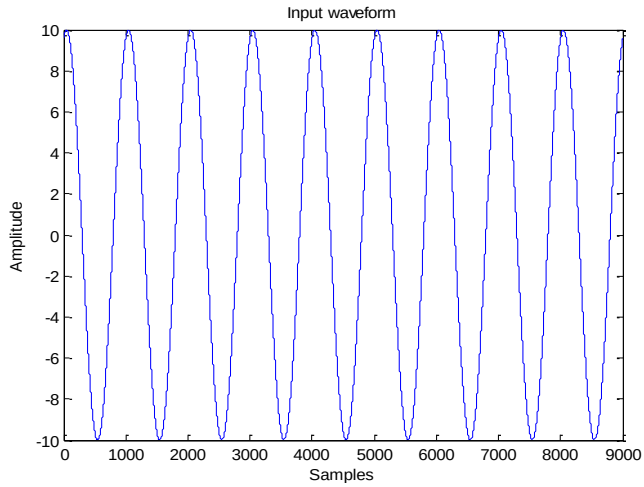

Figure 2. Input analog waveform

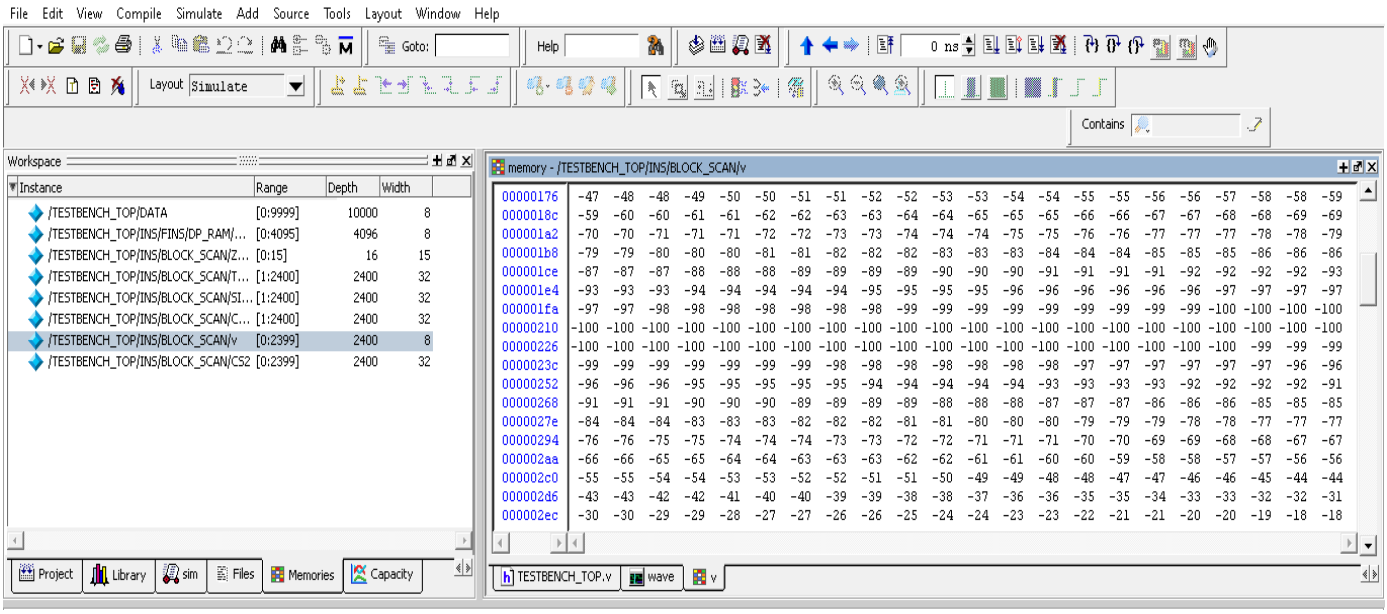

Figure 3. Twos complement representation

Table 1. Comparison of the proposed FPA-driven block-based phase estimator's performance with existing literature

Algorithms	Slices (Area)	LUT	DSP Blocks	Delay (ns)	Area*delay	Power (mw)
[23]	23901	21092	20	16.1	3,84,806.1	11.4
[24]	27623	10712	--	15.3	4,22,631.9	9.3
[25]	37612	5011	51	18.2	6,84,538.4	12.12
This work	20941	22371	2	11.29	2,36,423.89	7.2

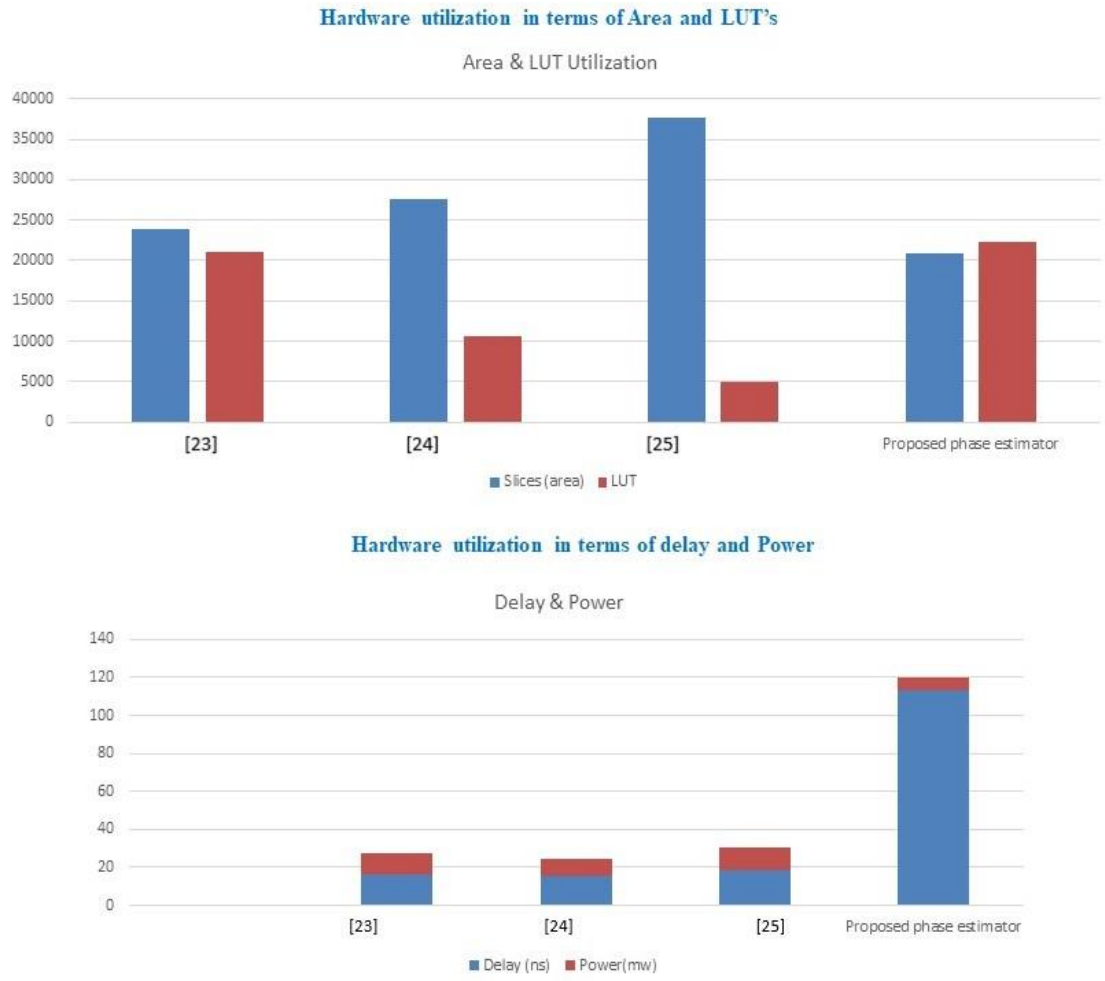

Figure 4. Hardware utilization

Comparing the proposed FPA-driven block-based phase estimator with existing literature, as shown in Figure 4, it is evident that the new approach exhibits notable advantages in terms of area utilization, LUT, and DSP blocks. However, it is essential to consider the trade-off with delay, as the proposed method shows a higher delay compared to some existing algorithms. The product of area and delay (area*delay) is also significantly influenced by this trade-off. Power consumption, on the other hand, is relatively lower in the proposed work, indicating potential efficiency in power management.

6.1 Energy efficiency

To overcome the drawbacks that are associated with energy, phase detection algorithms that are based on the unified block, as well as suitable clock generation techniques, are included. However, FPU-core-based phase computation requires advanced hardware design compared to the typical phase detection paradigm.

6.2 Internal parallelism

The consecutive path delay data propagation is improved for a specific configuration using the FIFO architecture and a ring counter-facilitated DCO module.

6.3 Parallelization

With the help of the divide as well as conquer technique, the application of hardware can be enhanced. Even though it has been frequently demonstrated that decomposed programmable delay approaches based on buffers generally offer high productivity and versatility to maximize power across models that are evaluated simultaneously.

7. RESULTS AND DISCUSSION

The model has been built with a Zybo-7000 FPGA board device from the Vivado Design Suite family, using a Xilinx FPGA synthesizer and a Verilog HDL script. Usually, functional verification is carried out with a comprehensive test bench that is enabled by a bit stream. It is clearly shown that clock rate constraints have both intrinsic and changeable rates using the simulation findings. The results of the experiments provide more evidence for the potential benefits of synchronization and how it helps variable-rate parallel processing.

8. CONCLUSION

This study work article introduces a phase detection system that performs at a high level, as well as a frequency synthesizer design that is well optimized for usage in space-based systems. An examination is conducted on the performance indicators in respect to the diverse standard's needs. Furthermore, the evaluation of phase detection using the FPA for estimating phase with millidegree precision is included in the project. The provided optimized sample block-based estimator model has demonstrated superior performance compared to other existing models for phase detection, making it the ideal choice for FPGA implementation. In conclusion, it is clear that the design of memory models, specifically RAM and FIFO, significantly enhances performance efficiency. Furthermore, a recommended approach for synchronization is proposed after careful research. The testing findings demonstrate that the phase detection strategy being utilized effectively reduces phase error by employing an iterative method to accommodate frequency variations.

9. OPEN ISSUES AND FUTURE WORKS

A few major challenges identified after a thorough evaluation of the presented model's hardware for estimating the phase for space-based systems are as follows: effective units of floating-point computations are required to enhance the system's performance. The research work is limited to the analysis of complexity in hardware, irrespective of the hardware constraints and requirements of various means of space environments. Different signal measurements with various snr ranges can be examined for approach performance evaluation. Even though it has several practical measures, a trade-off may exist in a natural world environment when the signal snr exceeds the threshold margin.

REFERENCES

[1] Chen, K.H., Chu, Y.S. (2007). A low-power multiplier with the spurious power suppression technique. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 15(7): 846-850. https://doi.org/10.1109/TVLSI.2007.899242

[2] Krad, H., Al-Taie, A.Y. (2008). Performance analysis of a 32-bit multiplier with a carry-look-ahead adder and a 32-bit multiplier with a ripple adder using VHDL. Journal of Computer Science, 4(4): 305-308.

[3] Usmani, A.F., Taslima, E., Khan, S.A. (2019). Design of FPGA based phase reconfiguration technique. In M. Sato 2019 3rd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), Kolkata, India, pp. 1-5. https://doi.org/10.1109/IEMENTech48150.2019.8981037

[4] Russo, D., Ricci, S. (2019). FPGA implementation of a synchronization circuit for arbitrary trigger sequences. IEEE Transactions on Instrumentation and Measurement, 69(7): 5251-5259. https://doi.org/10.1109/TIM.2019.2952478

[5] Uddin, M.N., Rezaei, N. (2020). An FPGA-based Cost-effective digital differential relay for wind farm protection. In 2020 IEEE Industry Applications Society Annual Meeting, Detroit, MI, USA, pp. 1-8. https://doi.org/10.1109/IAS44978.2020.9334863

[6] Fan, H., Yang, J., Zhang, J., Zhang, K., Xing, D., Feng, Q. (2020). FPGA based digital magnetic field detection system. In IGARSS 2020-2020 IEEE International Geoscience and Remote Sensing Symposium, Waikoloa, HI, USA, pp. 3215-3218. https://doi.org/10.1109/IGARSS39084.2020.9323272

[7] Drakontaidis, S., Stanchi, M., Glazer, G., Hussey, J., Leger, A.S., Matthews, S.J. (2018). Towards energy-proportional anomaly detection in the smart grid. In 2018 IEEE High Performance Extreme Computing Conference (HPEC), Waltham, MA, USA, pp. 1-7. https://doi.org/10.1109/HPEC.2018.8547695

[8] Díaz, E., Mateos, R., Bueno, E. (2019). Virtual platform of FPGA based SoC for power electronics applications. In 2019 IEEE 28th International Symposium on Industrial Electronics (ISIE), Vancouver, BC, Canada, pp. 1371-1376. https://doi.org/10.1109/ISIE.2019.8781247

[9] Psarakis, M., Dounis, A., Almabrok, A., Stavrinidis, S., Gkekas, G. (2020). An FPGA-based accelerated optimization algorithm for real-time applications. Journal of Signal Processing Systems, 92: 1155-1176. https://doi.org/10.1007/s11265-020-01522-5

[10] Atoui, E.B., Mesbah, T., Atoui, H., Kelaiaia, S. (2020). Implementation and co-simulation based on FPGA of circulating currents control in MMC using reduced order generalized integrator. Electrical Engineering, 102(3): 1531-1547. https://doi.org/10.1007/s00202-020-00973-0

[11] Huang, H., Zhao, K., Chen, H., Chen, G., Hu, D., Zhang, Y., Yang, Z. (2020). Improving time-efficiency of variational specific differential phase estimation. IEEE Transactions on Geoscience and Remote Sensing, 59(7): 5642-5664. https://doi.org/10.1109/TGRS.2020.3020914

[12] Ahmad, W.A., Kucharski, M., Ergintav, A., Abouzaid, S., Wessel, J., Ng, H.J., Kissinger, D. (2020). Multimode W-band and D-band MIMO scalable radar platform. IEEE Transactions on Microwave Theory and Techniques, 69(1): 1036-1047. https://doi.org/10.1109/TMTT.2020.3038532.

[13] Dikshtein, M., Longman, O., Villeval, S., Bilik, I. (2021). Automotive radar maximum unambiguous velocity extension via high-order phase components. IEEE Transactions on Aerospace and Electronic Systems, 58(1): 743-751. https://doi.org/10.1109/TAES.2021.3103262

[14] Neuberger, N., Vehmas, R., Ender, J.H. (2021). Dimension-reduced Rx beamforming optimized for simultaneous detection and estimation. IEEE Transactions on Aerospace and Electronic Systems, 57(4): 2501-2513. https://doi.org/10.1109/TAES.2021.3060758

[15] Xu, W., Hu, J., Huang, P., Tan, W., Gao, Z., Dong, Y. (2021). Continuous PRI variation and phase center adjustment for azimuth uniform sampling in staggered SAR. IEEE Transactions on Geoscience and Remote Sensing, 60: 1-13. https://doi.org/10.1109/TGRS.2021.3079230

[16] Son, H., Lee, S., Min, K. (2010). FPGA implementation of UWB radar signal processing for automotive application. In the 3rd European Wireless Technology Conference, Paris, France, pp. 49-52. https://doi.org/10.1109/EWTC.2010.5483549

[17] Byrd, A.D., Palmer, R.D., Fulton, C.J. (2021). Doppler velocity bias mitigation through sidelobe whitening for multistatic weather radar. IEEE Transactions on Geoscience and Remote Sensing, 59(2): 1130-1142. https://doi.org/10.1109/TGRS.2020.2997882.

[18] Scherhäufl, M., Hammer, F., Kastl, C., Stelzer, A., Pichler-Scheder, M. (2020). Viterbi decoder to resolve angular ambiguity in digital beamforming with widely spaced radar front ends. IEEE Transactions on Instrumentation and Measurement, 70: 1-9. https://doi.org/10.1109/TIM.2020.3026789

[19] Wu, Z., Wang, T., Wang, Y., Wang, R., Ge, D. (2021). Deep-learning-based phase discontinuity prediction for 2-D phase unwrapping of SAR interferograms. IEEE Transactions on Geoscience and Remote Sensing, 60: 1-16. https://doi.org/10.1109/TGRS.2021.3121906

[20] Izumi, Y., Nico, G., Sato, M. (2021). Time-series clustering methodology for estimating atmospheric phase screen in ground-based InSAR data. IEEE Transactions on Geoscience and Remote Sensing, 60: 1-9. https://doi.org/10.1109/TGRS.2021.3072037

[21] Shen, P., Wang, C., Hu, J., Fu, H., Zhu, J. (2021). Interferometric phase optimization based on PolInSAR total power coherency matrix construction and joint polarization-space nonlocal estimation. IEEE Transactions on Geoscience and Remote Sensing, 60: 1-14. https://doi.org/10.1109/TGRS.2021.3053278

[22] Microchip, "Low Power FPGAs & PLDs," https://www.microchip.com/en-us/products/fpgas-and-plds/low-power.

[23] Eddla, A., Yasoda, V., Pappu, J. (2022). Low area and power-efficient FPGA implementation of improved AM-CSA-IIR filter design for the DSP application. International Journal of Electrical and Electronic Engineering and Telecommunications, 11(4): 294-303. https://doi.org/10.5815/ijitcs.2022.04.02

[24] Ullah, S., Rehman, S., Shafique, M., Kumar, A. (2021). High-performance accurate and approximate multipliers for FPGA-based hardware accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 41(2): 211-224. https://doi.org/10.1109/TCAD.2021.3056337

[25] Zereen, S., Lal, S., Khalid, M.A., Chowdhury, S. (2018). An FPGA-based controller for a 77 GHz MEMS tri-mode automotive radar. Microprocessors and Microsystems, 58: 34-40. https://doi.org/10.1016/j.micpro.2018.02.005