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A Power-Efficient Error Detection and Correction Circuit Design Using Hamming Codes for Portable Electronic Devices

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ABSTRACT

Error-free communication is crucial for modern electronic devices. Error detection and correction mechanisms are essential to ensure accurate information transmission. With the increasing usage of mobile devices and integrated circuits operating at higher speeds, energy efficiency has become an important design consideration. This study presents carbon nanotube field-effect transistor (CNTFET)-based Hamming Error Detection and Correction circuits and compares them with complementary metal-oxide semiconductor (CMOS)-based counterparts in terms of power efficiency and delay. CNTFETs are more power-efficient and faster than CMOS transistors, making them ideal building blocks for logic circuits. The proposed circuits were simulated using HSPICE. Compared with CMOS circuits, the CNTFET designs consumed less power, had lower delays, and smaller power-delay products. The proposed error detection and correction circuits are suitable for power-efficient and portable systems.

1. INTRODUCTION

Data transmission involves sending information from one location to another. While copper wires were traditionally used, wireless networks have largely replaced them [1]. Higher data transfer rates increase the likelihood of errors arising from noise, crosstalk, electromagnetic interference, and other factors. Detecting and correcting these errors is critical to ensure the intended message is received accurately [2]. Error detection adds redundant bits to the transmitted data. A simple and widely used error detection and correction method is the Hamming Code, which employs exclusive-OR logic [3]. Although Hamming codes can detect certain errors, they can only correct one [4, 5].

Modern processors require faster speeds, smaller sizes, and lower power consumption [6]. Reducing transistor size improves performance but also increases power density. Challenges in scaling down complementary metal-oxide semiconductor (CMOS) transistors have been increasing [7-9]. Carbon nanotube field-effect transistors (CNTFETs) are nanoscale devices with high performance and low power consumption [10]. CNTFETs use carbon nanotubes (CNTs) instead of bulk silicon in the channel. Compared with CMOS, CNTs provide higher carrier mobility, enabling faster operation. While early CNTFETs were p-type due to contact doping, n-type CNTFETs were subsequently developed through alkali gas doping and thermal annealing in vacuum. Both p-type and n-type CNTFETs can now be fabricated. CNTFETs and MOSFETs have similar structures, but CNTFETs are suitable for nanoscale devices [11].

Figure 1 shows a CNTFET schematic with single-walled CNTs sandwiched between two electrodes. Highly doped CNTs are placed between the gate and source/drain electrodes. Undoped CNTs under the gate electrode form the channel [6, 11].

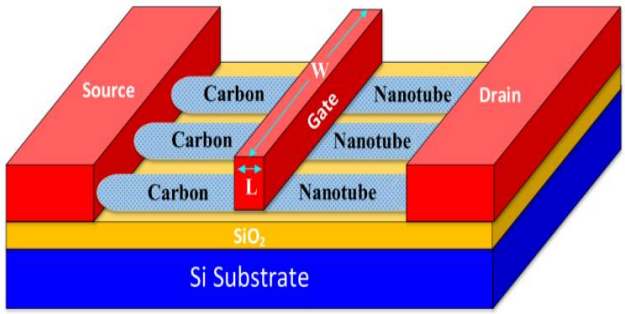

Figure 1. Schematic of CNTFET [2]

CNTFET gate width can be obtained from equation [2]:

$$W_{gate} \approx \text{Max}\left(W_{min}, MXP\right) \quad (1)$$

CNT diameter can be calculated from Eq. (2) [6]:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (2)$$

where,

a_0=142 pm=the distance in between adjacent carbon atoms;

m and *n* are chirality vectors which show the roll orientation of carbon Nano-tubes.

Now, the Eq. (2) can be written as,

$$D_{CNT} = 0.0783\sqrt{n^2 + m^2 + nm} \quad (3)$$

Carbon nanotubes (CNTs) are a novel material, and CNT field-effect transistors (CNTFETs) are the associated devices that can potentially replace CMOS FETs and enable scalability below 22 nm [12]. In fact, CNTFETs are a promising alternative to silicon transistors for high performance and low power consumption [13-15].

Plastic waste is a major environmental problem, generating over 500,000 tons per year. It poses dangers to human and animal health, especially for seabirds that cannot digest it, often leading to death. Polypropylene (PP) plastics account for 19% of this waste and have a high carbon content (86.7%) compared with other plastics like high-density polyethylene, low-density polyethylene, and polyethylene terephthalate. This carbon-rich PP waste is useful for generating CNTs [16].

CNTFETs can extend the validity of Moore's law [17]. Various digital and analog circuits and systems based on CNTFETs have been proposed, such as adders [18-21], flip-flops [22-25], and multiplexers [26-28]. CNTFETs resemble MOSFETs but replace the bulk silicon channel with semiconducting CNTs, as shown in Figure 2.

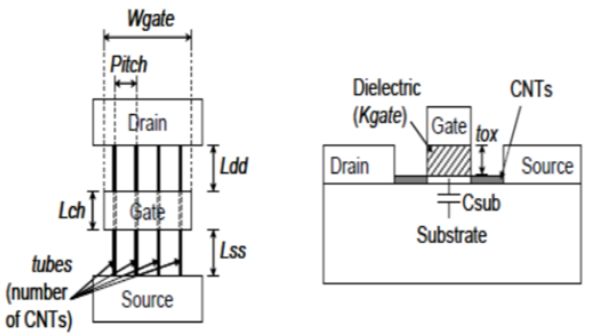

Figure 2. Schematic CNT-FET cross section [12, 29]

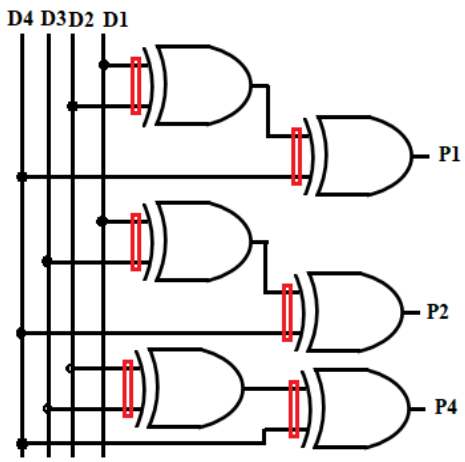

Figure 3. Codeword generation

2. HAMMING ERROR DETECTION

Various error detecting circuits have been discussed in past [30-33], the most common method is the Hamming Error Detection. R. W. Hamming is the inventor of this approach. Errors are not only detected but also corrected using Hamming codes. This method can detect and also capable to correct errors of two bit at the same time [3, 34]. While simple parity method cannot fix errors and can only discover odd number of them. R. W. Hamming introduced the (7, 4) coding in 1950. This method converts four data bits to seven after addition of three parity bits. Single-bit errors can be detected and corrected using Hamming (7, 4). It can identify (but not correct) double-bit errors with the inclusion of an overall parity bit [35]. Data bits along with parity bits are used to create a codeword. More than one parity bit is used in this and these are placed at certain positions of power of 2 [3]. Figure 3 represents the proposed CNT based circuit of Hamming Codeword Generation.

Number of parity bits is decided by below equation:

$$2^P \geq n + P + 1$$

where,

n=No. of Data Bits;

P=No. of Parity Bits.

Converting the parity bit value in to decimal equivalent detects error [6]. There is no error if Codeword contains solely 0's.

Let Data Bits=1011

No. of parity bits:

2^P>=n+P+1**;**

Let p=3;

2^3>=4+3+1**;**

8>=8;

So, P=3.

Position of parity bits:

Position of the first parity bit=1 (2°);

Position of the second parity bit=2 (2^1);

Position of the third parity bit=4 (2^2).

7 Bit Codeword will be: D4 D3 D2 P4 D1 P2 P1.

There are 4 data bits and 3 parity bits in this example. As a result, it will be known as the (7, 4) Hamming Code [35].

Calculation of P1

P1=Ex-OR(D1, D2, D4)=Ex-OR (1, 0, 1)

P1=0

Calculation of P2

P2=Ex-OR (D1, D3, D4)=Ex-OR (1, 1, 1)

P2=1

Calculation of P4

P4=Ex-OR (D2, D3, D4)=Ex-OR (0, 1, 1)

P4=0

Decimal equivalent of 010 (P4 P2 P1)=2, Error is found at Second bit.

3. HAMMING ERROR CORRECTION

Figure 4 represents the proposed CNT based Hamming Error Correcting Circuit. For Error Correction by Hamming Code, we are using 3X8 Decoder. Table 1 shows Input Combinations and Output of the Decoder.

Let Inputs of Decoder are: P11, P12 & P14.

Calculation of P11

P11=Ex-OR (P1, D1, D2, D4)=Ex-OR (0, 1, 0, 1)=0

Calculation of P12

P12=Ex-OR (P2, D1, D3, D4)=Ex-OR (1, 1, 1, 1)=0

Calculation of P14

P14=Ex-OR (P4, D2, D3, D4)=Ex-OR (0, 0, 1, 1)=0

Let Corrected Codeword is: OUT7 OUT6 OUT5 OUT4 OUT3 OUT2 OUT1.

where,

OUT7=Ex-OR (Y7, D4);

OUT6=Ex-OR (Y6, D3);

OUT5=Ex-OR (Y5, D2);

OUT4=Ex-OR (Y4, P4);

OUT3=Ex-OR (Y3, D1);

OUT2=Ex-OR (Y2, P2);

OUT1=Ex-OR (Y1, P1).

Table 1. Input combinations and output of decoder

Inputs of decoder			Output of decoder
P14	P12	P11	
Logic 0	Logic 0	Logic 0	Y0
Logic 0	Logic 0	Logic 1	Y1
Logic 0	Logic 1	Logic 0	Y2
Logic 0	Logic 1	Logic 1	Y3
Logic 1	Logic 0	Logic 0	Y4
Logic 1	Logic 0	Logic 1	Y5
Logic 1	Logic 1	Logic 0	Y6
Logic 1	Logic 1	Logic 1	Y7

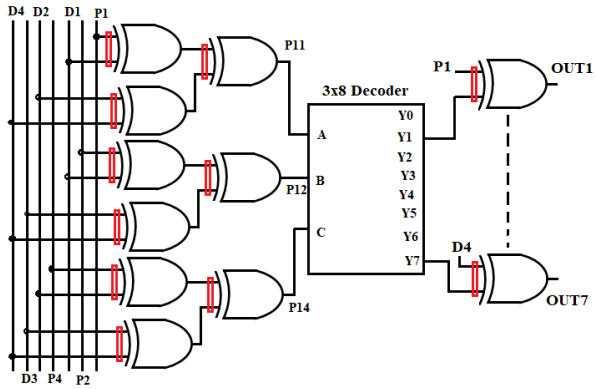

Figure 4. Hamming Error Correcting Circuit

4. RESULTS AND DISCUSSION

4.1 Hamming Error Detection

When the input voltage is varied from 0.7V to 1.3V, Table 2 illustrates the Delay and Average Power Consumption using CMOS and CNTFET while Table 3 represents power-delay-product. The tables demonstrates that the delay with proposed CNTFET is shorter than the delay with CMOS, and that the power consumption with proposed CNTFET is less than the power consumption with CMOS. In addition, the power delay product of CNTFET is lower than that of CMOS.

When the temperature is varied from 0°C to 75°C, Table 4 illustrates the Delay and Average Power Consumption using CMOS and CNTFET while Table 5 represents power-delay-product. The tables demonstrates that the delay in proposed CNTFET is smaller than the delay in CMOS, and that the power consumption in CNTFET is likewise much lower than the power consumption in CMOS. In addition, while comparing CNTFET with CMOS, it can be shown that the power delay product is lower in proposed CNTFET. Average Power Comparison on Different Input Voltages and on different temperatures of Hamming Error Detection are represented by Figure 5 and Figure 6 respectively. Figure 7 and Figure 8 represents PDP as a function of supply voltage and temperature of Hamming Error Detection respectively.

Table 2. Delay and average power comparison on input voltage variation when temp=25°C

Input voltage (V)	Delay (CMOS) (nS)	Delay (CNTFET) (nS)	Average power (CMOS) (µW)	Average power (CNTFET) (µW)
0.7	5.0792	5.0017	9.44	1.14
0.9	5.0446	5.0082	16.38	2.60
1.1	5.0337	5.0089	30.56	5.56
1.3	5.0277	5.0092	61.59	9.74

Table 3. Power delay product on input voltage variation when temp=25°C

Input Voltage (V)	PDP (CMOS) (fJ)	PDP (CNTFET) (fJ)
0.7	47.94	5.736
0.9	82.66	13.02
1.1	153.8	27.85
1.3	309.67	48.83

Table 4. Delay and average power comparison on temperature variation when input voltage=0.9V

Temp. (°C)	Delay (CMOS) (nS)	Delay (CNTFET) (nS)	Average power (CMOS) (µW)	Average power (CNTFET) (µW)
0	5.04	5.01	16.06	2.601
25	5.04	5.01	16.38	2.601
50	5.05	5.01	16.80	2.601
75	5.057	5.01	17.30	2.601

Table 5. Power delay product on temperature variation when input voltage=0.9V

Temperature (°C)	PDP (CMOS) (fJ)	PDP (CNTFET) (fJ)
0	80.94	13.02
25	82.66	13.02
50	84.89	13.02
75	87.49	13.02

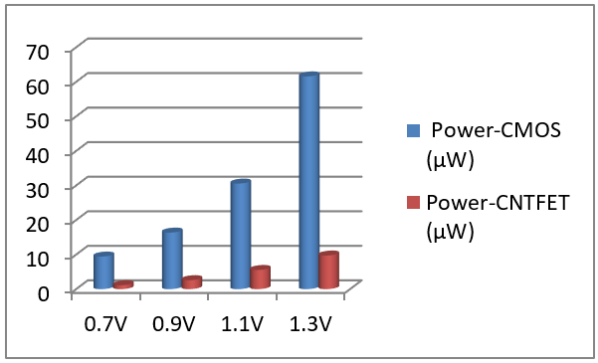

Figure 5. Average power comparison on different input voltages of Hamming Error Detection

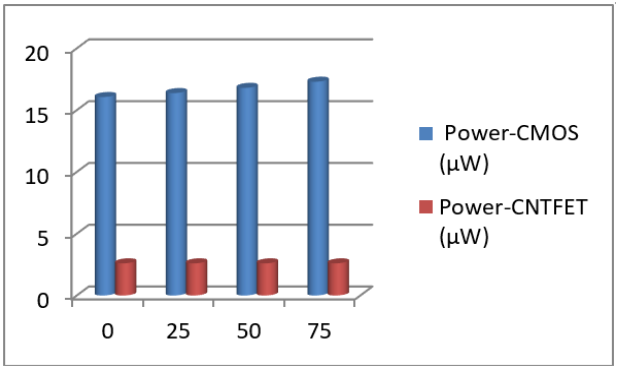

Figure 6. Average power comparison on different temperatures of Hamming Error Detection

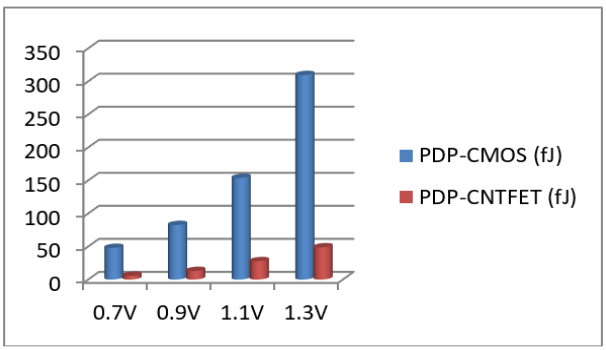

Figure 7. PDP vs. supply voltage (V) of Hamming Error Detection

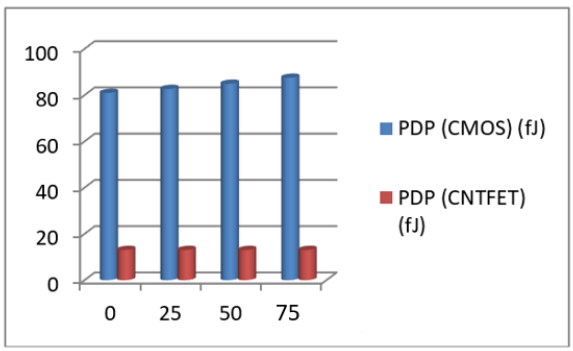

Figure 8. PDP vs. temperature (°C) of Hamming Error Detection

4.2 Hamming Error Correction

When the input voltage is varied from 0.7V to 1.3V, Table 6 illustrates the Delay and Average Power Consumption using CMOS and CNTFET while Table 7 represents power-delay-product. The tables demonstrates that the delay with CNTFET is shorter than the delay with CMOS, and that the power consumption with CNTFET is less than the power consumption with CMOS. In addition, the power delay product of CNTFET is lower than that of CMOS.

When the temperature is varied from 0°C to 75°C, Table 8 illustrates the Delay and Average Power Consumption using CMOS and CNTFET while Table 9 represents power-delay-product. The tables demonstrates that the delay in CNTFET is smaller than the delay in CMOS, and that the power consumption in CNTFET is likewise much lower than the power consumption in CMOS. In addition, while comparing CNTFET with CMOS, it can be shown that the power delay product is lower in CNTFET. Average Power Comparison on Different Input Voltages and on different temperatures of Hamming Error Correction are represented by Figure 9 and Figure 10 respectively. Figure 11 and Figure 12 represents PDP as a function of supply voltage and temperature of Hamming Error Correction respectively.

Table 6. Delay and average power comparison on input voltage variation when temp=25°C

Input voltage (V)	Delay (CMOS) (nS)	Delay (CNTFET) (nS)	Average power (CMOS) (µW)	Average power (CNTFET) (µW)
0.7	5.531	3.623	57.41	2.62
0.9	6.136	3.764	102.74	5.209
1.1	6.109	4.304	177.46	9.258
1.3	5.376	4.435	333.23	14.99

Table 7. Power delay product on input voltage variation when temperature=25°C

Input voltage (V)	PDP (CMOS) (fJ)	PDP (CNTFET) (fJ)
0.7	317.58	9.49
0.9	630.50	19.60
1.1	1084.13	39.85
1.3	1791.47	66.52

Table 8. Delay and average power comparison on temperature variation when input voltage=0.9V

Temperature (°C)	Delay (CMOS) (nS)	Delay (CNTFET) (nS)	Average Power (CMOS) (µW)	Average Power (CNTFET) (µW)
0	6.1246	3.7644	102.02	5.2092
25	6.1369	3.7644	102.74	5.2092
50	6.1498	3.7644	102.83	5.2092
75	5.4655	3.7644	104.17	5.2092

Table 9. Power delay product on temperature variation when input voltage=0.9V

Temperature (°C)	PDP (CMOS) (fJ)	PDP (CNTFET) (fJ)
0	624.83	19.609
25	630.505	19.609
50	632.38	19.609
75	569.34	19.609

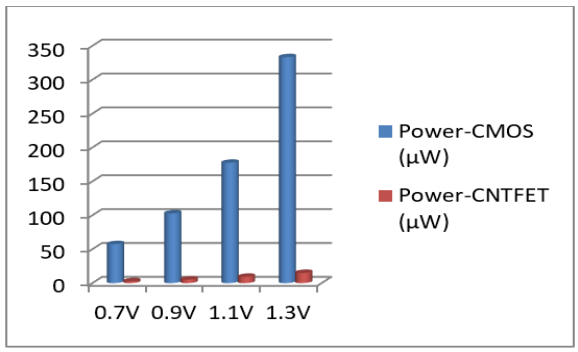

Figure 9. Average power comparison on different input voltages of Hamming Error Correction

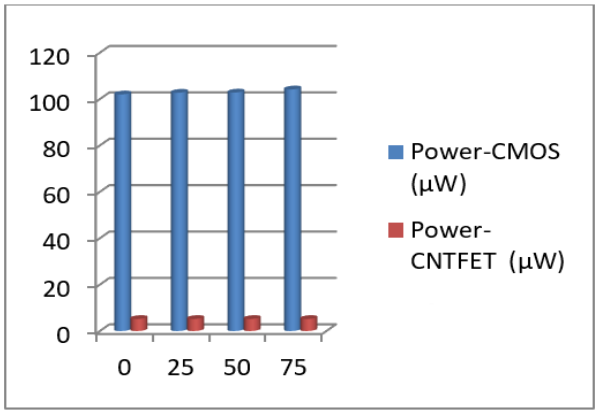

Figure 10. Average power comparison on different temperatures of Hamming Error Correction

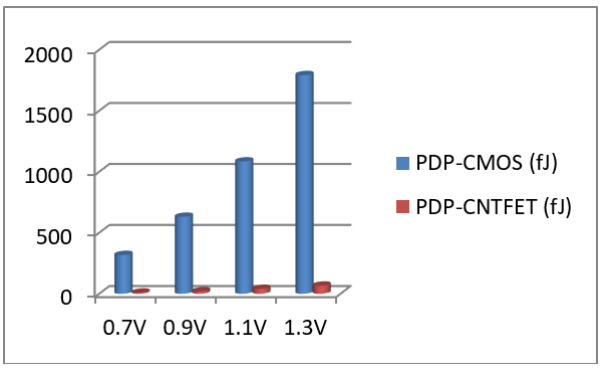

Figure 11. PDP vs. supply voltage (V) of Hamming Error Correction

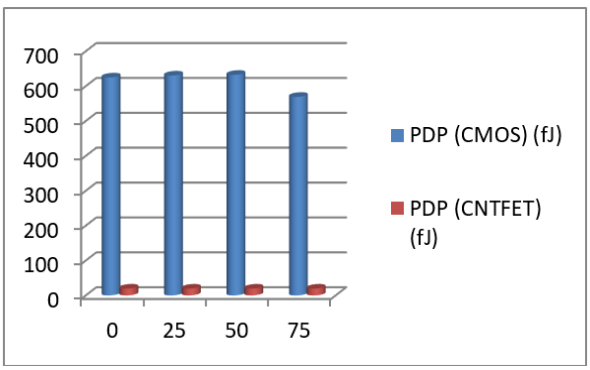

Figure 12. PDP vs. temperature (°C) of Hamming Error Correction

5. CONCLUSIONS

For error-free communication, Hamming Error Detecting and Correcting Circuits are commonly employed. In this paper, CNTFET-based Hamming Error Detection and Correction circuits are presented. CNTFET is favoured over CMOS for a variety of reasons, including low power consumption and increased speed. The Hamming Error Detecting and Correcting circuit was simulated using HSPICE. According to comparative charts of typical power consumption utilising CMOS and CNTFET, CNTFET consumes significantly less power than CMOS. The results also show that the delay in the case of CNTFET is shorter than that of CMOS, and that the power delay product for CNTFET is likewise lower than that of CMOS. Therefore, Hamming Error Detecting and Correcting Circuits are suitable for Power Efficient and Portable Systems.

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