Three-level (NPC) shunt active power filter topology for harmonic reduction using different control strategies

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1. INTRODUCTION

Active power filter implemented with two levels voltage source inverters have been widely studied and used to eliminate harmonics and compensate reactive power [1-2]. Due to power handling capabilities of power semiconductors these active power filters are limited in medium power applications. Hybrid topologies shunt passive filter and series active filter were proposed to achieve high power filters [3]. Recently, there has been an increasing interest in using multilevel inverters for high power drives and reactive power and harmonics compensation [4-5]. Multilevel pulse width modulation inverters can be used as active power filter for high power applications solving the problem of power semiconductor limitation. The use of neutral-point-clamped (NPC) inverters allows equal voltage sharing of the series connected devices in each phase.

This paper presents an active power filter implemented with a three level NPC voltage source inverter. The proposed current control and DC capacitor voltage control schemes are simple to implement. The hysteresis and PWM technique are employed to generate the inverter switching signals and p-q theory [6-7] for harmonic current identification. MATLAB power system blocks are used to carry out the simulation work.

2. DESCRIPTION OF THE APF TOPOLOGY

Figure 1 presents a classical three-leg shunt active power system. It is composed of a grid (esi for i={1, 2, 3}), a non-linear load, a voltage source converter. The load is a three phase diode rectifier feeding a series (R, L) load. The grid is supposed to be balanced with equal series resistance \( R_s \) and inductance \( L_s \) for each phase. The static converter is a voltage source inverter with equal series inductance \( L_f \) for each phase [8-9].

The output currents of the shunt active filter are controlled by Hysteresis controllers and PWM control to provide reactive power and harmonic currents generated by the non-linear load to ensure filtering. Several faulty cases can occur: power switch or power switch driver can be faulty. In each case, it results in the following models:

- A switch is closed instead of being normally open. It results in a short-circuit of the DC voltage source, increasing is 123 current. To isolate the faulty switch as fast as possible, one can use fuses.
- A switch is open instead of being normally closed. It results in an open phase. The filter may continue injecting currents to the power supply. These currents don't cause any prompt risk because they are at the same range level as the case of no-fault condition. However, the filter in this case is polluting more the power supply instead of elimination of harmonic currents of non-linear load. This case is considered in this paper.
2.1 Three-level voltage inverter

Figure 2, describes the structure of three-level voltage inverter. The diodes are used to make the connection with the point of reference O to obtain Midpoint voltages. In order to produce a voltage of N-Level, N-1 capacities are required. The voltage across each condenser is equal to \( E/(N-1) \), E is the total voltage of the DC source. Each couple of switches (S1, S3) form a cell of commutation, the two switches are ordered in a complementary way [10].

The inverter provides three voltage levels according to (1):

\[
v_{io} = K_i E / 2
\]

where
- \( V_{io} \): is the phase-to-middle fictive point voltage
- \( K_i \): is the switching state variable (\( K_i = 1, 0, -1 \))
- \( E \): is the DC source voltage
- \( i \): is the phase index (i=a, b, c). The three-level voltages are shown in Table 1 (E/2, 0, -E/2).

### Table 1. Obtaining of three-level inverters

<table>
<thead>
<tr>
<th>( K_i )</th>
<th>( T_{1a} )</th>
<th>( T_{1b} )</th>
<th>( T_{1c} )</th>
<th>( T_{1d} )</th>
<th>( V_{io} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>E/2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-E/2</td>
</tr>
</tbody>
</table>

The phase-to-neutral point voltage \( V_{in} \) is linked to \( V_{io} \) via:

\[
v_{in} = v_{ia} + v_{io} + v_{io}
\]  

(2)

Assuming that the system is balanced, then:

\[
v_{ia} + v_{ib} + v_{ic} = 0
\]  

(3)

By substituting (3) in (2), the equation presented below is obtained:

\[
v_{io} = 1/3(v_{ia} + v_{ib} + v_{ic})
\]  

(4)
The expressions of instantaneous inverter phase output voltages are obtained by replacing (4) in (2):

\[
\begin{bmatrix}
  v_{a}\n  v_{b}\n  v_{c}
\end{bmatrix} = \begin{bmatrix}
  2/3 -1/3 -1/3 \\
  -1/3 2/3 -1/3 \\
  -1/3 -1/3 2/3
\end{bmatrix} \begin{bmatrix}
  v_{ao} \\
  v_{bo} \\
  v_{co}
\end{bmatrix}
\]

(5)

The line to line voltages are determined by the following equation:

\[
\begin{bmatrix}
  v_{ab} \\
  v_{bc} \\
  v_{ca}
\end{bmatrix} = \begin{bmatrix}
  1 -1 0 \\
  0 1 -1 \\
  -1 0 2
\end{bmatrix} \begin{bmatrix}
  v_{ao} \\
  v_{bo} \\
  v_{co}
\end{bmatrix}
\]

(6)

2.2. Reference current calculation

Several methods were proposed for the identification of the harmonic current references. Mainly, the methods based on the FFT (Fast Fourier Transformation) in the frequency domain and the methods based on instantaneous power calculation in the time domain. In this study, the 

\[
pq\]

theory method is used allowing the compensation of harmonic currents, reactive power and unbalanced currents. The reference currents (harmonic currents) identification is based on \(\alpha\beta\) transformation to obtain real and imaginary powers.

\[
\begin{bmatrix}
  X_{a} \\
  X_{s\beta}
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
  1 & -1 & 1 \\
  2 & 0 & 1 \\
  2 & 0 & -1
\end{bmatrix} \begin{bmatrix}
  X_{1} \\
  X_{2} \\
  X_{3}
\end{bmatrix}
\]

(7)

The instantaneous active and reactive powers of the system are calculated as follows:

\[
\begin{bmatrix}
  p \\
  q
\end{bmatrix} = \begin{bmatrix}
  v_{sa} & v_{s\beta} \\
  -v_{s\beta} & v_{sa}
\end{bmatrix} \begin{bmatrix}
  i_{ca} \\
  i_{c\beta}
\end{bmatrix}
\]

(8)

Instantaneous powers are composed from a constant part and a variable part corresponding to fundamental and harmonic currents respectively.

\[
\begin{bmatrix}
  i_{ca} \\
  i_{c\beta}
\end{bmatrix} = \frac{1}{v_{sa}^2 + v_{s\beta}^2} \begin{bmatrix}
  v_{sa} & -v_{s\beta} \\
  v_{s\beta} & v_{sa}
\end{bmatrix} \begin{bmatrix}
  \tilde{p} \\
  \tilde{q}
\end{bmatrix}
\]

(9)

3. CURRENT CONTROL BY HYSTERESIS

The method is based on the comparison of the difference \(\varepsilon\) between the current reference and the measured currents with a fixed band. Each violation of this band gives a switching command switches to Figure 3.

4. HARMONIC CURRENTS CONTROL USING PWM

This control implements initially a proportional controller which starts from the difference between the injected current (active filter current) and reference current (identified current) that determines the reference voltage of the inverter (modulating wave). This standard reference voltage is compared with two carrying triangular identical waves shifted one from other by a half period of chopping. The control of inverter arm constituting the filter is summarized in the two following stages.

• Determination of the intermediate signals \(V_{i1}\) and \(V_{i2}\).
  - If error \(\geq\) carrying 1=>\(V_{i1}=1\)
  - If error < carrying 1=>\(V_{i1}=0\)
  - If error \(\geq\) carrying 2=>\(V_{i2}=0\)
  - If error < carrying 2=>\(V_{i2}=1\)

• Determination of control signals of the switches \(T_{ij}\) (j=1, 2, 3, 4).
  - If \(V_{i1}+V_{i2}=1\) => \(T_{i1}=1, T_{i2}=1, T_{i3}=0, T_{i4}=0\)
  - If \(V_{i1}+V_{i2}=0\) => \(T_{i1}=0, T_{i2}=1, T_{i3}=1, T_{i4}=0\)
  - If \(V_{i1}+V_{i2}=-1\) => \(T_{i1}=0, T_{i2}=0, T_{i3}=1, T_{i4}=1\)

The general block diagram of control currents is illustrated in Figure 4.

5. DC CAPACITOR VOLTAGE CONTROL

The capacitors (C1 and C2) average voltage (\(V_{dc1}, V_{dc2}\))
has to be maintained at a fixed value. The main cause of its variation is the active filter switching losses and output filter. To ensure inverter permanent and continuous voltage supply, a controlled scheme is adopted as illustrated in Figure 5.

![Figure 5. Dc voltage control block](image)

6. RESULTS OF THE SIMULATION

The simulation is carried out using a program working in MATLAB Simulink environment. The simulation parameters are shown in Table 2, presented below.

<table>
<thead>
<tr>
<th>Table 2. Simulation parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Source settings</strong></td>
</tr>
<tr>
<td><strong>Lcc=0.2136.10^-6H</strong></td>
</tr>
<tr>
<td><strong>Active filter settings</strong></td>
</tr>
<tr>
<td><strong>Lf=0.004 H</strong></td>
</tr>
<tr>
<td><strong>Load parameters</strong></td>
</tr>
<tr>
<td><strong>Lch=0.1H</strong></td>
</tr>
<tr>
<td><strong>For the load variation at t=0.04s</strong></td>
</tr>
<tr>
<td>From 0.04 s to 0.1s: Rch=13.13 Ω, Lch=0.1 H</td>
</tr>
</tbody>
</table>

The frequency spectrum of the line currents presents the presence of several harmonics of amplitudes which coincide with those developed theoretically (THDI=31.63%).

6.1 Hysteresis control strategy for a band Δh=0.1 A

![Figure 7. Currents injected by the inverter and their frequency spectra for the hysteresis control (Δh = 0.1 A)](image)
Figure 8. Reference currents, injected and their frequency spectra for the hysteresis control (Δh=0.1 A)

Figure 9. Source currents after filtering and their frequency spectra for the hysteresis control (Δh=0.1 A)
6.2 Hysteresis control strategy for a band $\Delta h=1$ A

**Figure 10.** Currents injected by the inverter and their frequency spectra for the hysteresis control ($\Delta h=1$ A)

**Figure 11.** Reference currents, injected and their spectra for control with hysteresis ($\Delta h=1$ A)
Figure 12. Source currents after filtering and their frequency spectra for the hysteresis control ($\Delta h=1$ A)

6.3 MLI command with two carriers for a frequency 2500Hz

Figure 13. Currents injected by the filter and their frequency spectra for the control at MLI ($f_p=2500$ Hz)
Figure 14. Reference currents, injected and their frequency spectra for the PWM control (fp=2500 Hz)

Figure 15. Source currents after filtering and their frequency spectra for the PWM control (fp=2500 Hz)
6.4 MLI command with two carriers for a frequency 7500Hz

Figure 16. Currents injected by the filter and their frequency spectra for the control at MLI (fp=7500 Hz)

Figure 17. Reference currents, injected and their frequency spectra for the PWM control (fp=7500 Hz)
7. RESULTS AND DISCUSSIONS

The table below present the summary results of the different simulations obtained for the direct control strategy applied to the topologies of Three-level shunt active power filter.

Table 3. Synthesis of the results

<table>
<thead>
<tr>
<th>Method</th>
<th>THD%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Controlled hysteresis</td>
<td>Δh=0.1 A: 4.17%</td>
</tr>
<tr>
<td></td>
<td>Δh=1 A: 4.96%</td>
</tr>
<tr>
<td>Controlled PWM</td>
<td>fp=2500Hz: 4.21%</td>
</tr>
<tr>
<td></td>
<td>fp=7500Hz: 4.18%</td>
</tr>
</tbody>
</table>

Three-level shunt active power filter performances are related to current references quality, p-q theory is used for harmonic currents identification and calculation the obtained current is shown in Figure 8. This method is very important; it allows harmonic currents and reactive power compensation simultaneously, the obtained current and voltage waveforms are in phase as illustrated the Figure 9, 12, 15 and 18.  

The reduction of the hysteresis band leads to an improvement of the quality of the currents: (THD=4.17% for Δh=0.1 A and THD=4.96% for the case Δh=1 A).

- The increase of the hash frequency leads to an improvement of the quality of the currents: (THD=4.21% for fp=2500Hz and THD=4.18% for fp=7500Hz).

8. CONCLUSION

A theoretical study with simulation of three-level shunt active power filter controlled with the hysteresis and PWM modulation was presented and analyzed in this paper. The three-level APF provides numerous advantages such as improvement of the supply current wave form, less harmonic distortion (THD <5%), which responds well to international standards and its use in high power/medium voltage with a lower maximum device rating. The effectiveness of the proposed scheme is proved by simulation using MATLAB.

REFERENCES


