AMSE JOURNALS-AMSE IIETA publication-2017-Series: Modelling A; Vol. 90; N°2; pp 209-220
Submitted Mar. 26, 2017; Revised May 18, 2017; Accepted Jun. 15, 2017

SOPC-based Magnet Flux Measurement System

Baohai Yang*, Changchun Yang, Qin Xu, ZeLiang Liu, Jing Luo, Ningli Liang

College of Electronic Engineering, Jiujiang University, Jiujiang 332005, China
(Corresponding author's email: yangbaohai@sohu.com)

Abstract

To overcome the impreciseness and poor stability of the traditional flux measurement systems, this paper puts forward an SOPC-based flux measurement system that integrates the main control system into an FPGA chip. Centred on the SOPC, the proposed system replaces the traditional analogue integrator with the digital integrator. In addition to digital filtering and auto-calibration, the proposed system realizes automatic range selection, digital integration and other logic functions. It is proved that the system boasts great market potential with measurement accuracy above 0.5% and no drift phenomenon.

Key words

System on a Programmable Chip (SOPC), Field-Programmable Gate Array (FPGA), Magnet flux measurement, Digital integrator.

1. Introduction

With the rapid development of electronics and information technology in recent years, the magnetic materials have been extensively applied in China, posing stricter requirements on the magnetic flux measurement system. Most of the traditional flux measurement systems are cantered on the operational amplifier, which causes increase in input offset voltage/current, temperature drift, and undesirable resistance of the components. Under the combined effect of these factors, the system may suffer from significant zero drift, and even result in the integrator failure [1]. The impreciseness and poor stability of these systems have severely constrained the development of magnetic materials. To make up for the defects, some designers have tried to enhance the system

performance with better op-amps and electronic components. Nevertheless, the enhancement is very limited because it relies on analogue resistor-capacitor (RC) integrator, which is featured by inconsistencies and imperfections [2]. In view of the problems of the traditional systems, this paper puts forward an SOPC-based flux measurement system [3] that integrates the main control system into a FPGA chip, and realizes all the functions (e.g. measurement and display) with the SOPC [4]. Compared with the traditional system, the SOPC-based system boasts deep integration, good anti-interference, high accuracy, and, most importantly, the online update function.

2. Measurement Principle

2.1 Digital Integration Algorithm

The Helmholtz coil was adopted for measurement. Assuming that the coil has N turns and a magnetic flux of Φ, the electromotive force (EMF) can be expressed as follows according to Faraday's law of induction:

$$e(t) = N\frac{\mathrm{d}\phi}{\mathrm{d}t} \tag{1}$$

It can be seen that EMF is proportional to the rate of change of the magnetic flux.

Through the integration of e in formula (1), the variation of Φ can be expressed as:

$$\Delta\phi = \phi(t) = \phi(0) = \frac{1}{N}\int_0^t e(t)\mathrm{d}t \tag{2}$$

Suppose the magnetic flux is 0 at time 0, then $\Phi(0) = 0$, and $\Phi(t) = \Delta\Phi$. As shown in Figure 1, the right trapezoid represents the voltage signal curve across the coil.

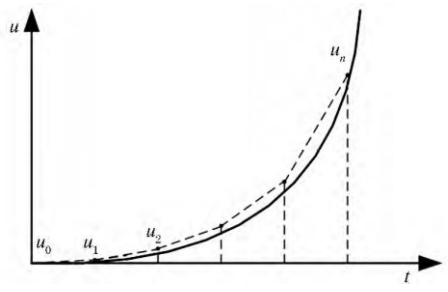

Fig.1. The Compound Trapezoidal Integration

According to the figure above, the height is negatively correlated with the approximation of the right trapezoid, but positively correlated with the error of the digital integration [5]. Then, the compound trapezoid integration can be expressed as:

$$\phi(0) = \int_0^t u(t)\mathrm{d}t \approx \frac{\Delta t}{2}\left[u(0) + 2\sum_{i=1}^{n-1} + u(n)\right] \tag{3}$$

In the digital domain, the integration algorithm can be rewritten as:

$$F(n) = F(n-1) + \frac{T}{2}\left[u(n-1) + u(n)\right] \tag{4}$$

where T is the sampling period. Thus, the transfer function of the system can be expressed as:

$$H(z) = \frac{T(z+1)}{2(z-1)} \tag{5}$$

2.2 Algorithm Simulation

The frequency characteristics of the digital integration algorithm can be expressed as:

$$H(e^{j\omega}) = H(z)\Big|_{z=e^{j\omega}} = \frac{T(e^{j\omega}+1)}{2(e^{j\omega}-1)} \tag{6}$$

Based on the simulation software MATLAB, the author compared the frequency responses of the digital integrator and the ideal integrator $\left(H(e^{j\omega} = \frac{T}{j\omega})\right)$. The comparison results are illustrated in Figure 2. As can be seen from Figure 2, the amplitude frequency curve of the digital integrator is in close proximity to that of the ideal integrator [6].

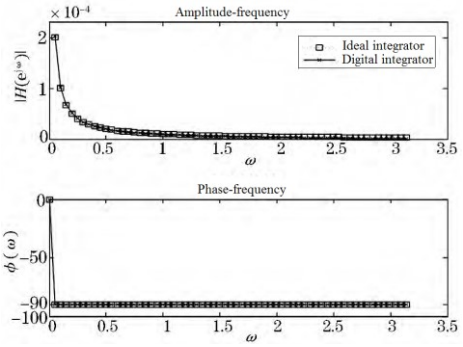

Fig.2. Curve Graph of Frequency Response

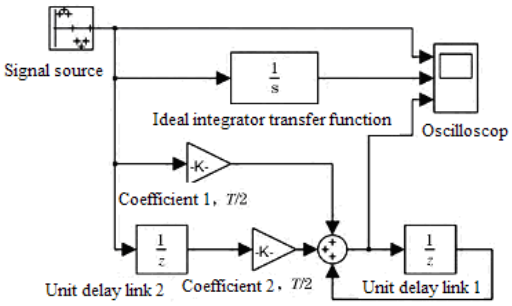

Fig.3. Simulation Model of the Digital Integrator

In light of formula (4), the Simulink was adopted to construct the digital integrator model. Moreover, a three-channel oscilloscope was introduced to integrate the discrete sine signal. Denoted as Channels 1, 2 and 3, the three channels were connected to the original signal sequence, the ideal integrator output and the digital integrator output [7], respectively. The details on the model are presented in Figure 3.

Figure 4 displays the simulated results of the model (Figure 3) were processed in the Founder software. It can be observed that the digital integrator outputted the same waveform with the ideal integrator, and the phase difference between the output and input waveforms was 90°. The consistency between simulation and formula derivation results [8] proves that the digital integration algorithm is close to an ideal integrator.

3. Hardware Design

3.1 General Design of the System

According to the general design in Figure 5, the system consists of such three parts as the amplifier circuit, the AD convertor circuit and the SPOC, the centrepiece of the magnetic flux measurement system. The system operates in the following steps. First, the flux signal induces the voltage signal via the Helmholtz coil; then, the simulation switch selects and amplifies the corresponding signals, conducts simultaneous signal sampling, and transmits the signals to the SPOC; after that, the SPOC makes computations, and shows the measured results on the display.

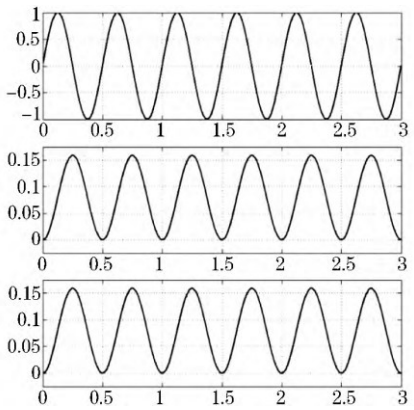

Fig.4. Simulated Waveform of the Digital Integrator

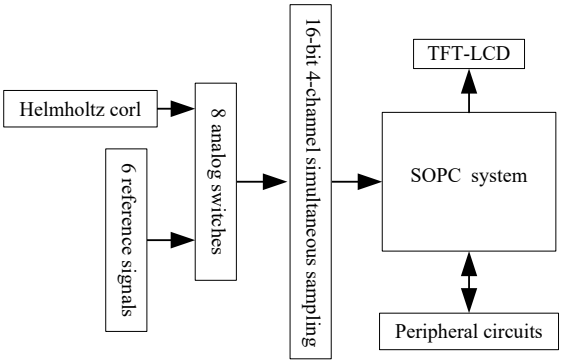

Fig.5. The General Design of the System

3.2 SOPC System

The SOPC system was custom-made with the SOPC Builder, a tool in Quartus II software. EP4CE15F17C8 FPGA (Altera) was employed as the chip of the system. Due to the insufficient chip RAM, an extra 512MB SDRAM chip was added for application to ensure the smooth functioning of the internal procedures [9]. The logic functions of FPGA internal hardware were programmed in VHDL, a hardware description language. In addition to digital filtering and auto-calibration, the FPGA system must realize automatic range selection, digital integration and other logic functions. The top-level design is displayed in Figure 6. In demand of advanced logic functions, the ADC control module should achieve 500kSPS sampling, which is the only way to acquire accurate 4-channel 16-bit data for the zero-drift correction of the zero calibration module.

In application, the accuracy of the measured results is affected by the high sensitivity of the digital integrator to high frequency noises. To solve the problem, a four-channel FIR low-pass filter was designed in the VHDL, laying the basis for 4-channel digital signal filtering. After filtering, the signal will enter the range selection module, which identifies the absolute value of the signal and automatically selects the range [10]. Next, the amplified digits will be sent to the gain correction module, restored to digits corresponding to the original signals, and transmitted to the digital integration module for integration. To prevent integral drift during the digital integration, the system takes any signal that is not big enough after being amplified 1,000 times as noise, and does not perform integral operation on the signal.

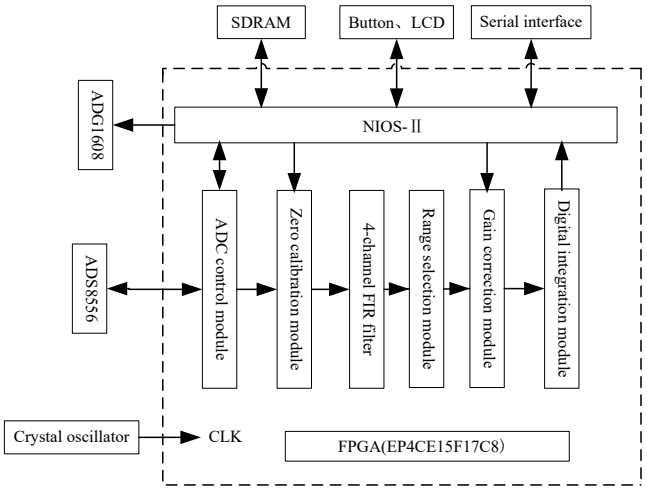

Fig.6. The Top-level Design of the FPGA

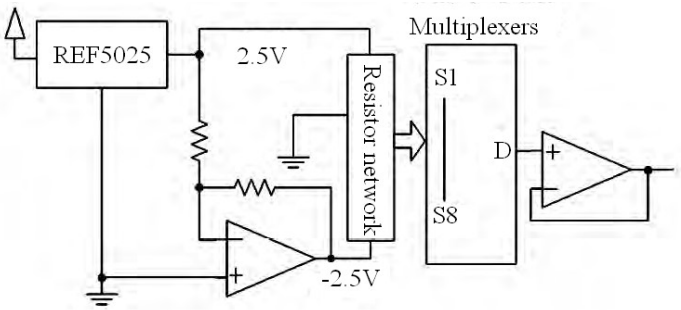

Fig.7. The Correction Circuit

3.3 Correction Circuit

The correction circuit is mainly responsible for zero-point correction and gain correction. In terms of hardware, the circuit is composed of an analogue switch and a reference signal source. The REF5025 voltage chip was selected to generate a reference voltage of 2.5V, and acquire ± 50mV, ± 25mV and ± 2.5mV through a resistor network. The voltage also serves as the external reference source of the ADC. Such a hardware circuit (Figure 7) eliminates the reference voltage drift during correction [11].

Zero-point calibration must be performed before the circuit is put into operation. Taking the strobe signal as the reference voltage, it is possible to correct the gains of 10 times, 100 times, and 1,000 times, and achieve the signals at the stabilizing point [12].

3.4 Amplifier Circuit and AD Converter Circuit

Whereas the range of measured signals is unpredictable in magnetic flux measurement, the system adopts a 4-way amplifier, together with a high-precision 16-bit, 6-channel, simultaneous-

sampling AD chip to realize automatic range selection [13-14]. The hardware circuit design is shown in Figure 8.

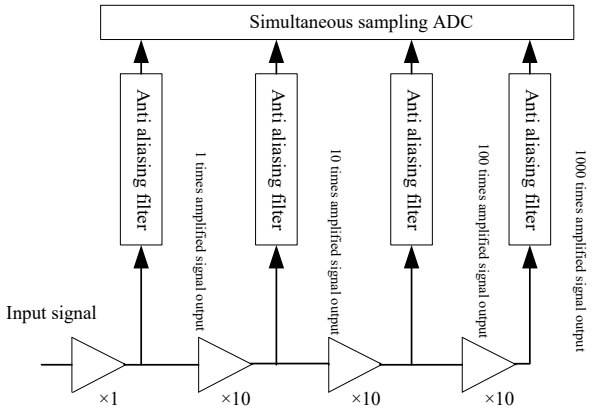

Fig.8. Principles of the Amplifier Circuit and AD Converter Circuit

To ensure the high DC precision of the integrator, the OPA188 amplifier chip (TI) was chosen for the circuit. Capable of automatic zero resetting, the chip has a maximum input offset voltage of 25μV and a maximum temperature drift of only 0.085μV/°C. The plural serial structure was adopted for the hard-point circuit to guarantee the amplified bandwidth. The structure allows the amplifier to make more gains with fewer elements, thus reducing the system cost [15].

The16-bit, 6-channel A/D converter chip is the ADS8556 (TI) with a maximum sampling rate of 630kSPS. After the measured signals are converted, the chip will transmit them in two's complement form through 16-bit parallel port. With an internal clock and reference source, the chip greatly simplifies the design of the hardware circuit. A first-order low-pass filter was installed at the front end of the ADC to reduce the converter's aliasing errors and high frequency noises in the measured signals.

3.5 Display Module

In strict accordance with the design requirements, an Innolux L43T42 display was adopted with the size of 105.5mm×67.2mm×4.05mm (W×H×D), resolution of 640×480, brightness (typical) of 400cd/m2 (16.7M colours), and working temperature range of -20~70 °C. The display module can show four lines simultaneously.

3.6 Key Module

There are 24 keys in the proposed system, including number keys from 0 to 9 and measurement keys of each range, area, reset, clear and confirm.

4. Software Design

The VHFL programmed software mainly covers the calibration module, filter module, and digital integrator module. The FPGA supports parallel data processing, making it possible to achieve fast, real-time sampling. As the control centre of the entire measurement system, the SOPC is responsible for calculating zero-point and gain correction parameters, initializing the keys, driving the display system, and transferring the measured data to the host computer [16].

4.1 Main Program Design

The flow chart of the main program is shown in Figure 9. After switch-on, the system will initialize the entire SOPC system, control the analogue switches to gate, perform zero-point and gain correction, and collect real-time data. Then, the acquired data will be transmitted to the digital integrator for calculation and processing, and eventually exhibited on the LCD display.

4.2 Correction Subprogram Design

For the purpose of accurate measurement, the correction subprogram should always be ran prior to the main program. Responsible for zero correction and gain correction, the correction subprogram can be controlled via the keys in the magnetic flux measurement. During correction, the sampling must be conducted at the rate of 1,024, and the sampled data should be averaged and taken as the correction parameter. The parameter will be transferred to the zero-point correction module and gain correction module. The flow chart of the subprogram is presented in Figure 10.

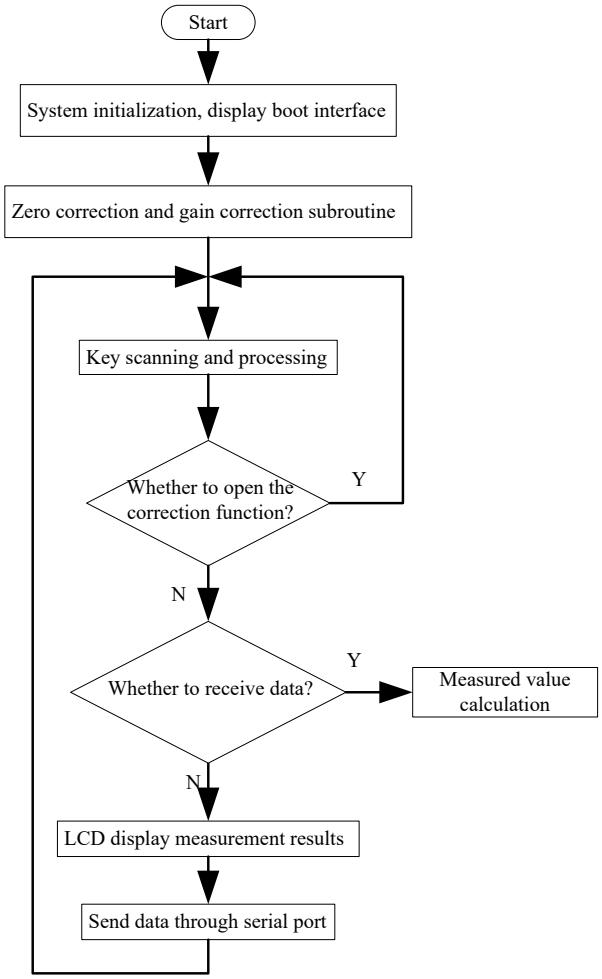

Fig.9. Flow Chart of the Main Program

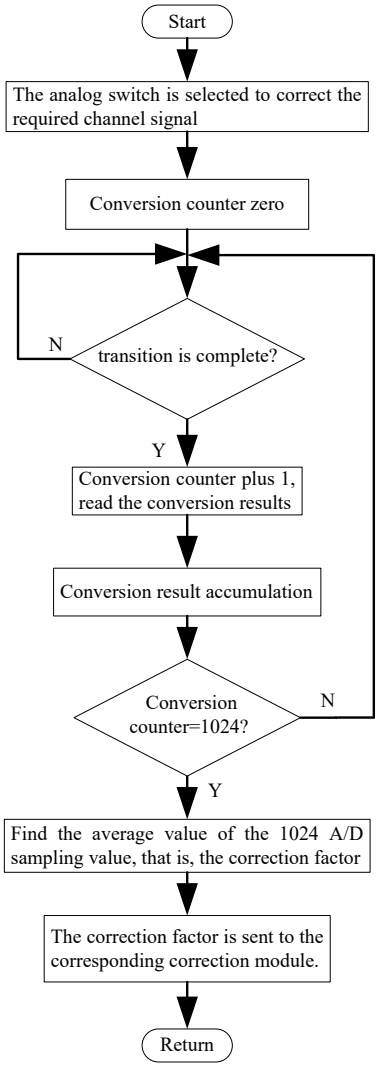

Fig.10. Flow Chart of the Correction Subprogram

5. Test Results and Conclusions

5.1 Test Results

Tab.1. Test Result

Standard signal/mVs	Positive measured value/mWb	Relative error/%	Positive measured value/mWb	Relative error/%
0.1	+0.1025	0.25	-0.0979	0.21
1	+1.014	0.14	-0.998	0.2
10	+10.013	0.13	-9.988	0.12
100	+100.122	0.122	-99.893	0.107
1000	+998.9	0.11	-1001.2	0.12

A system performance test was conducted to verify the effect of the flux measurement system. The signal source was CB-4 voltage picosecond generator (Acer) with five ranges and a time accuracy of 0.01%. The results are listed in Table 1.

The system repeatability was checked in the test. Specifically, the system was applied to test a square magnet for 10 times. The position of the magnet and the sampling rate were kept constant throughout the test. According to the results in Table 2, the repeatability of the results can be expressed as:

$$S(y_i) = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(y_i - \bar{y})^2} = 0.01077$$

Tab.2. The Results of the Repeatability Test

Measuring times	Measured value/mWb	Average value
1	+10.594	
2	+10.596	
3	+10.610	
4	+10.602	
5	+10.593	10.6043
6	+10.598	
7	+10.621	
8	+10.623	
9	+10.599	
10	+10.607	

Conclusion

To overcome the defects of the traditional analogue devices, this paper introduces an SOPC-based magnetic flux measurement system, which integrates the main control system into an FPGA chip and replaces the traditional analogue integrator with digital integrators. The proposed system has obvious advantages over the traditional systems, such as sound stability, no zero drift, automatic range selection, online update, high integration, good automation and advanced intelligence. A series of functional tests were performed to verify the effect of the system. The results demonstrate that the system has good feasibility, excellent accuracy and great market potential.

Acknowledgements

This work is supported by National Science Foundation of China (No.51667009), Research Foundation of health department of Jiangxi Province China (No.20175561), Science Foundation of Jiangxi Provincial Department of Education (No. GJJ161067), Science Foundation of Jiujiang University (No.2016KJ001,No.2016KJ003), National Science Foundation of Jiangxi Province (No.20151BAB207013), Soft Science Research of Jiangxi Province(No. 20161BBA10034).

References

1. C. Chen, The design of handheld meter field calibrator based on SOPC, 2012, Electrical Measurement & Instrumentation, vol. 49, no. 10, pp. 161-164.
2. W.L. Jiang, Y.M. Hu, A. Chen, The placement machine vision processing system based on SOPC, 2011, Instrument Technique and Sensor, no. 3, pp. 79-81.
3. J.J. Zhang, N.J. Pu, Design of the embedded data recorder based on the SOPC, 2011, Journal of Electronic Test, no. 8, pp. 81-83.
4. B.B. Wu, B. Shen, X.Y. Du, Low zero drift digital integrator based on FPGA, 2010, Computer Measurement and Control, vol. 17, no. 7, pp. 1587-1589.
5. S. Chai, X. Li, X. Cheng, Application of electronic integrator in micro-flux measurement system, 2008, Electrical Measurement & Instrumentation, vol. 45, no. 1, pp. 14-16.
6. Y Wang., Z.S. Ji, R. Luo, Design of low automatically compensates for zero drift integrator, 2006, Computer Measurement & Control, vol. 14, no. 4, pp. 530-532.
7. X.Y. Du, Z.S. Ji, Y. Wang, Design of self-adaption intelligent integrator, 2009, Computer Engineering and Applications, vol. 45, no. 9, pp. 85-87.
8. C.B. Liang, G.R. Qin, Z.J. Liang, Electromagnetism, 1995, Beijing: Higher Education Press, pp. 298-299.
9. W.C. Xie, Y.X. Dai, Integral technology research of the rogowski coil electronic current transformer, 2011, Electrical Measurement & Instrumentation, vol. 48, no. 5, pp. 10-13.
10. H. Chen, W. Chen, W. Li, Research and simulation of Rogalski coil digital integrator, 2009, Power System Protection and Control, vol. 37, no. 2, pp. 43-47.
11. R.D. Lu, J.Q. Xiong, On the integrating circuit analysis method, 2004, Journal of Electronics, vol. 28, no. 6, pp. 223-225.
12. L. Jiang, C.L. Wang, L. Liu, et al., The realization of FIR digital filter algorithm based on FPGA, 2006, Ship Electronic Engineering, no. 1, pp. 151-156.

13. Z.G. Wu, The principle and application of ICL7650 chopper-stabilized op amp, 2003, Foreign Electronic Components, vol. 13, no. 4, pp. 41-42.
14. Z.D. Tang, M. Liu, X.M. Liu, The realization of parameterized FIR filter based on high density programmable logic devices, 2002, Chongqing University: Natural Science Edition, vol. 25, no. 3, pp. 72-74.
15. Z.B. Gao, H. Chen, Q.Y. Han, Design and realization of variable 2n point pipelined FFT processor, 2006, Beijing Institute of Technology, vol. 26, no. 4, pp. 338-341.
16. W.H. Du, The zero adjusting method of the practical operational amplifier, 2002, Chengde National Vocational and Technical College, vol. 34, no. 2, pp. 55-56.